

Suspended superconducting weak links from aerosol-synthesized single-walled carbon nanotubes

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S1 Electrode fabrication process

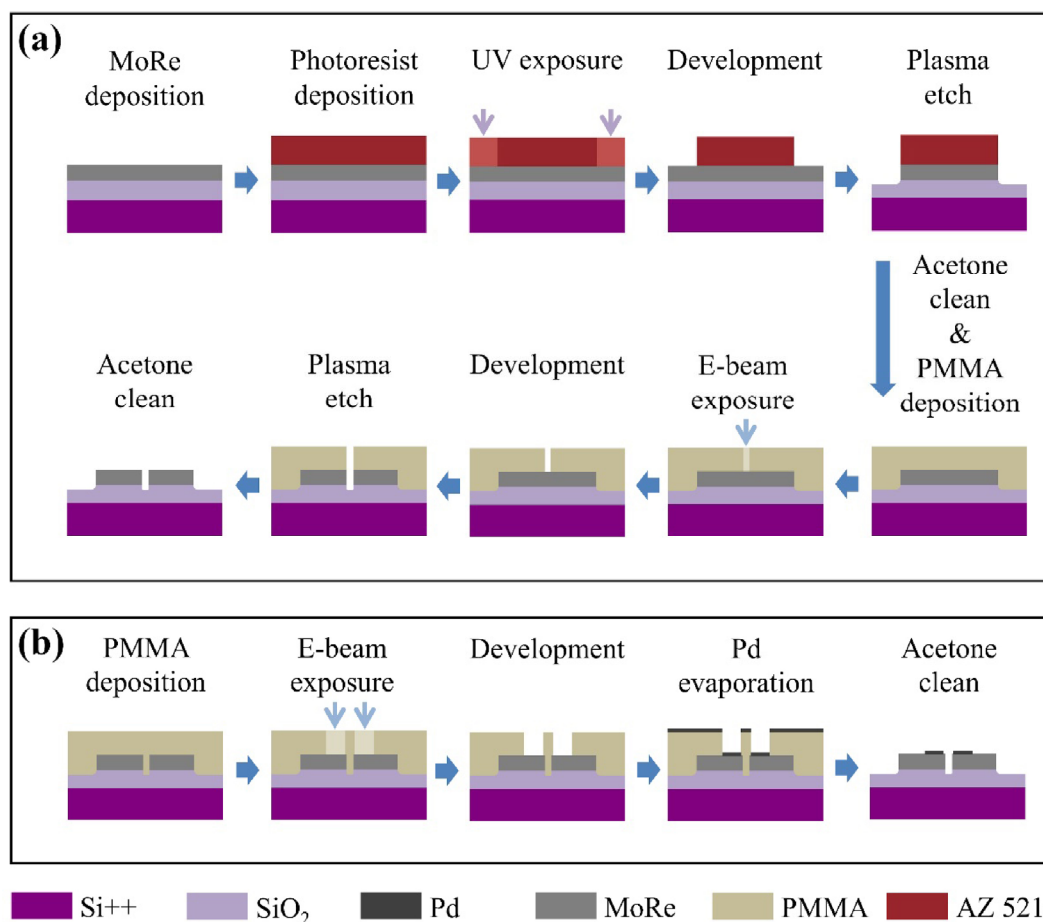


Figure S1 (a) Schematic of the electrode fabrication procedure. MoRe is first deposited onto a Si/SiO₂ wafer by sputtering. Large features of the electrodes are then defined using photolithography. The patterned photoresist (AZ 5214) serves as an etching mask in SF₆/Ar RIE, which removes MoRe from the exposed areas. RIE is followed by a sonication in acetone and a deposition of electron beam resist (PMMA). Source-drain gap is created by patterning a narrow line into this resist by EBL and etching away MoRe from the exposed regions. Finally, the chip is cleaned by a short O₂ plasma etching and a thorough sonication in a heated acetone bath. (b) Schematic of the additional fabrication steps done for the devices with a Pd contact layer. Two 10 μm × 10 μm windows are patterned next to the source-drain gap using EBL and Pd is evaporated onto the chip. Lift-off and cleaning are done in a heated acetone bath.

S2 SEM micrograph of SWCNTs deposited on Si/SiO₂ substrate

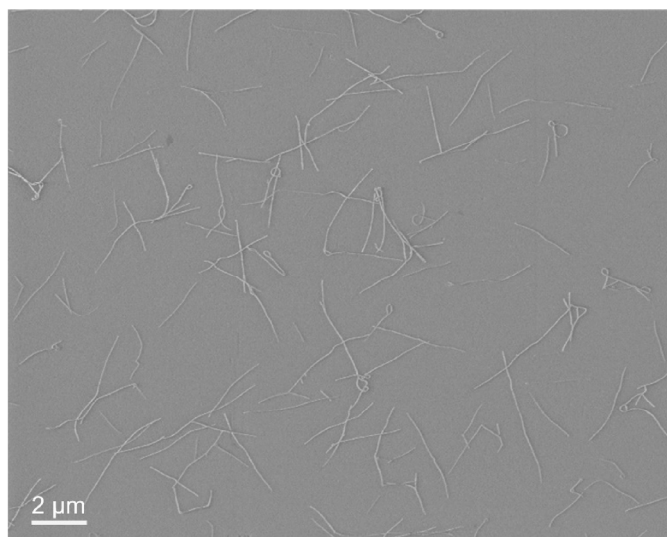


Figure S2 SEM micrograph of SWCNTs on a bare Si/SiO₂ substrate deposited by thermophoretic precipitator [S1].

Growth parameters and deposition times of the floating-catalyst chemical vapour deposition (FC-CVD) process were calibrated by running test depositions on bare Si/SiO₂ chips and imaging the resulting configurations on a scanning electron microscope (SEM). Typical SEM micrograph of deposited single-walled carbon nanotubes (SWCNTs) on a Si/SiO₂ chip is displayed in Fig. S2. In this figure, the density of SWCNTs is rather high and therefore, a shorter deposition time was used when SWCNTs were deposited on the actual device chips. The uniformity of the SWCNT deposition was monitored by taking SEM images at multiple locations of the chip.

S3 Number size distribution and optical absorption spectrum of SWCNTs

Figure S3(a) presents a number size distribution of SWCNT aerosols measured using a scanning mobility particle sizer with a condensed particle counter (SMPS+C). The number concentration of the SWCNTs at the outlet of the CVD reactor was kept around 10^5 cm^{-3} to reduce undesirable bundling of the tubes [S2]. The measured number size distributions were also used to monitor that there was no considerable emission of inactive catalyst nanoparticles out from the reactor.

Figure S3(b) displays an ultraviolet/visible/near-infrared (UV/vis/NIR) absorption spectrum measured from a SWCNT thin film collected by filtration and transferred on a quartz substrate. The positions of the first and second interband transitions of semiconducting SWCNTs (S_{11} and S_{22}) were used to determine the mean diameter of the SWCNTs. The first interband transition of metallic SWCNTs (M_{11}) was also observed in the absorption spectrum.

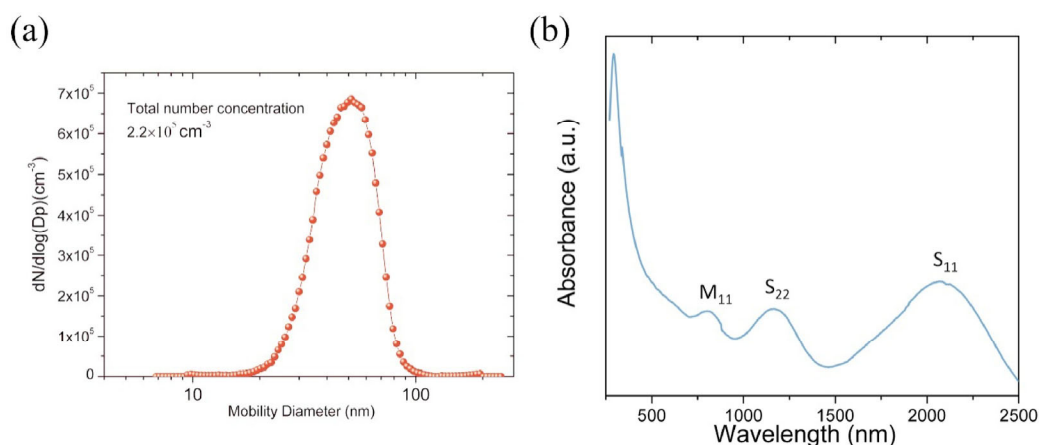


Figure S3 (a) The number size distribution of SWCNTs measured by a scanning mobility particle sizer with a condensed particle counter. The total number concentration deduced from this measurement is $2.2 \times 10^5 \text{ cm}^{-3}$. (b) Optical absorption spectrum of a SWCNT thin film. The mean diameter of the SWCNTs extracted from the absorption spectrum is 1.8 nm.

S4 Quasi-four-terminal measurement configuration

Figure S4 schematically illustrates different kinds of configurations for four-terminal and quasi-four-terminal measurements. In the true four-terminal measurement configuration shown in Fig. S4(a), the voltage and current wires are fully distinct, and they also make separate contacts to the SWCNT. In this configuration both the resistance of the measurement wires and the contact resistance of the SWCNT-electrode interfaces are excluded and only the resistance of the SWCNT is measured. In the

quasi-four-terminal configuration shown in Fig. S4(b), the voltage and current wires are separate, but they have shared contacts to the SWCNT. Therefore, the contact resistances of the SWCNT-electrode interfaces are included in the measurement. However, if the SWCNT-electrode interfaces are considered to belong to the device that is being measured (e.g. SWCNT SNS junction), then this configuration can also be viewed as a true four-terminal measurement of such a device.

In our experimental setup, the voltage and current lines ran separately from room temperature down to the mixing chamber. They were, however, joined just before the SWCNT contact so that the resistance of this common path was also included in the measured total resistance. A schematic of this 'stretched quasi-four-terminal' measurement configuration is shown in Fig. S4(c). The voltage and the current lines for our molybdenum-rhenium (MoRe) devices were combined to single copper strips on a printed circuit board (PCB) using aluminium bonding wires. Aluminium bonding wires were also used to make the subsequent connections from the PCB copper strips to the MoRe leads on the chip. The bonding wire configuration is displayed in Fig. S5. Aluminium bonding wires (MoRe leads) become superconducting below 1.2 K (6.5 K) so the common MoRe + Al parts of the voltage and the current lines were superconducting at low temperatures. In this situation, the stretched quasi-four-terminal measurement configuration reduces to the quasi-four-terminal case shown in Fig. S4(b). At higher temperatures, MoRe leads and bonding wires were normal conducting and their resistance was included in the measurement. This allowed us to detect the superconducting transition of the MoRe leads.

The devices with MoRe/palladium (Pd) leads were measured in a similar fashion using a stretched quasi-four-terminal configuration. In this setting, the voltage and the current wires were combined outside the sample box using a tee adapter. Therefore, a small additional resistance ($< 1 \Omega$) due to ~ 10 -cm-long coaxial cables and ~ 1 -cm-long PCB transmission lines was measured in series with this device.

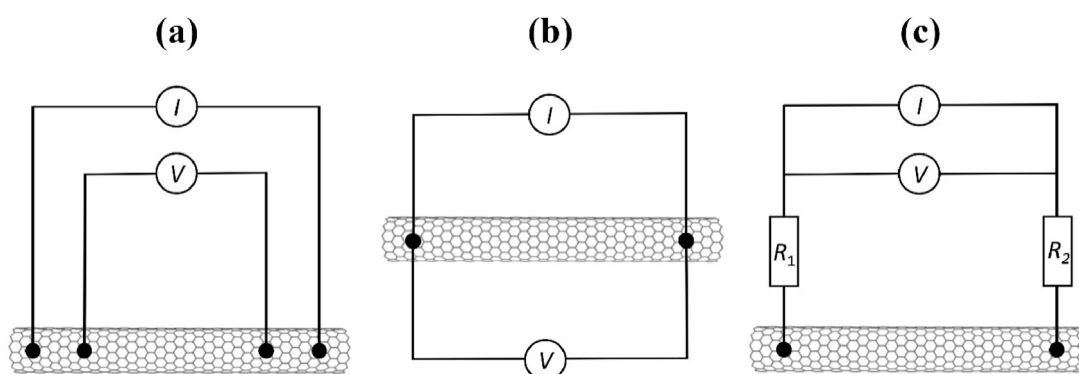


Figure S4 Schematics of varied four-terminal measurement configurations. (a) Four-terminal measurement configuration of a SWCNT. This configuration excludes both the resistance of the measurement wires and the resistance of the SWCNT-electrode contacts. (b) Quasi-four-terminal measurement configuration of a SWCNT. This configuration excludes the resistance of the measurement wires but includes the contact resistances. (c) 'Stretched quasi-four-terminal' measurement configuration with partially shared voltage and current leads. Resistances of the shared leads (R_1 , R_2) also contribute to the measurement in this configuration. If the shared leads are superconducting, this stretched quasi-four-terminal configuration is equal to the quasi-four-terminal one.

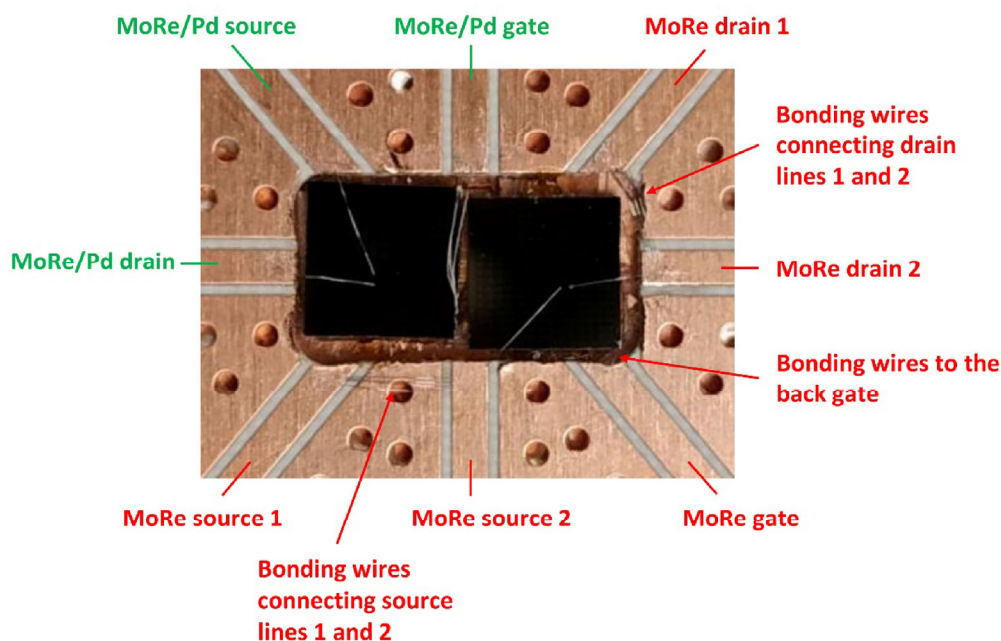


Figure S5 Illustration of the bonding wire configuration used in the low temperature measurements. Each of the source and drain lines were split to allow for quasi-four-terminal measurements. In the device with MoRe leads (red), this splitting was done on a printed circuit board using aluminium bonding wires as shown in the figure. The source and drain lines of the device with MoRe/Pd contacts (green) were split outside the sample box using an SMA tee adapter.

S5 Fourier transform of the Fabry-Pérot pattern

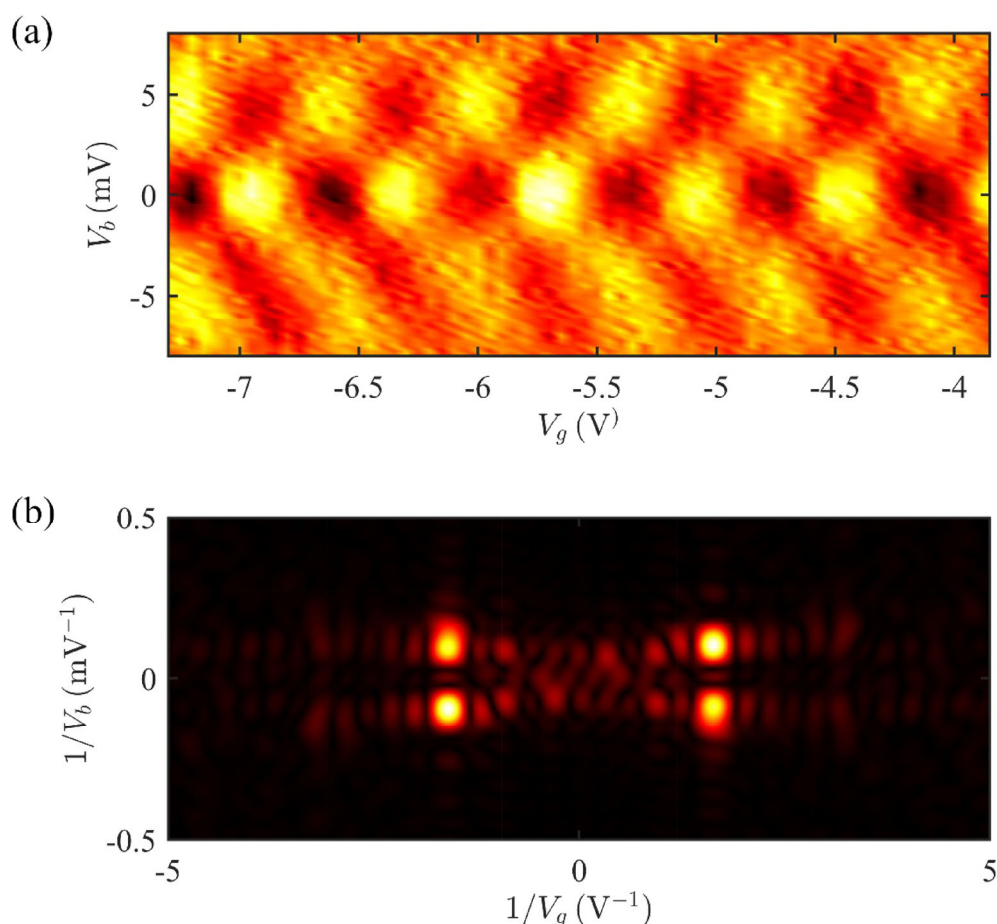


Figure S6 (a) Figure 3 of the main text differentiated with respect to gate voltage V_g . (b) Fourier transform of (a). Four main peaks can be identified from this figure, which is expected for a single Fabry-Pérot resonant cavity. The small ripples seen in this figure are likely caused by additional scattering and limited sample interval.

S6 SEM micrographs of the measured devices

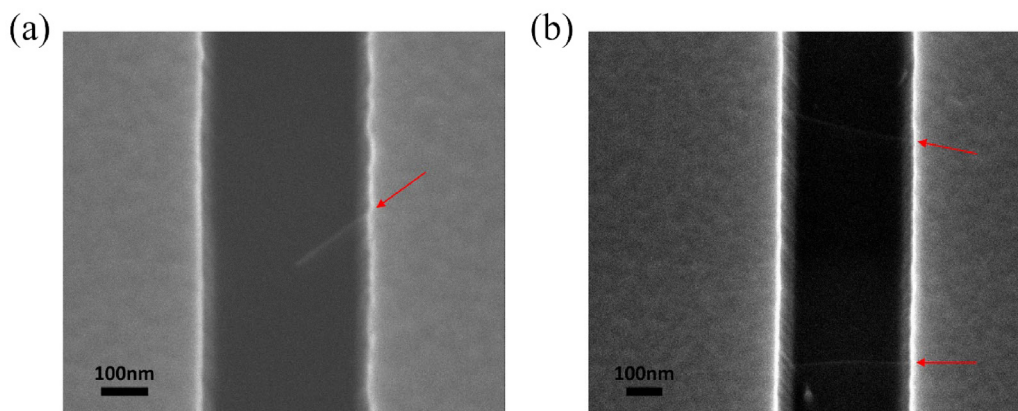


Figure S7 SEM micrographs of the two SWCNT devices considered in the manuscript. These images were taken after the measurements. (a) SEM micrograph of the device with MoRe leads. This device broke down in the measurements and only one SWCNT was found in the source-drain trench of this device. (b) SEM image of the device with MoRe/Pd leads. This image was taken after the measurements and two SWCNTs were found suspended across the source and drain electrodes.

Figure S7 presents SEM micrographs of the two SWCNT devices considered in the manuscript. These images were taken after the measurements. The device with MoRe leads broke down in the measurements and only one SWCNT was found in the source-drain trench of this device. This SWCNT was collapsed, as shown in Fig. S7(a). Two SWCNTs were found bridging the source-drain trench in the device with MoRe/Pd leads, as shown in Fig. S7(b). We did not perform detailed electrical characterization on this device at low temperatures since it was found to sustain rather low supercurrents (~ 350 pA). Therefore, we are not able to conclude if both SWCNTs contributed to the observed supercurrent.

S7 Effect of annealing on the contacts between SWCNTs and MoRe

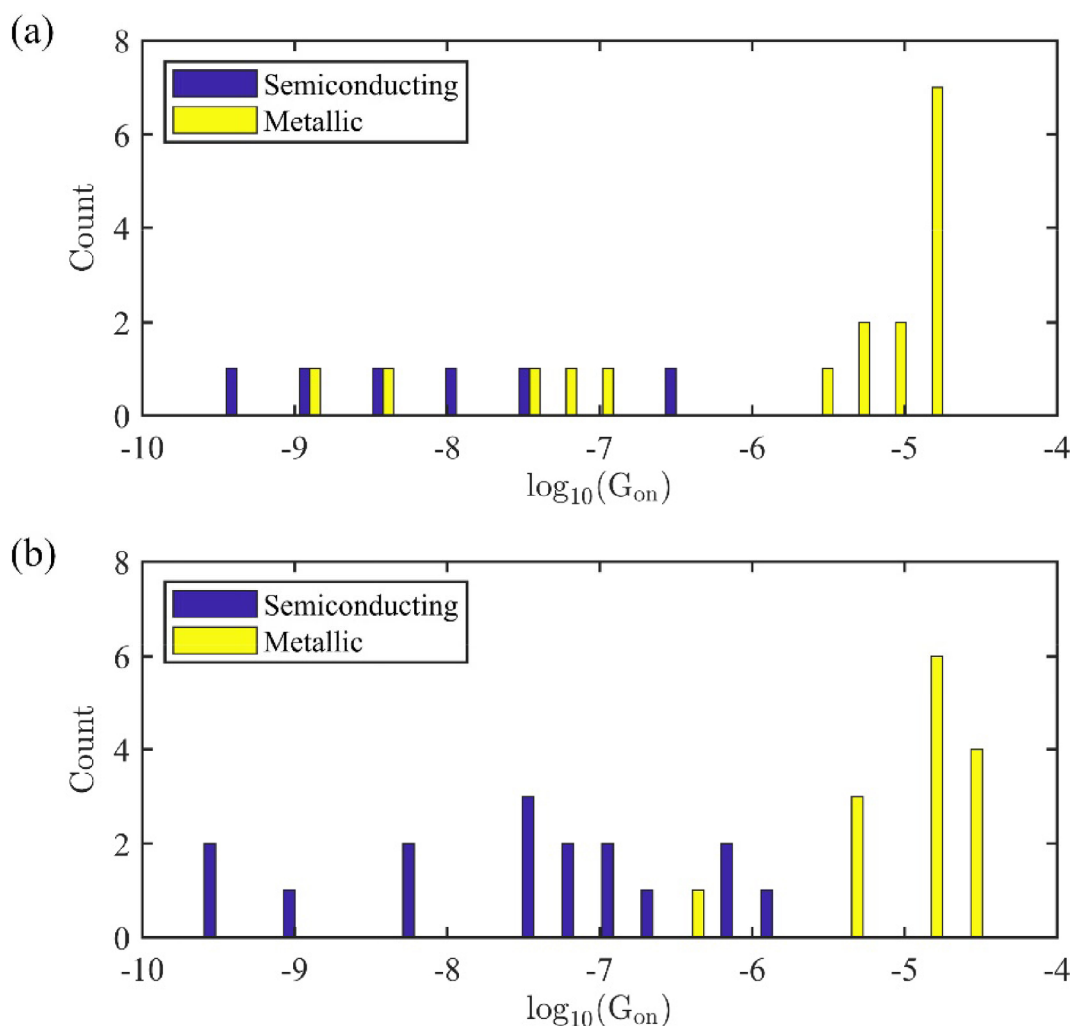


Figure S8 On-state conductance ($V_b = -50$ mV) distribution of the devices on a chip with MoRe leads before (a) and after (b) annealing in vacuum at 900 °C for 10 min. Through annealing, the mean on-state conductance of semiconducting (metallic) devices increased from 0.049 μ S (8.348 μ S) to 0.232 μ S (15.797 μ S), demonstrating the significant positive impact of annealing on the contact between SWCNTs and MoRe. The corresponding increase in the median on-state conductance of semiconducting (metallic) devices was from 0.007 μ S (8.804 μ S) to 0.057 μ S (14.717 μ S).

The samples were annealed in vacuum to improve the contacts between SWCNTs and MoRe electrodes. Figure S8 plots the on-state conductance distribution of the devices on a chip with MoRe leads before (a) and after (b) annealing in vacuum at 900 °C for 10 min. The mean on-state conductance of metallic devices nearly doubled in the annealing process while the mean on-state conductance of semiconducting devices was over four times higher after annealing. Similar results are obtained with annealing time of 5 min, which was the annealing time used for the device considered in the main text of the manuscript.

The number of devices in Figs. S8(a) and S8(b) is slightly different since only devices with on-state current above 10 pA were taken into consideration in the analysis. Through annealing, on-state current of some devices crossed this limit, thereby changing the number of devices included in the analysis. Additionally, annealing created a gate leakage in a few devices so these devices were excluded from the analysis after annealing. Within those devices that were not leaking and had an on-state current above 10 pA before and after annealing, the mean on-state conductance of semiconducting (metallic) devices increased from 0.049 μ S (10.527 μ S) to 0.5493 μ S (11.905 μ S). The corresponding change in the median on-state conductance of semiconducting (metallic) devices was from 0.007 μ S (11.905 μ S) to 0.405 μ S (17.053 μ S).

S8 Effect of annealing on the contacts between SWCNTs and palladium

The devices with a Pd contact layer were annealed at relatively low temperature of 220 °C. To illustrate the positive impact of such low temperature annealing on the contacts between SWCNTs and Pd, Fig. S9 plots the on-state conductance distribution of the devices on a chip with Pd leads before (S9(a)) and after (S9(b)) annealing in air at 200 °C for 120 min. The chip design (1000 pairs of contacts) and the annealing procedure are the same as in reference [S3] and thus, differ from the ones considered in the main text of the manuscript. The results, however, clearly demonstrate that even a relatively low annealing temperature improves contacts between SWCNTs and Pd.

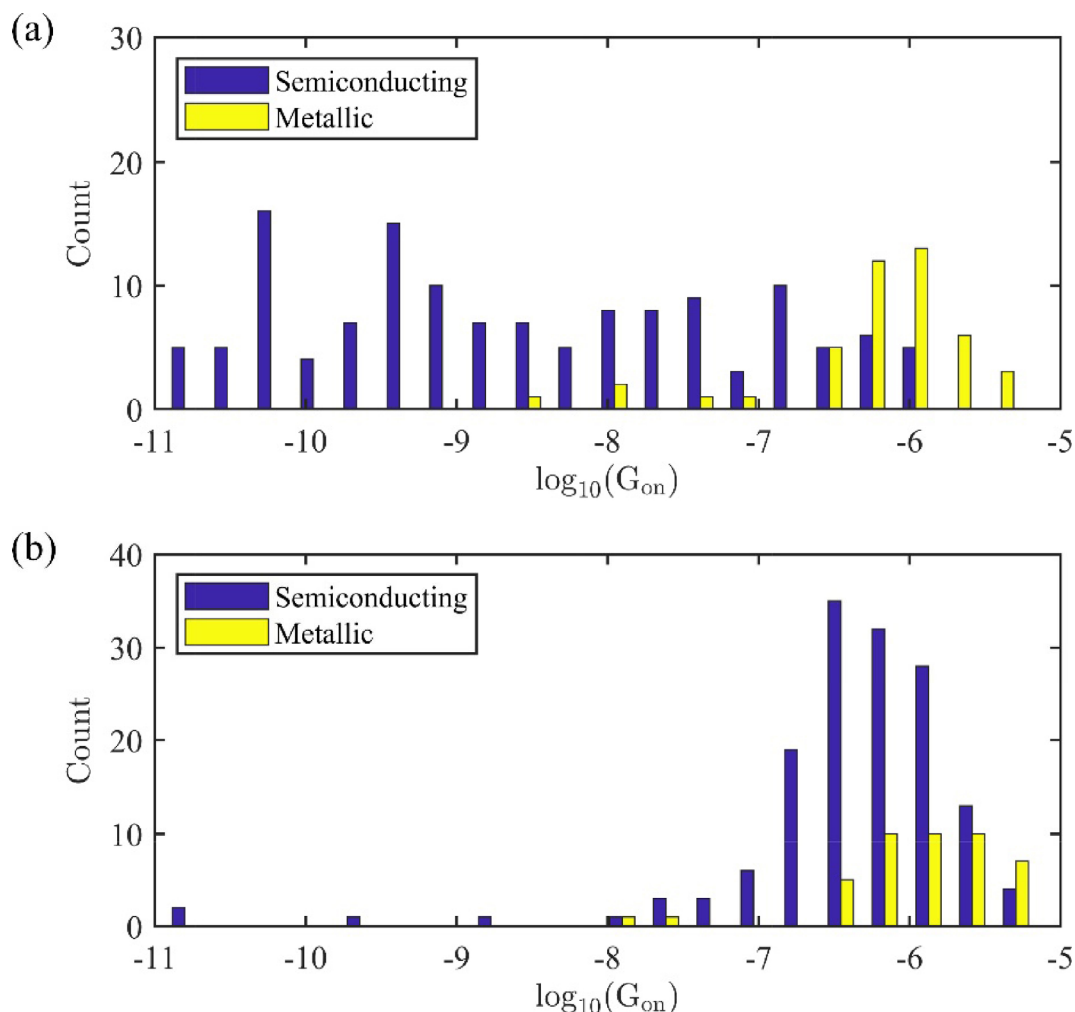


Figure S9 On-state conductance ($V_b = -1V$) distribution of the devices on a chip with Pd leads before (a) and after (b) annealing in air at 200 °C for 120 min. The mean diameter of SWCNTs on this chip is 1.2 nm. Through annealing, the mean on-state conductance of semiconducting (metallic) devices increased from 0.094 μS (1.105 μS) to 0.836 μS (1.888 μS), demonstrating the significant positive impact of annealing on the contact between SWCNTs and Pd. The corresponding change in the median on-state conductance of semiconducting (metallic) devices was from 0.002 μS (0.804 μS) to 0.524 μS (1.283 μS)

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