Supplementary Information

High performance Si-MoS_2 heterogeneous embedded DRAM

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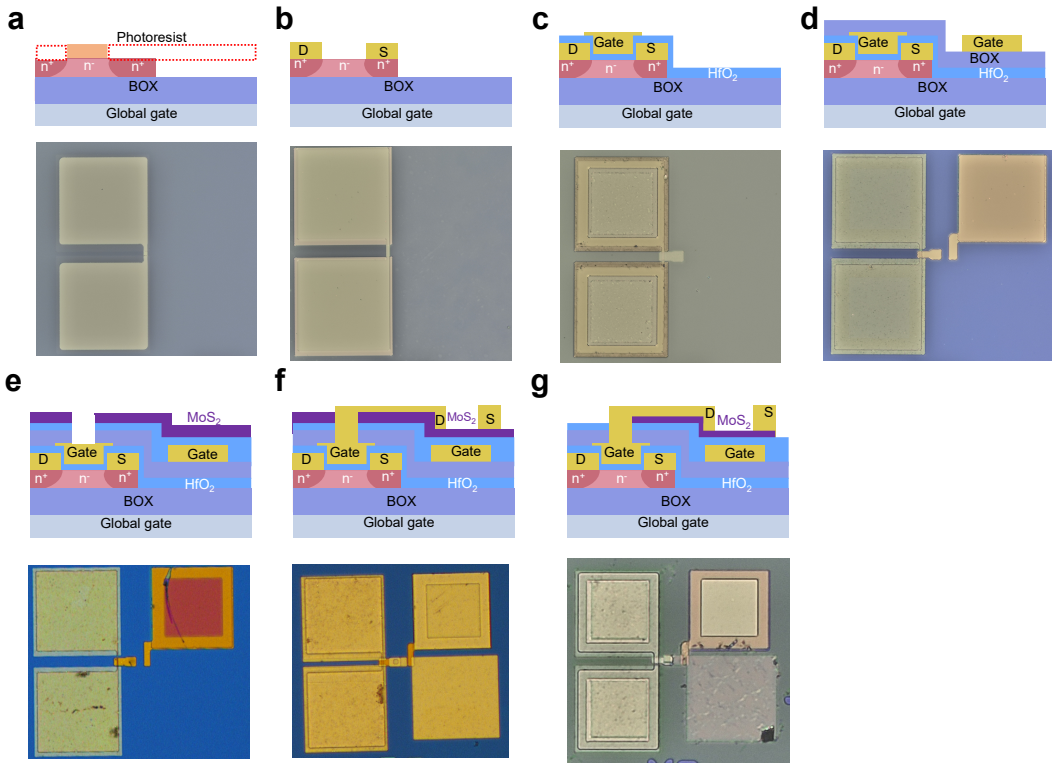
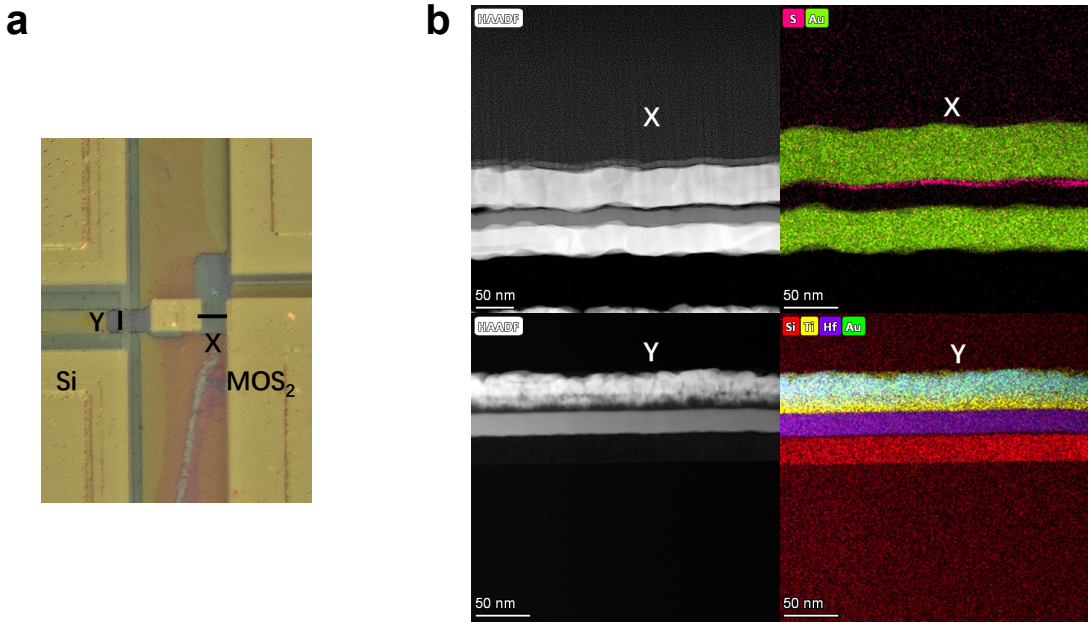


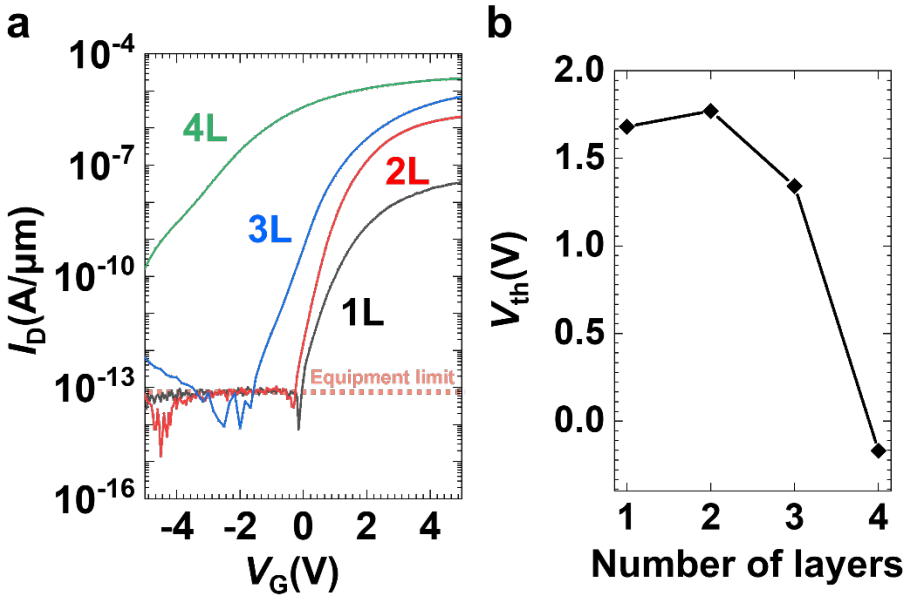
Supplementary Figure 1. Fabrication flow of the 3D interconnection 2T-eDRAM. **a.** Definition of active region and ion-implantation. **b.** Metal deposition to form source/drain of Si-FET. **c.** Deposition of gate dielectric and gate electrode of Si-FET. **d.** Dielectric insulating layer deposition and metal deposition to form the gate electrode as MoS_2-FET. **e.** Second dielectric deposition to form gate dielectric of MoS_2-FET, the transfer of bilayer MoS_2 on the top of the second dielectric and etching of the dielectric between the sources of MoS_2-FET and gate of Si-FET by SF_6. **f.** Metal deposition to form the source/drain of MoS_2-FET and the interconnections of the upper and lower transistors. **g.** Etching of the unnecessary MoS_2 by CF_4.

Supplementary Note 1. Detailed fabrication processes of Si-MoS_2 2T-eDRAM.

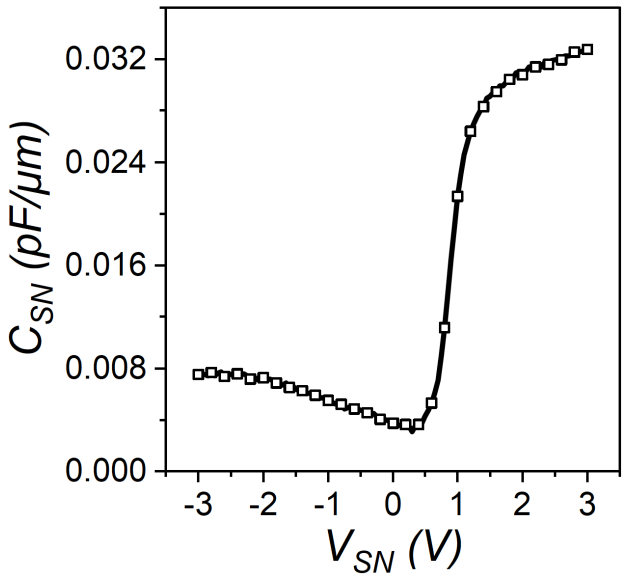
Supplementary Figure 1 shows the fabrication process scheme for the 2T-eDRAM. Firstly, to fabricate the first layer Si-based read transistor, selective photolithography and wet-etching were performed to define the active region and channel. Then, ion-implantation of P (Energy: 10 keV, Dose: 10^{15} cm^{-2}) was carried out to form heavily n-type doping in the active region, while the channel Si is lightly n-type doping (concentration: 10^{15} cm^{-3}), followed by rapid-thermal anneal at 950 °C for activation. As shown in Supplementary Figure 1a, the dashed box in the schematic image illustrates the active regions of the Si-FET. After that, photolithography and electron beam evaporation (EBE) were employed to form the metal contacts (Ti/Au: 5 nm/45 nm) on active region, as shown in Supplementary Figure 1b. The rapid-thermal anneal at 350 °C for 5 min was also used to improve the quality of contact. Secondly, to construct the read transistor gate, ALD-grown 18 nm thick HfO_2 was deposited on the as-fabricated SOI-FET as high-k dielectric , then photolithography and EBE were utilized to form the gate (Au: 50 nm), as illustrated in Supplementary Figure 1c. Thirdly, 80 nm SiO_2 was deposited by Plasma-Enhanced Chemical Vapor Deposition (PECVD) as a dielectric insulating layer, on which 50 nm Au was grown by EBE as the bottom gate of the writing transistor, as shown in Supplementary Figure 1d. A 20 nm HfO_2 was grown with ALD as the gate oxide layer of the write transistor, on which a bilayer of Chemical Vapor Deposition (CVD) MoS_2 was then stacked and transferred as the channel material of write transistor, and the interconnecting vias of the top and bottom transistors were etched using selective photolithography and dry etching as shown in Supplementary Figure 1e. Then, the source-drain metal contacts of MoS_2 and the interconnections of the upper and lower transistors (120 nm Au) were formed using photolithography and EBE. In particular, as shown in Supplementary Figure 1f. Lastly, photolithography and ICP etching (CF_4) were employed to remove the unnecessary MoS_2 to define the channel of nFET, as shown in Supplementary Figure 1g.



Supplementary Figure 2. Cross-sectional TEM image and the corresponding energy dispersive spectroscopy (EDS) mapping images at the metal contact region. a. Optical microscope image of the 2T-eDRAM at low magnification. **b**. Magnified image of TEM of MoS_2 read transistor in x-direction with Si write transistor in y-direction cross-section and EDS spectra of each element, the EDS spectra nicely demonstrate the 3D stacked structure of the device that we have successfully fabricated.



Supplementary Figure 3. Electrical performance of the transferred monolayer to few-layer MoS_2 FETs. a. Transfer characteristics of the 1L-4L MoS_2 FETs at a bias voltage of 1 V. **b.** The extracted V_{th} as a function of the number of MoS_2 layers. When the number of MoS_2 layers increases monotonically from monolayer (1L) to four layers (4L), the MoS_2 FET exhibits gradually increasing field-effect mobility and on-state current, as well as a negatively shifted V_{th}, which may be attributed to the current carrying increase in carrier concentration and plasma etching of isolation channels[1, 2].



Supplementary Figure 4. The measured CV curve of SN node.

Supplementary Note 2. The deviation of I_{OFF} of the write transistor.

Considering the common issue of measurement limitation, calculating the OFF current through retention time and storage capacitance is widely used in memory researches[3, 4, 5]. For capacitor discharge, the variation of stored charge and V_{SN} with time follows equation (1) and (2):

$$Q_{SN}(t) = Q_{SN}(0) - \int_0^t I_{OFF} dt \tag{1}$$

$$V_{SN}(t) = \frac{Q_{SN}(t)}{C_{SN}} = V_{SN}(0) - \frac{1}{C_{SN}} \int_0^t I_{OFF} dt \tag{2}$$

$$I_{OFF}(t) = \frac{dQ_{SN}(t)}{dt} = \frac{C_{SN} \times dV_{SN}(t)}{dt} \tag{3}$$

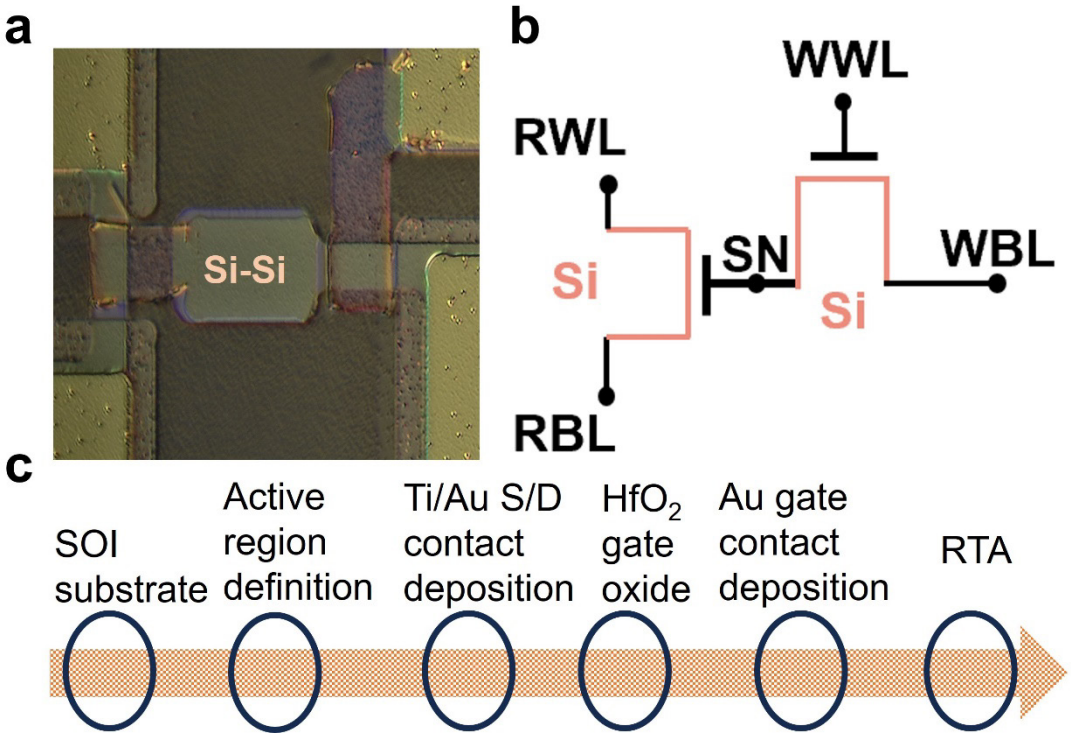
To simplify calculations, I_{OFF} is assumed to remain constant. As retention time is defined as the duration during which the storage node voltage drops by 0.1V, the I_{OFF} can be calculated using equation (4):

$$I_{OFF} = \frac{Q_{SN}(0) - Q_{SN}(t_{ret})}{t_{ret}} = \frac{C_{SN} \times [V_{SN}(0) - V_{SN}(t_{ret})]}{t_{ret}} = \frac{C_{SN} \times 0.1V}{t_{ret}} \tag{4}$$

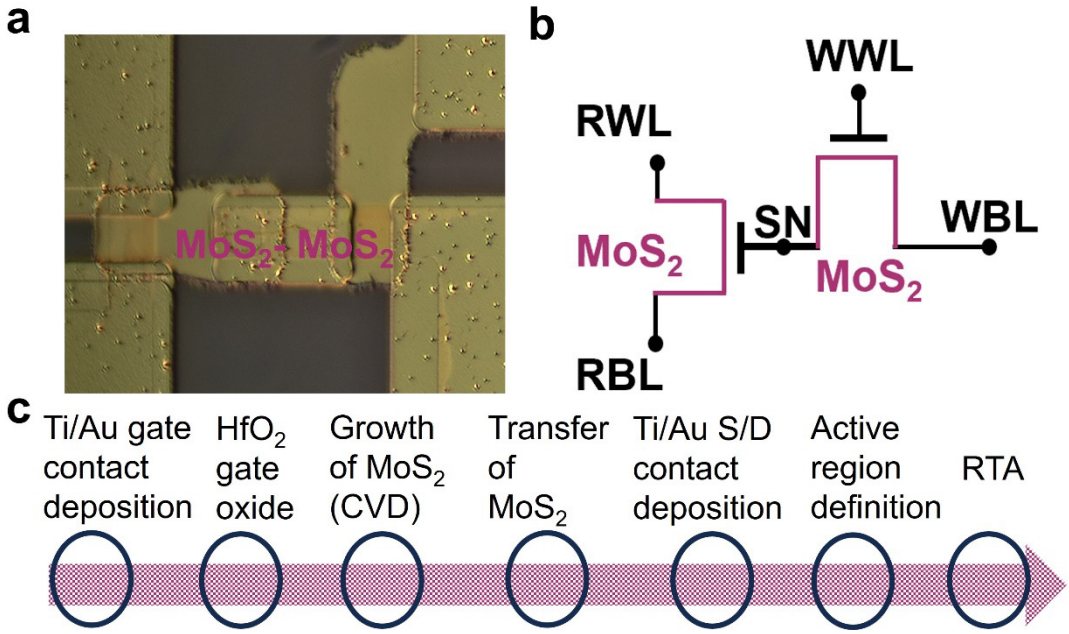
Supplementary Figure 4 demonstrates the measured CV curve of the storage node. The curve exhibits the standard characteristic of MIS CV testing at high frequencies, where $V_{SN} < 0$ indicates depletion capacitance and $V_{SN} > 0$ indicates accumulation capacitance, i.e., gate capacitance. With a measured gate capacitance of 0.032pF/μm, the I_{OFF} can be calculated using equation (5) and (6).

$$I_{OFF(2L)} = \frac{C_{SN} \times 0.1V}{t_{ret}} = \frac{0.032pF/\mu m \times 0.1V}{1000s} = 3.2 \times 10^{-18} A/\mu m \tag{5}$$

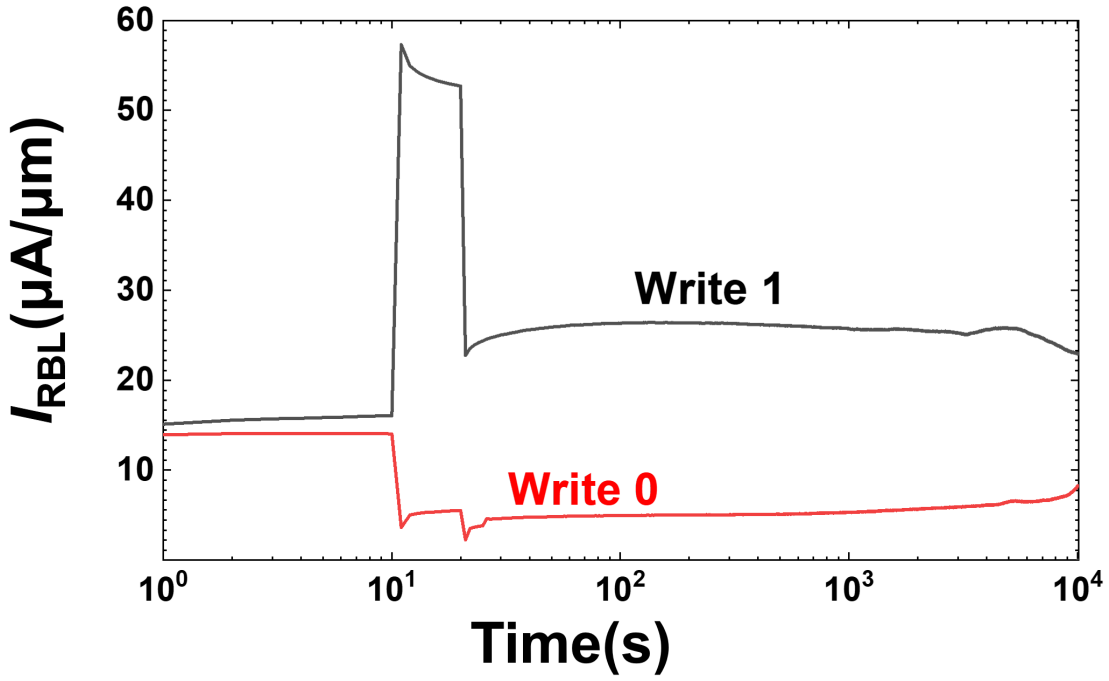
$$I_{OFF(1L)} = \frac{C_{SN} \times 0.1V}{t_{ret}} = \frac{0.032pF/\mu m \times 0.1V}{6000s} = 5.3 \times 10^{-19} A/\mu m \tag{6}$$



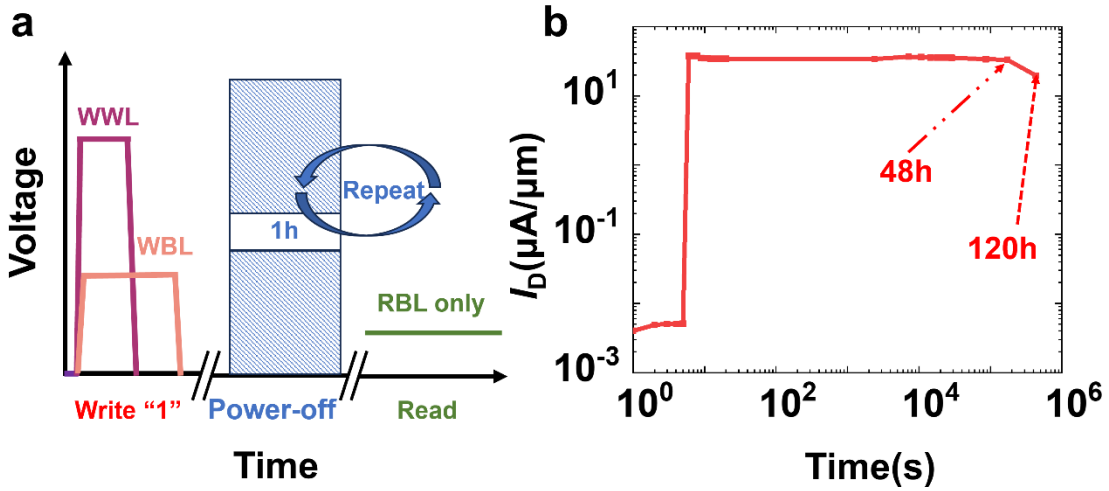
Supplementary Figure 5. Si-Si 2T-eDRAM device and process flow diagram. a. Optical image of Si-Si 2T-eDRAM. **b.** The corresponding equivalent circuit diagram. **c**. The process flow diagram of Si-Si 2T-eDRAM.



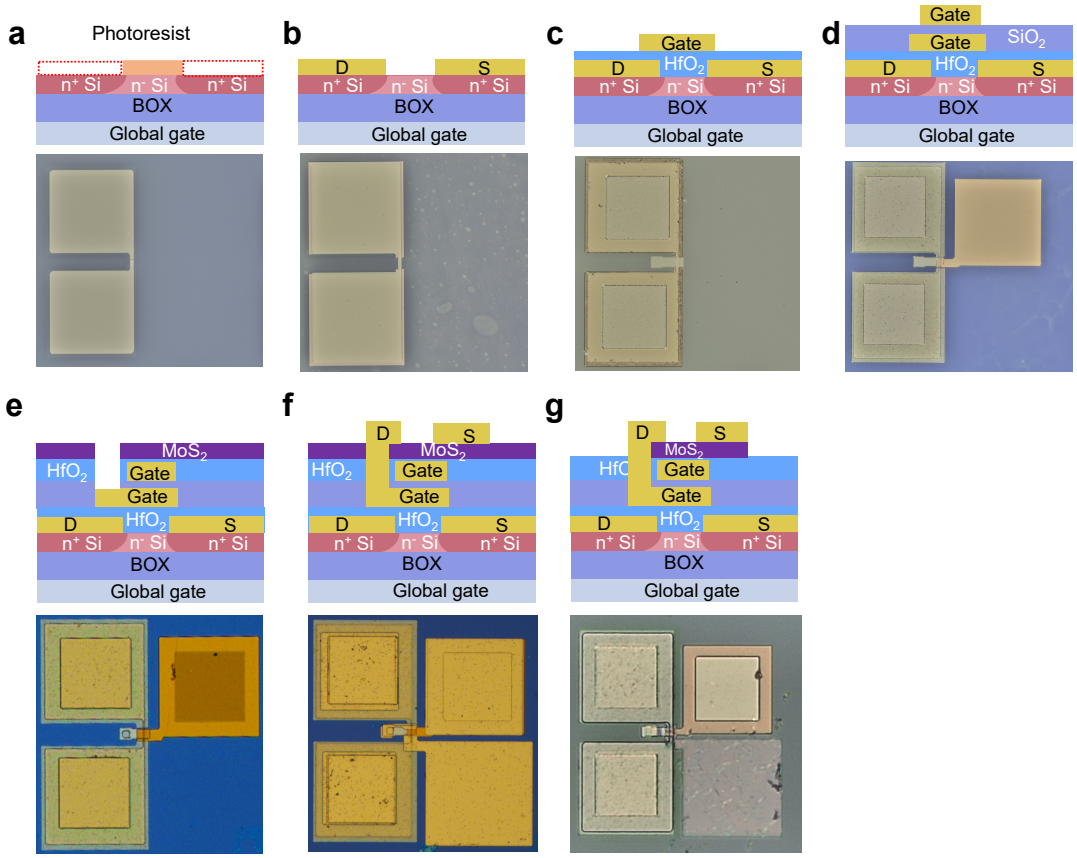
Supplementary Figure 6. MoS_2-MoS_2 2T-eDRAM device and process flow diagram. a. Optical image of MoS_2-MoS_2 2T-eDRAM. **b.** The corresponding equivalent circuit diagram. **c**. The process flow diagram of MoS_2-MoS_2 2T-eDRAM.



Supplementary Figure 7. Advantages of Si-1L MoS_2 2T-eDRAM in terms of long retention time. The output current of DRAM cell as the function of measurement time at V_{hold} = 0 V.



Supplementary Figure 8. Si-MoS_2 2T-eDRAM ultra-long-term retention under power interruption. a. Time diagram schematic for repeated measurements. During the read operation, only the RBL terminal is biased at 1V after each 1 h powerless cycle. **b.** I_{RBL} of Si-MoS_2 DRAM cell measured at the end of each powerless cycle for up to 120 h.

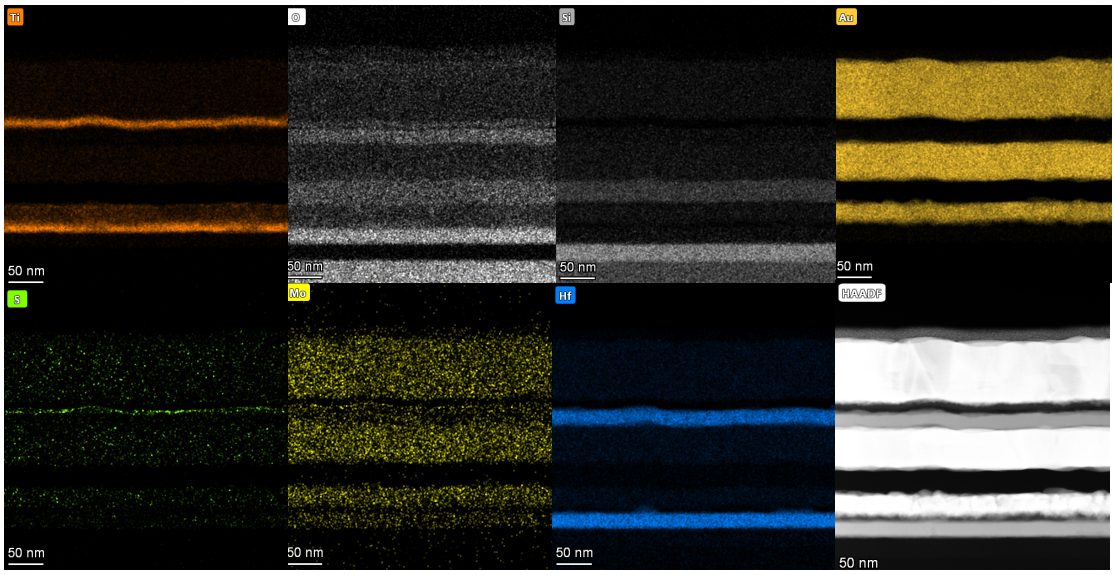


Supplementary Figure 9. Fabrication flow of the 3D vertically stacking 2T-eDRAM. a. Definition of active region and ion-implantation. **b.** Metal deposition to form source/drain of Si-FET. **c.** Deposition of gate dielectric and gate electrode of Si-FET. **d.** Dielectric insulating layer deposition and metal deposition to form the gate electrode as MoS_2-FET. **e.** Second dielectric deposition to form gate dielectric of MoS_2-FET, the transfer of bilayer MoS_2 on the top of the second dielectric and etching of the dielectric between the sources of MoS_2-FET and gate of Si-FET by SF_6. **f.** Metal deposition to form the source/drain of MoS_2-FET and the interconnections of the upper and lower transistors. **g.** Etching of the unnecessary MoS_2 by CF_4.

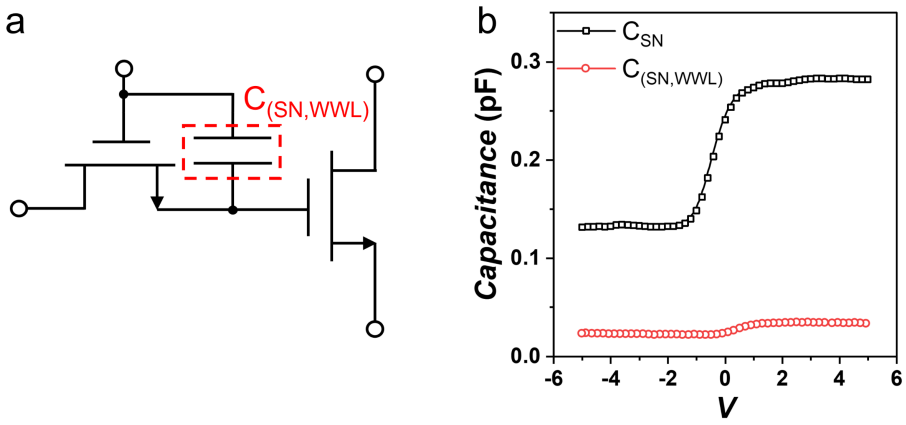
Supplementary Note 3. Detailed fabrication processes of Si-MoS_2 vertically 2T-eDRAM.

Supplementary Figure 9 shows the fabrication process scheme for the 3D vertically stacking 2T-eDRAM. Firstly, to fabricate the first layer Si-based read transistor, selective photolithography and wet-etching were performed to define the active region and channel. Then, ion-implantation of P (Energy: 10 KeV, Dose: 10^{15} cm^{-2}) was carried out to form heavily n-type doping in the active region, while the channel Si is lightly n-type doping (concentration: 10^{15} cm^{-3}), followed by rapid-thermal anneal at 980 °C to activation. As shown in Supplementary Figure 9a, the dashed box in the schematic image illustrates the active regions of the Si-FET. After that, photolithography and EBE were employed to form the metal contacts (Ti/Au: 5 nm/45 nm) on active region, as shown in Supplementary Figure 9b. The rapid-thermal anneal at 350 °C for 5 min was also used to improve the quality of contact. Secondly, to construct the read transistor gate, ALD-grown 18 nm thick HfO_2 was deposited on the as-fabricated nFET as high-k dielectric, then photolithography and EBE were utilized to form the gate (Au: 50nm), as illustrated in Supplementary Figure 9c. Thirdly, 80 nm SiO_2 was deposited by PECVD as the dielectric insulating layer, and 50 nm Au was grown by EBE in the vertical direction as the bottom gate of the writing transistor, as shown in Supplementary Figure 9d. A 20 nm HfO_2 was grown with ALD as the gate oxide layer of the write transistor, and a bilayer of CVD MoS_2 was then stacked and transferred as channel material, and the interconnecting vias of the top and bottom transistors were etched using selective photolithography and dry etching as shown in Supplementary Figure 9e. Then, the source-drain metal contacts of MoS_2 and the interconnections of the upper and lower transistors (120 nm Au) were formed using photolithography and EBE. In particular, as shown in Supplementary Figure 9f.

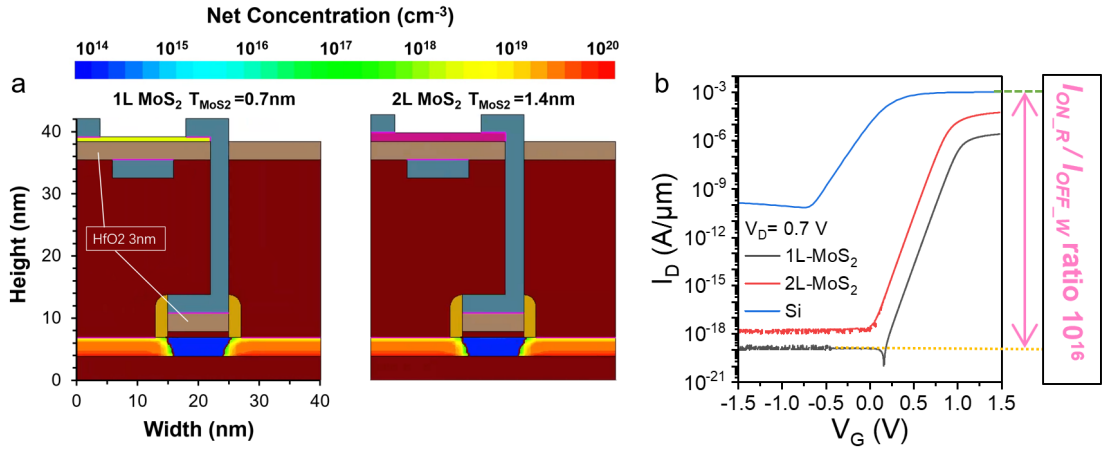
Lastly, photolithography and ICP etching (CF_4) were employed to remove the unnecessary MoS_2 to define the channel of wirte transistor as shown in Supplementary Figure 9g.



Supplementary Figure 10. The EDS mapping images of the Si-MoS_2 vertical stacked 2T-eDRAM.



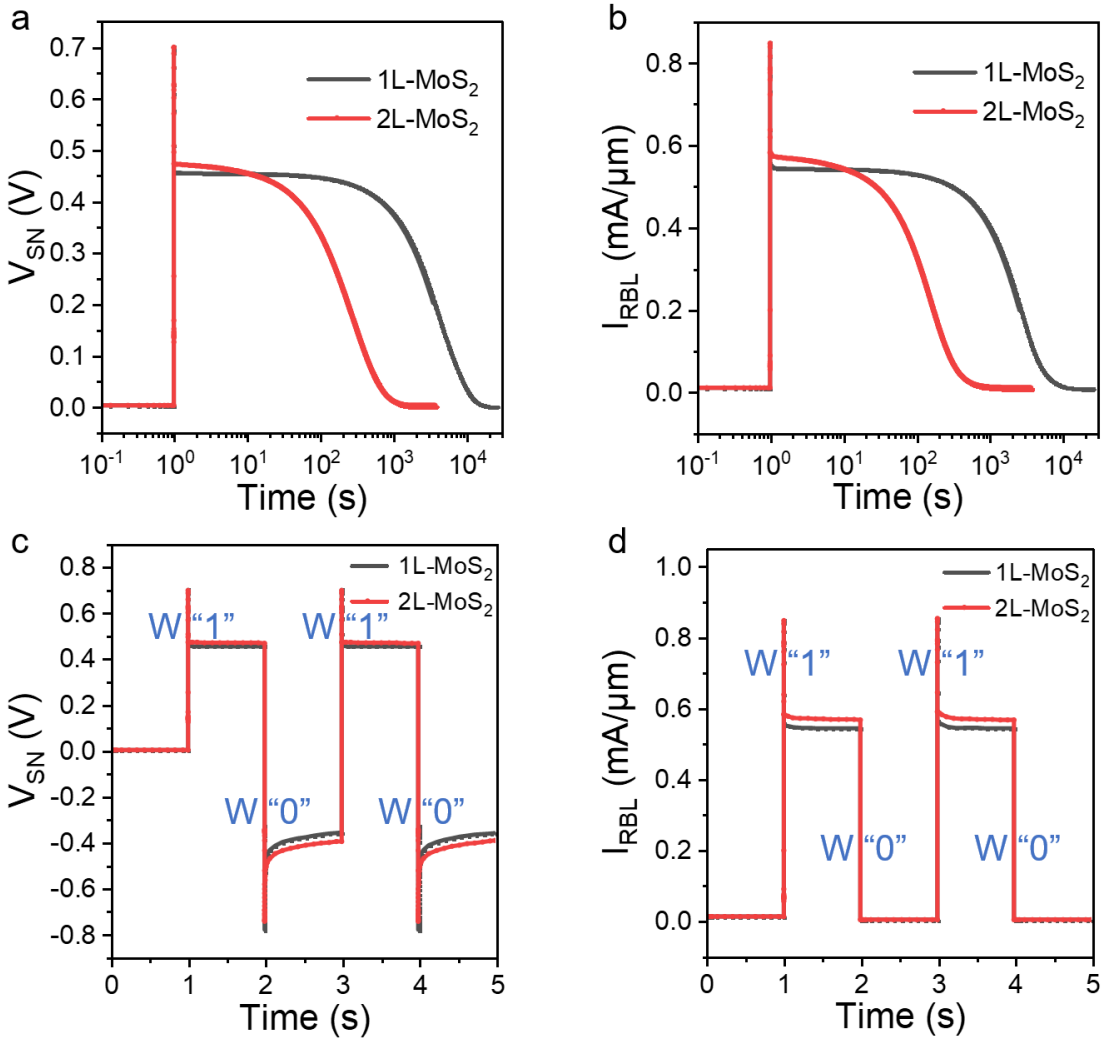
Supplementary Figure 11. The storage capacitance and parasitic capacitance of SN node for vertical stacked 2T-eDRAM. a. schematic diagram of parasitic capacitance. **b.** The measured CV curve of SN node and parasitic capacitance.



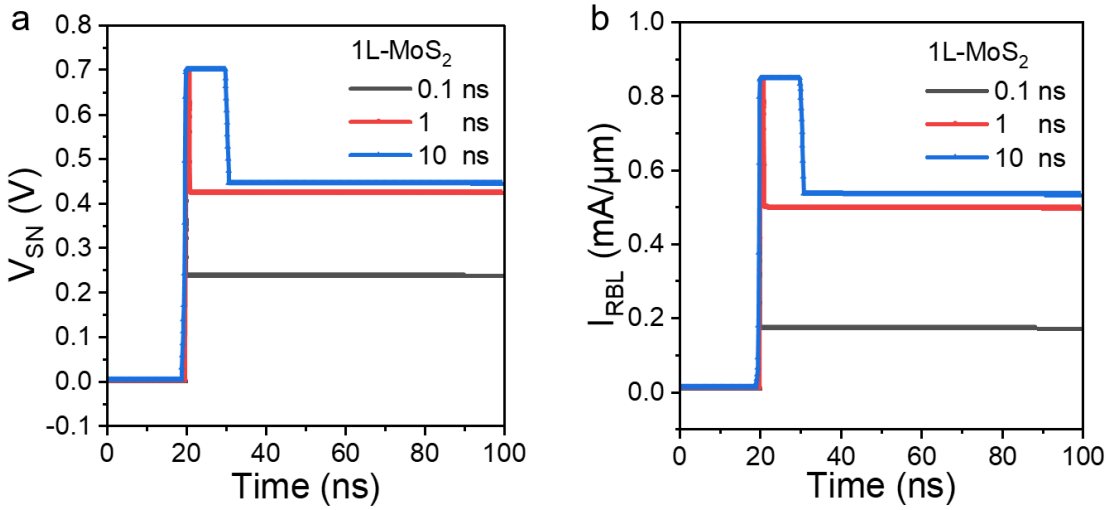
Supplementary Figure 12. TCAD simulation results of the Si/MoS_2 FETs. a. Simulated structure of the 10 nm gate-length Si-MoS_2 2T-eDRAM. **b.** The simulated transfer curves of the MoS_2 /Si nFET at same V_D = 0.7 V.

Sentaurus TCAD simulation is performed to demonstrate the scaling capability of our Si-1L MoS_2 / Si-2L MoS_2 2T-eDRAM device. As shown in Supplementary Figure 12a, the gate-length is defined as 10 nm according to the definition of 1 nm technology node. The thickness of each layer is indicated in the structure, in which the thicknesses of 1L MoS_2, 2L MoS_2 and Si are fixed as 0.7 nm, 1.4 nm and 3 nm, respectively, and the gate-dielectric is 3 nm HfO_2. The mobility of MoS_2 nFET and Si nFET are all 150 $cm^2\ V^{-1}\ s^{-1}$, according to the literature reported values[6, 7, 8] of the advanced MoS_2 write transistor and Si read transistor. Quantum confinement model is used in the simulation due to the ultra-thin films.

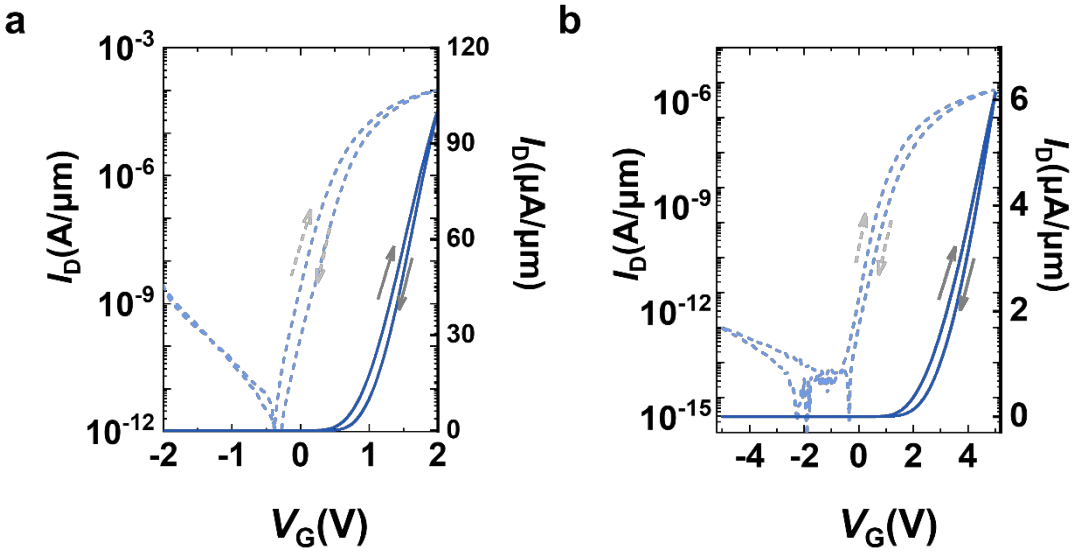
The simulated I_D-V_G curve in Supplementary Figure 12b shows large switching current ratio, right threshold voltage of the write transistor MoS_2, low off-current of the write transistor and high on-current of the read transistor, meeting the industrial requirements of 1 nm technology nodes according to the 2023 IEEE International Roadmap for Devices and Systems (IRDS). Furthermore, the simulated I_D-V_G curve also demonstrates the excellent capability in matching the read transistor sense margin to the write transistor channel material drive current to read and write speeds.



Supplementary Figure 13. TCAD simulation results of the Si-MoS_2 2T-eDRAM. **a**. V_{SN} -Time characteristics and **b.** I_{RBL} -Time characteristic after writing "1" (V_{WBL}=0.7 V) of the simulated 2T-eDRAM. **c.** V_{SN} and **d.** I_{RBL} waveforms in "Write 1-Read 1-Write 0-Read 0" Timing sequence.



Supplementary Figure 14. TCAD simulation results for Si-1L MoS_2 2T-eDRAM in various write pulse width. a. The storage node voltage variation and **b.** output current variation under 0.1ns-10ns writing 1 pulse width.



Supplementary Figure 15. Hysteresis and trap density of a. Si read transistor and b. 2L-MoS_2 write transistor. The dual-sweep I_D-V_G transfer characteristics were measured at V_D = 1V. Solid lines correspond to linear scale and dashed lines correspond to log scale. The arrows indicate the scanning directions.

The hysteresis and the trap density are very important for 2T-eDRAM operation and strongly related with the gate oxide process. The hysteresis of the Si read transistors is around 0.13 V, the hysteresis of the MoS_2 write transistors is around 0.27 V This means that the influence of the floating grid effect is weak.

The trap density (N_T) can be extracted from the following equation[9]:

$$N_T = \frac{\Delta V_{TH} \cdot C_{OX}}{q}$$

where ΔV_{TH} (0.17 V) is the difference of the threshold voltage (V_{TH}) during the forward and backward sweep. $q \approx 1.6 \times 10^{-19}$ C is the elementary charge. $C_{OX} = \varepsilon_0 \varepsilon_r / d$ is the oxide capacitance per unit area, in which $\varepsilon_0 \approx 8.85 \times 10^{-14}$ F/cm is the vacuum permittivity, ε_r = 17.4 is the experimentally measured permittivity of HfO_2 gate dielectric[10], d = 20 nm is the thickness of the HfO_2 gate dielectric.

As a result, C_{OX} is calculated to be about 7.7×10^{-7} F/cm^2, and the Si trap density (N_T) is estimated to be 6.2×10^{11} cm^{-2}and the MoS_2 trap density (N_T) is estimated to be 12.9×10^{11} cm^{-2}.

Supplementary Table 1

Summarizes of The Major Parameters of Other Typical Related Work

Reference	2016[11]	2016[12]		2021[13]		2008[14]	2020[15]	2023[5]	2022[3]	2023[16]	2023[17]	This Work	
Structure	1T1C	1T1C	2T0C	1T1C	2T1C	2T0C	2T0C	2T0C	2T0C	Stacked 2T0C	Stacked 2T0C	Planer 2T0C	Stacked 2T0C
Material	Si	MoS_2		MoS_2		Si	IWO	ITO	IGZO	IGZO	IGZO	Si- MoS_2	
Write pulse width	8.75ns	0.2ms	-	20ms	140ms	8ns	3ns (simulation)	100 ns	10ns	-	5ns	5ns/1ns(simulation)	
Retention time	64ms	>251ms	>1s	>10s	>100s	~5us	1-10s	2250 s	>7000s	20s	75s	1000s(2L) 6000s(1L)	>1000s/ 65s(simulation)
$I_{OFF\ W}$ (A/μm)	-	10^{-15}-10^{-18}		$<10^{-13}$			10^{-15}	4×10^{-19}	$<6\times10^{-20}$	-	$<10^{-13}$	3.2×10^{-18}(2L), 5.3×10^{-19}(1L)	
$I_{ON\ W}$ (A/μm)	-	10^{-6}		10^{-7}-10^{-8}		-	10^{-4}	22.6×10^{-6}	24×10^{-6}	-	10^{-5}– 10^{-6}	6.31×10^{-6}	
$I_{ON\ R}$ (A/μm)												166×10^{-6}	
Sense margin (μA/μm)	-	-		-	<0.01	-	-	-	~27		≤10	35	20
Additional lithography	-	-		-	-	-	1	-	-	4	4	4	
Compatibility	-	BEOL		BEOL		CMOS	BEOL	BEOL	BEOL	BEOL	BEOL	BEOL	
Feature size	1x (19-17nm) $6F^2$	0.5μm		20μm		50nm	50nm	50nm	70nm	75nm $4F^2$	65nm $4F^2$	3μm (10nm in simulation) $4F^2$ for stacked 2T0C	

"-" represents that the data is not available.

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