nature portfolio

Peer Review File

High performance Si-MoS2 heterogeneous embedded DRAM

REVIEWER COMMENTS

Reviewer #1 (Remarks to the Author):

Comments:

The manuscript titled "High Performance Si-MoS2 Heterogeneous Embedded DRAM," authored by Kai Xiao et al., presents a hybrid eDRAM comprising a Si FET and MoS2 FET. The paper follows a structured format, including device introduction, material characterizations (Raman, SEM, and STEM), eDRAM measurements (transfer curves and retentions), and verification of device mechanism with a band diagram. However, there are numerous typos and mistakes throughout the manuscript. Before proceeding with publication, detailed suggestions/comments are recommended to enhance the article's quality.

1. At Line 128 in Page 5, the authors claim the developed Si- MoS2 eDRAMs have longer retentions and the sense margin than that consisting of only either Si or MoS2. To facilitate a comprehensive comparison, it would be beneficial for the authors to include references related to all-Si and all-MoS2-based eDRAMs. This would offer readers a broader understanding of the advancements and limitations in both approaches, providing valuable context for the hybrid Si-MoS2 eDRAM presented in the manuscript.

2. Please clarify if each STEM image in the paper was acquired in the bright-field or dark-field mode, for which question the referee believes that the latter is the case. Regarding STEM, another issue here is that the ADF-STEM image in Fig. 1g is not clear enough to prove the authors' claim on bilayer MoS2 channel. The authors might provide clearer atomic-resolution STEM images or deterministic proofs other than the peak separation between two Raman characteristic peaks, given that Raman spectra are not conclusive enough to deduce the layer number of 2D materials.

3. The referee suggests that the reason(s) that bilayer MoS2 was chosen to make 2T-eDRAM should be put more explicitly. For instance, at Line 193 in Page 8, there is a sentence saying "to optimize the compromise between data retention and write speed of the eDRAM…". Is this statement based on Supplementary Fig. 3? The referee's inference is that the compromise is related to the Vth shift. In any case, a detailed explanation should be added to help readers to get the reason of using bilayer MoS2 immediately.

4. Line 221 in Page 9, the switch ratio between the ON current of the reading FET (~270uA~10^-4A) and the OFF current (10^-13A) of the writing FET is about 10^9 or 10^10. Why do authors claim 10^14 in Fig. 2c?

5. The authors attribute the improvement of sense margin and retention to the higher ON current held by the Si FET and lower leakages via the MoS2 FET, for which is intuitive but reasonable. The referee inquires whether the authors referenced any formula or model to correlate the sense margin with the ON current. This correlation would provide additional validation for the selling point presented in their

experimental observations.

6. In Figure 3a, why does high current with logic “1” drop sharply at 1000 s? Please clarify it.

7. In Figure 3d, the referee requests clarification regarding the formula presented. The referees are unsure how to interpret the value of 3.9 x 10^-18 and please seek a definition or description to aid reader’s understanding.

8. The referee notes a discrepancy between the schematics and cross-sectional SEM image in Figures 4d and 4e, highlighting a lack of alignment between the two representations. Revise it.

9. How many devices were fabricated? It is worth to note the reliability and reproducibility of the proposed fabricated process.

10. Considering state-of-the-art non-volatile memories, a retention of 6000 seconds cannot be considered extremely long. Please avoid using “extremely” and its synonyms.

11. Fig. 4a somewhat looks like a band structure under a negative gate voltage, which would be contradictory to the zero hold bias as claimed. To prevent misunderstanding, the band structure should be refined to reflect the real case in the proposed MoS2 device. In addition, the definition/notation of leakage in the paper is not the same with that has been commonly used for field-effect transistors, where leakage is nominally referred to the current through the gate and drain terminals. This is something that needs to be noted in the paper.

12. The developed process was claimed to be a BEOL-compatible process. Through detailed literature searching, the referee found that in terms of 3D integration of 2D materials and Si technology, some manufacturing processes were recently reported and also appear to be promising like the one presented in the paper. For instance, [S. X. Guan, et al. npj 2D Mater. Appli. 2023, 7, 9] or [J. H. Kang, et al. Nat. Mater. 2023, 22, 1470-1477], to name a few. It would be great to involve a discussion about the technological merits between the current work and parallel research works.

Typos and Minor comments:

1. At Line 176 in Page 7, there is a typo in the sentence, directly quoted “Figure 1c exhibit three characteristic peaks of MoS2:”, though the presented spectra show only two peaks. Please correct the number of the Raman peaks.

2. Kindly remind that the axis titles and units are missing in Supplementary Fig. 3. Fig. 6, Fig. 11 and Fig. 12. These are not professional figures.

3. At Line 226 in Page 9, the authors might have to add relevant references for the simplified model.

4. In what conditions were those devices measured (i.e. vacuum or ambient)? The info should be provided somewhere in the manuscript.

5. At Line 332 in Page 13, The word “heterogeneous” seems not necessary and should be deleted. At 332 in the same page, in “MOS2” the O should be a lower case “o”. Typos and inaccurate grammars are found in many places over the manuscript, which is distracting during reading. It would be helpful to address the paper format more carefully and have a professional editor for proofreading before submitting the revised version.

6. Are Vsn and VSN the same? Please make it consistent if they are the same.

7. Symbols for authors contributed equally (*) and corresponding authors (†) are typos in the notation used in title page.

8. The referee suggests reorganizing Figure 2, 3 and 4, as each figure looks too crowded, making it difficult to distinguish each sub-figure.

In summary, the referee finds that the current version of the paper is not ready for publication due to numerous artificial defects. Suggest that the paper is premature in its current form and recommend further revisions and improvements before considering it for publication in Nature Communications.

Reviewer #2 (Remarks to the Author):

I co-reviewed this manuscript with one of the reviewers who provided the listed reports. This is part of the Nature Communications initiative to facilitate training in peer review and to provide appropriate recognition for Early Career Researchers who co-review manuscripts.

Reviewer #3 (Remarks to the Author):

The proposed research work based on Si-MoS2 heterogenous eDRAM technology promises significant improvements in data retention and integration density.
Further, auhtors have adderssd the challenges such as fabrication complexity, long-term stability, scalability, and compatibility issues practical implementation.
Minor comment:
I some places authors have used Fig and Figure, it would be better to be consistent with terminology.
Also there is need of careful proof reading.

Reviewer #4 (Remarks to the Author):

Please find the comments in the attached document.

Reviewer #5 (Remarks to the Author):

In this paper, the authors demonstrate a 2T gain-cell eDRAM using a hybrid MoS2 write transistor/Si read transistor scheme, leveraging the low off-current of MoS2 FET and the high on-current of Si transistor to achieve long retention and short read time, and demonstrates the potential of 3D stacking for even higher density. The eDRAM exhibits an excellent retention up to 6000 s and sense margin up to 40 μA/μm. Overall, the work is impressive and demonstrates a highly intriguing application of 2D materials for embedded memory, and it should merit publication in Nature Communication eventually. However, there are still several points that the reviewer would like to see the authors revise/clarify before a recommendation could be made:

• In the Introduction, the authors claim that compared with 2D material channel, amorphous oxide semiconductors suffer from low mobility and on-current due to percolation transport when Vth is shifted to the right. However, a recent paper on IEDM 2022 (Qianlan Hu, Qijun Li, Shenwu Zhu, Chengru Gu, Shiyuan Liu, Ru Huang and Yanqing Wu, "Optimized IGZO FETs for Capacitorless DRAM with Retention of 10 ks at RT and 7 ks at 85 °C at Zero Vhold with Sub-10 ns Speed and 3-bit Operation," IEDM 2022, 26.6) demonstrates IGZO FETs for GC-eDRAM with very good performance, including an extremely low off-current of 6e-20 A/μm and a decently high on-current of 24 μA/μm at Vds=1V and Vg=Vth+1V, which is arguably even better than the MoS2 FET in this work. In addition, apart from amorphous oxide semiconductors, there are also demonstrations of crystalline oxide semiconductors such as c-axis-aligned crystalline IGZO (CAAC-IGZO). Therefore, the reviewer suggest the authors tone down the statement, and also include the work mentioned above in the benchmark.

• The authors mentioned in the Introduction "As the size of the transistor scales down, the storage capacitance is reduced and the leakage current of the write transistor increases due to short channel effect (SCE). This significantly degrades the data retention of the GC-eDRAM to the level of microsecond." That said, the authors use very large size transistors (several μm) for their demonstration. Although it's understandable for an experimental prototype, the reviewer suggests the authors project the memory performance with scaled dimensions.

• (Continuing from the comment above) judging from the fact that in Fig. 3g, even the full-Si eDRAM also exhibits a rather long retention of several seconds, it has to be concluded that the long retention time of MoS2-Si hybrid eDRAM can at least be partially attributed to the large gate capacitance of the Si read transistor with a large μm size. If the device dimensions were scaled down to ~10nm, the capacitance (proportional to W*L) would be reduced by ~6-7 orders of magnitude and so would the retention, unless the off-state current can also be scaled accordingly, yet the raw off-current (before width normalization) would only reduce by ~3 orders of magnitude. The reviewer suggestes the authors address the issue by further reducing the off-state current or show a viable path for doing so (the 1L MoS2 in SI seems to be in the right direction, but the on-state performance need serious improvement).

• The long retention and low off-current of 3.9e-18 A/um in Fig. 3d is achieved at V_WWL=-1V, which is also the exact same thing the authors argued against in the Introduction ("Moreover, it is noted that AOS achieves extremely high retention time only when an additional negative holding voltage is applied on the gate of the write transistor to reduce leakage"; and to be fair, some works such as the IEDM 2022 paper mentioned above have already achieved long retention with zero hold voltage, therefore the statement should be revised). The authors should at least discuss viable solutions to shift Vth to more positive voltages to achieve long retention at zero hold voltage (again, the 1L MoS2 in SI seems to be in

the right direction, but the on-state performance need serious improvement).
• Apart from retention and read margin, the authors should also comment on the write performance of the eDRAM.
• A prior work on using MoS2 FET with ultra-low leakage for DRAM application (ACS Nano 2016, 10, 9, 8457–8464) should be included (although it's 1T1C DRAM).
• Scale bars should be given in Figs. 1d-f.

Reviewer #6 (Remarks to the Author):

I co-reviewed this manuscript with one of the reviewers who provided the listed reports. This is part of the Nature Communications initiative to facilitate training in peer review and to provide appropriate recognition for Early Career Researchers who co-review manuscripts.

The authors report on the first demonstration of a heterogenous gain cell embedded DRAM (GC-eDRAM) combining silicon (Si) and molybdenum disulfide (MoS_2) to improve the data retention and integration density of GC-eDRAM.

This is realized in a 3D-integrated BEOL-compatible process, which offers great promise for integrating mixed Si-2D technology for embedded memory.

In particular, the memory behavior reported in this work is impressive and surpasses state-of-the-art reports for eDRAM based on full-Si CMOS, full-2D materials, and oxide semiconductor materials. In particular, the Si-MoS_2 heterogenous eDRAM shows long data retention (up to 6000 s), high sense margin, fast operation (5 ns access time), and 3D integration capability.

Overall, this work is not only of great interest to embedded memory community, but also to the heterogenous Si-2D community, which will be of increasing importance going forward for next-generation high-performance computing and high-bandwidth memory paradigms. Therefore, this work is both timely and impactful

I have the following minor comments. After these minor comments are addressed, I can recommend the manuscript for publication in *Nature Communications.*

Sincerely, Suraj Cheema

Comments

1. ON-OFF and benchmarking (Figure 2). In Fig 2c, it is better to denote "I_{ON}/I_{OFF}" as "I_{ON_R}/I_{OFF_W}"to avoid confusions. Also, based on Figu 1a and 1b, the value of I_{ON_R}/I_{OFF_W} for the DRAM in this work seems it should be around 1e10 (around 100*1e-6 /1e-14) at 1V V_D instead of 1e14. Could the authors clarify where the 1e14 number comes from? If the number is indeed 1e10, then it does not demonstrate much advantage in this metric over the other candidates, and the authors should clarify this.
2. Parasitic and gate capacitance. How large is the parasitic capacitance at the SN node when stacking the MoS_2 transistor on top of the silicon transistor. The authors should provide a quantitative comparison with the gate capacitance of the silicon transistor.
3. Comparison to Si 2T-eDRAM: The authors should please comment on the area and cost (e.g., additional lithography steps) of the heterogeneous 2T-eDRAM, compared with conventional silicon 2T-eDRAM, in a highly integrated case (i.e., without probing pads). [this can be conveyed in the comparison table mentioned in Comment 5].
4. Discussion on 1T1C-eDRAM: The introduction states: "*However, the 1T1C eDRAM needs high pillar capacitor whose fabrication is not compatible with CMOS logic process*[9]*. Thus, it is typically fabricated separately with DRAM process and bonded to the processing unit chip with 2.5D and 3D packaging technology*". There are many examples of integrated 1T1C eDRAM where the trench process is directly fabricated over the CMOS logic, e.g. ref [R1]. So the authors should adjust this critique of 1T-1C and instead mention a different benefit of GC structure over 1T-1C [this benefit can be conveyed in the comparison table mentioned in Comment 5].
5. Comparison Table: To help illustrate the benefits of this eDRAM platform, the authors should prepare a summary table comparing their performance against other emerging eDRAM paradigms. I would suggest some key metrics in the table should include (but not limited to): device structure (e.g. other 2T-eDRAM, some 1T-1C), speed (ns), retention or refresh rate, I_{ON}/I_{OFF} ratio, density or bit cell size (n F^2), channel materials (compare some oxide channels, poly-Si, 2D), and BEOL compatibility.

References

- [R1] Ramaswamy, N. *et al.* NVDRAM: A 32Gb Dual Layer 3D Stacked Non-volatile Ferroelectric Memory with Near-DRAM Performance for Demanding AI Workloads. in *2023 International Electron Devices Meeting (IEDM)* 1–4 (IEEE, 2023). doi:10.1109/IEDM45741.2023.10413848.

Authors' responses to the reviewers' comments

Reviewer #1:

The manuscript titled "High Performance Si-MoS_2 Heterogeneous Embedded DRAM," authored by Kai Xiao et al., presents a hybrid eDRAM comprising a Si FET and MoS_2 FET. The paper follows a structured format, including device introduction, material characterizations (Raman, SEM, and STEM), eDRAM measurements (transfer curves and retentions), and verification of device mechanism with a band diagram. However, there are numerous typos and mistakes throughout the manuscript. Before proceeding with publication, detailed suggestions/comments are recommended to enhance the article's quality.

Response:

We sincerely appreciate the reviewer for thoroughly reviewing our manuscript and providing very positive feedback on our work. Your generous appraisal of our efforts is highly encouraging, and we hope that the global scientific community will acknowledge our contributions. We have carefully revised the manuscript, addressed your comments and improved its readability. The modifications are indicated with red strikethroughs for deletions and yellow highlights for additions in the revised manuscript. We believe that these modifications effectively address all your concerns.

Comment 1:

At Line 128 in Page 5, the authors claim the developed Si- MoS_2 eDRAMs have longer retentions and the sense margin than that consisting of only either Si or MoS_2. To facilitate a comprehensive comparison, it would be beneficial for the authors to include references related to all-Si and all-MoS_2-based eDRAMs.

This would offer readers a broader understanding of the advancements and limitations in both approaches, providing valuable context for the hybrid Si-MoS_2 eDRAM presented in the manuscript.

Response:

We greatly appreciate the reviewer's comments and suggestions. The conclusion of '*longer retentions and higher sense margins of the Si-MoS_2 heterogenous eDRAM compared to full Si and MoS_2 eDRAMs*' is based on our experimental results. We simultaneously fabricated and measured identical-sized all MoS_2 and all Si 2T-eDRAMs, with the experimental results shown in Figure R1 (Figure 3a and g in the revised manuscript). We have revised the description in the last sentence of the second paragraph on page 5 of the revised manuscript to avoid misunderstandings, The updated description is as follows:

'the Si-MoS_2 heterogenous eDRAM shows data retention up to 6000 s and sense margin of 35 μA/μm, which are improved 1000 times and 100 times compared to the simultaneously fabricated full Si and MoS_2 eDRAMs respectively.'

We have also supplemented a benchmark table to compare our heterogeneous 2T-eDRAM with other works, including all-Si, all-MoS_2, and AOS based 2T-eDRAMs, as shown in Table RI (Supplementary Table I in the page S17 in the revised supplementary information).

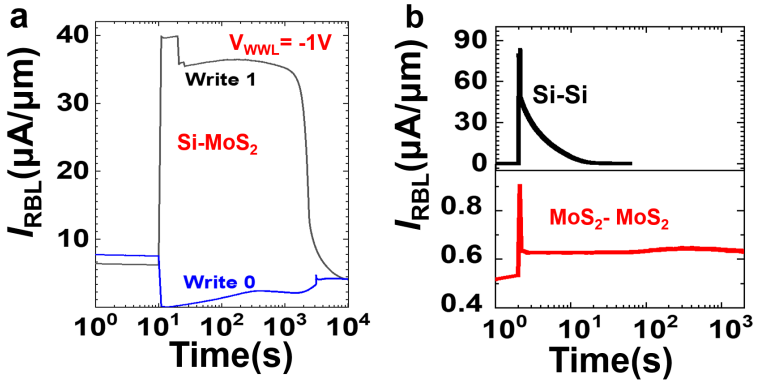

Figure R1 The retention characteristic of **a.** the fabricated heterogeneous Si-MoS_2 2T-eDRAMs and **b.** simultaneously fabricated full Si and full MoS_2 2T-eDRAMs.

TABLE RI

Summarizes of The Major Parameters of Other Typical Related Work

Reference	2016[1]	2016[2]		2021[3]		2008[4]	2020[5]	2023[6]	2022[8]	2023[9]	2023[10]	This Work	
Structure	1T1C	1T1C	2T0C	1T1C	2T1C	2T0C	2T0C	2T0C	2T0C	Stacked 2T0C	Stacked 2T0C	Planer 2T0C	Stacked 2T0C
Material	Si	MoS_2		MoS_2		Si	IWO	ITO	IGZO	IGZO	IGZO	Si- MoS_2	
Write pulse width	8.75ns	0.2ms	-	20ms	140ms	8ns	3ns (simulation)	100 ns	10ns	-	5ns	5ns/1ns(simulation)	
Retention time	64ms	>251ms	>1s	>10s	>100s	~5us	1-10s	2250 s	>7000s	20s	75s	1000s(2L) 6000s(1L)	>1000s/ 65s(simulation)
$I_{OFF\ W}$ (A/μm)	-	10^{-15}-10^{-18}		<10^{-13}			10^{-15}	4×10^{-19}	<6×10^{-20}	-	<10^{-13}	3.2×10^{-18}(2L), 5.3×10^{-19}(1L)	
$I_{ON\ W}$ (A/μm)	-	10^{-6}		10^{-7}-10^{-8}		-	10^{-4}	22.6×10^{-6}	24×10^{-6}	-	10^{-5}– 10^{-6}	6.31×10^{-6}	
$I_{ON\ R}$ (A/μm)												166×10^{-6}	
Sense margin (μA/μm)	-	-		-	<0.01	-	-	-	~27		≤10	35	20
Additional lithography	-	-		-	-	-	1	-	-	4	4	4	
Compatibility	-	BEOL		BEOL		CMOS	BEOL	BEOL	BEOL	BEOL	BEOL	BEOL	
Feature size	1x (19-17nm) $6F^2$	0.5μm		20μm		50nm	50nm	50nm	70nm	75nm $4F^2$	65nm $4F^2$	3μm (10nm in simulation) $4F^2$ for stacked 2T0C	

"-" represents that the data is not available.

Comment 2

Please clarify if each STEM image in the paper was acquired in the bright-field or dark-field mode, for which question the referee believes that the latter is the case. Regarding STEM, another issue here is that the ADF-STEM image in Fig. 1g is not clear enough to prove the authors' claim on bilayer MoS_2 channel. The authors might provide clearer atomic-resolution STEM images or deterministic proofs other than the peak separation between two Raman characteristic peaks, given that Raman spectra are not conclusive enough to deduce the layer number of 2D materials.

Response:

We apologize for the unclear description. All STEM images in the manuscript were acquired in High Angle Annular Dark Field (HAADF) mode, which has been clarified in the revised manuscript. We have supplemented it in the last sentence of the caption for Figure 1 on page 7 in the revised manuscript, as follows:

'All STEM images were acquired in High Angle Annular Dark Field (HAADF) mode.'

Additionally, a clearer resolution STEM image has been included to replace the original Figure 1g to illustrate the bilayer MoS_2 channel, as shown in Figure R2 (Figure 1g in the revised manuscript).

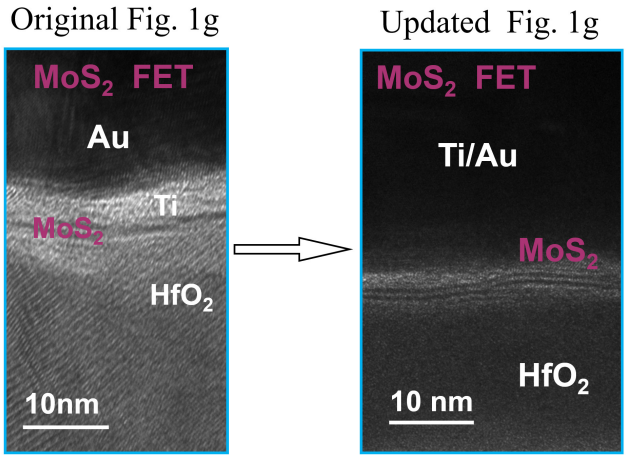

Figure R2. Changes of Figure 1g before (left) and after (right) revision.

Comment 3

The referee suggests that the reason(s) that bilayer MoS_2 was chosen to make 2T-eDRAM should be put more explicitly. For instance, at Line 193 in Page 8, there is a sentence saying "to optimize the compromise between data retention and write speed of the eDRAM…". Is this statement based on Supplementary Fig. 3? The referee's inference is that the compromise is related to the V_{th} shift. In any case, a detailed explanation should be added to help readers to get the reason of using bilayer MoS_2 immediately.

Response:

We appreciate the reviewer's comments and suggestions. The statement of *'to optimize the compromise between data retention and write speed of the eDRAM…'* in the original manuscript is supported by supplementary Figure 3 and related references[11-14]. In DRAM applications, there is a critical need for high speed, long retention time, and low static power consumption, which requires high I_{ON}, low I_{OFF}, and an appropriate V_{th} of the write transistor. Supplementary Figure 3 illustrates that the on-state current of MoS_2 transistors increases with the number of layers of MoS_2, while V_{th} decreases. And for V_G=0V, 1L and 2L MoS_2 transistors remain at a low OFF current level, whereas 3L and 4L exhibit high OFF currents, which will lead to high power consumption in the hold state. Although the variation in off-state current with layer number has not been fully characterized due to measurement limitations, it can be inferred that the off-state current

decreases with fewer layer of MoS_2 due to the higher bandgap, as supported by related researches[11-14]. Considering speed, storage time, and holding voltage comprehensively, we selected bilayer MoS_2 as the channel material.

At the last sentence of the first paragraph on page 9 of the revised manuscript, we now provide a more explicit rationale for using bilayer MoS_2. The revised text is as follows:

'Based on the requirements for long retention time, high write speed, and low static power consumption in DRAM applications, achieving a balance between low off-current, high on-current, and an appropriate threshold voltage (V_{th}) for the write transistor poses a significant challenge. Based on related researches[11,12,14] and experimental results detailed in Supplementary Figure 3, bilayer MoS_2 demonstrates a balanced combination of V_{th}, I_{ON}, and I_{OFF} simultaneously, therefore, it is chosen as the channel material for the write transistor in this paper.'

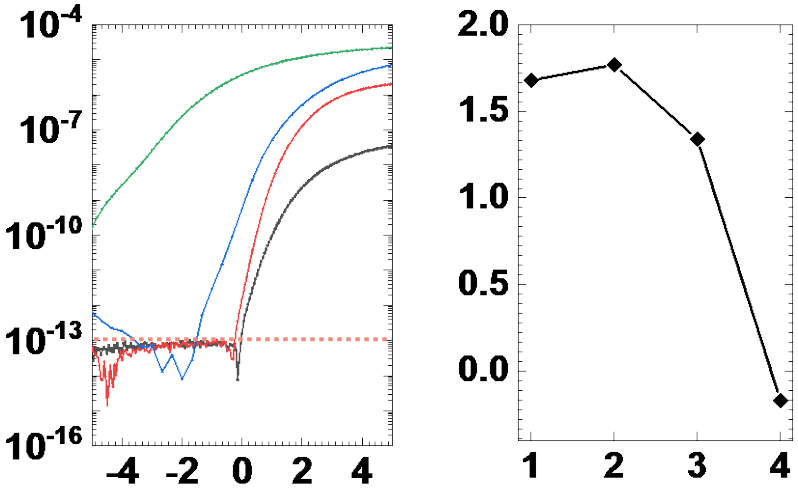

Figure R3 Electrical performance of the transferred monolayer to few-layers MoS_2 FETs. **a.** Transfer characteristics of the 1 L-4 L MoS_2 FETs at a bias voltage of 1 V. **b.** The extracted V_{th} as a function of the number of MoS_2 layers.

Comment 4

Line 221 in Page 9, the switch ratio between the ON current of the reading FET (~270uA~10^-4A) and the OFF current (10^-13A) of the writing FET is about 10^9 or 10^10. Why do authors claim 10^14 in Fig. 2c?

Response:

Thanks for raising the question. Due to the equipment constraints, the minimum measurable current is on the order of 10^{-13} A, and currents below this level are masked by noise. Therefore, the minimum current shown in the transfer curve in Figure 2b does not represent the actual I_{OFF}. This is a common issue in memory device researches, and the actual I_{OFF} is typically calculated using retention time and storage node capacitance[6-8]. The detailed derivation of I_{OFF} is provided below:

The variation of stored charges and V_{SN} over time during capacitor discharge can be described by equation (1) and (2):

$$Q_{SN}(t) = Q_{SN}(0) - \int_0^t I_{OFF}dt \qquad (1)$$

$$V_{SN}(t) = \frac{Q_{SN}(t)}{C_{SN}} = V_{SN}(0) - \frac{1}{C_{SN}}\int_0^t I_{OFF}dt \qquad (2)$$

$$I_{OFF}(t) = \frac{dQ_{SN}(t)}{dt} = \frac{C_{SN} \times dV_{SN}(t)}{dt} \qquad (3)$$

To simplify calculations, I_{OFF} is assumed to remain constant. As retention time is defined as the duration during which the storage node voltage drops by 0.1V, I_{OFF} can be calculated using equation (4):

$$I_{OFF} = \frac{Q_{SN}(0) - Q_{SN}(t_{ret})}{t_{ret}} = \frac{C_{SN} \times [V_{SN}(0) - V_{SN}(t_{ret})]}{t_{ret}} = \frac{C_{SN} \times 0.1V}{t_{ret}} \qquad (4)$$

In the original manuscript submitted, C_{SN} was calculated using the formula for parallel plate capacitors and the calculated I_{OFF} is approximately 3.9×10^{-18} A/μm, which is reasonable but lacks precision. To improve the accuracy of I_{OFF} calculation, we performed CV measurement to obtain the precise capacitance of SN node and recalculated I_{OFF}, as illustrated in Figure R4(Supplementary Figure 4 on page S6 of the revised manuscript) and described by equation (5) and (6):

$$I_{OFF(2L)} == \frac{C_{SN} \times 0.1V}{t_{ret}} = \frac{0.032pF/\mu m \times 0.1V}{1000s} = 3.2 \times 10^{-18} A/\mu m \qquad (5)$$

$$I_{OFF(1L)} = \frac{C_{SN} \times 0.1V}{t_{ret}} = \frac{0.032pF/\mu m \times 0.1V}{6000s} = 5.3 \times 10^{-19} A/\mu m \qquad (6)$$

As the I_{ON} of read transistor is around 10^{-4}A/μm, the I_{ON_R}/I_{OFF_W} of Si-2L MoS_2 2T-

eDARM is around 10^{14}. The detailed deviation and the C_{SN}-V_{SN} curve are supplied in Supplementary Note 2 and supplementary Figure 4.

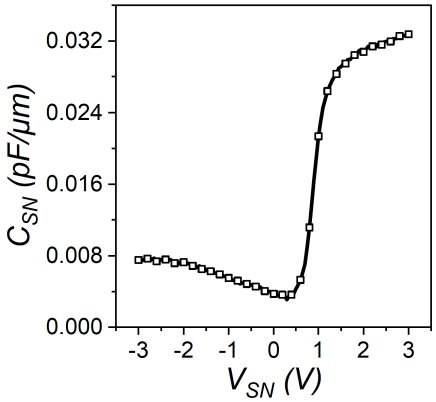

Figure R4 The measured CV curve of SN node.

Comment 5

The authors attribute the improvement of sense margin and retention to the higher ON current held by the Si FET and lower leakages via the MoS_2 FET, for which is intuitive but reasonable. The referee inquires whether the authors referenced any formula or model to correlate the sense margin with the ON current. This correlation would provide additional validation for the selling point presented in their experimental observations.

Response:

We appreciate the reviewer for this valuable comment. Sense margin refers to the variation in output signal between data "1" and "0", and it is quantified as the difference in read current observed when the storage node is charged (representing data "1") versus when it is not charged (representing data "0") in our paper. For a read transistor with an appropriate threshold voltage (V_{th}), when the storage node (SN) is charged (data "1"), V_{SN} turns the device on with a high current density. Conversely, when the SN is not charged (data "0"), the device remains off. Therefore, the sense margin can be expressed as:

$$\begin{aligned}\text{Sense margin} &= I_{RBL}(\text{data "1"}) - I_{RBL}(\text{data "0"}) \\ &= I_{D\_READ}(V_{G\_READ} = V_{SN}) - I_{D\_READ}(V_{G\_READ} = 0) \\ &\approx I_{D\_READ}(V_{G\_READ} = V_{SN})\end{aligned} \quad (1)$$

Based on the transfer characteristics curves shown in Figure R5, under a fixed voltage difference (V_{SN}-0), the Si transistor exhibits a larger range of current variations, indicating a higher sense margin compared to the MoS_2 transistor.

In the practical operation of DRAM arrays, the current from RBL needs to be amplified and read by the sense amplifier (SA). Given that the minimum detectable current by SA remains fixed[15], using materials that exhibit higher on-state currents for read transistors effectively enhance output reliability.

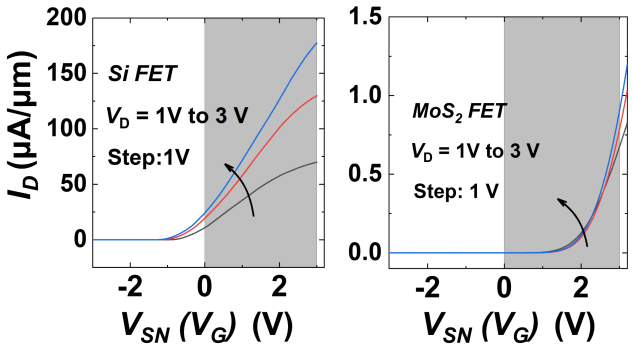

Figure R5 The transfer curves of Si transistor and MoS_2 transistor in linear coordinates. Within a fixed range of V_{SN} (V_G) variation (using gray areas as an example), Si transistors have a larger ΔI_D, which is conducive to be sensed and amplified.

Comment 6

In Figure 3a, why does high current with logic "1" drop sharply at 1000 s? Please clarify it.

Response:

Thank you for raising the thought-provoking question for discussion. There are two reasons why data "1" appears to rapidly decrease at 1000 s. Firstly, in Figure 3a, the X-axis is in logarithmic scale, which makes data "1" appear to drop quickly on the axis, but in reality, this process spans several thousand seconds. We exhibited a new plot with a linear time axis, showing that the decline of data "1" is more gradual in linear

coordinates, as shown in Figure R6(b). Secondly, as illustrated by the I_D-V_G curve of the Si FET in Figure R6(c), the drain current initially reduces slowly with V_{SN} (V_G), then accelerates before gradually decelerating, forming an "S" shaped curve. In regard to the proposed 2T-DRAM, as V_{SN} gradually decreases due to the OFF current, which effectively reducing the V_G of the read transistor. Thus, the retention curve of reading current over time also shows a shape similar to an "S", resulting in a sharp decline observed between 1000 and 3000 seconds, as shown in Figure R6(b).

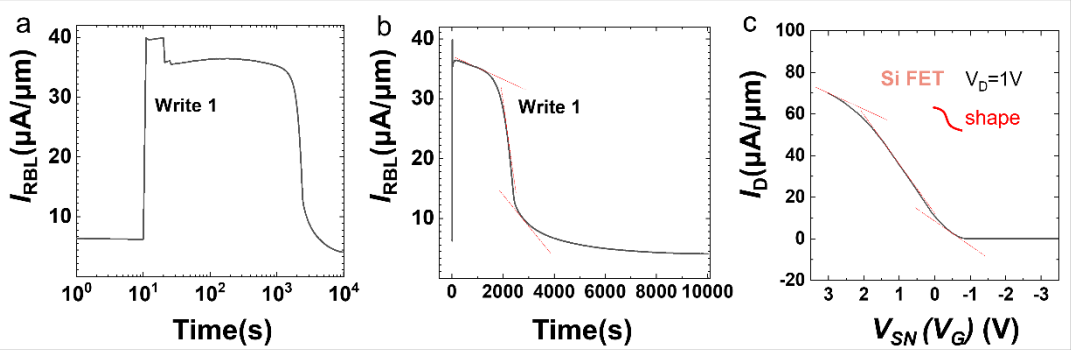

Figure R6. The retention characteristic with time in a. log x axis and b. linear x axis. c. transfer curve of Si transistor in linear coordinates. The drain current (I_D) increases in an S-shaped pattern with respect to V_{SN} (V_G).

Comment 7

In Figure 3d, the referee requests clarification regarding the formula presented. The referees are unsure how to interpret the value of 3.9 × 10^-18 and please seek a definition or description to aid reader's understanding.

Response:

We apologize for any confusion caused by a minor error in our formula, the author carelessly wrote the formula as $\boldsymbol{I_{OFF} = \frac{0.1V \times V_{SN}}{t_{ret}}}$, while the revised formula is $\boldsymbol{I_{OFF} = \frac{0.1V \times C_{SN}}{t_{ret}}}$. This is a method commonly used to estimate OFF current when limited by the measurement capabilities of equipment [6-8]. We have measured the capacitance of SN node and recalculated the OFF current, as shown in equation (1) and (2). The specific derivation process and CV curve are supplied in the revised supplemental material and

can be found in the response to the fourth comment of the reviewer 1# and Figure R4.

$$I_{OFF(2L)} == \frac{C_{SN} \times 0.1V}{t_{ret}} = \frac{0.032pF/\mu m \times 0.1V}{1000s} = 3.2 \times 10^{-18} A/\mu m \quad (1)$$

$$I_{OFF(1L)} == \frac{C_{SN} \times 0.1V}{t_{ret}} = \frac{0.032pF/\mu m \times 0.1V}{6000s} = 5.3 \times 10^{-19} A/\mu m \quad (2)$$

Comment 8

The referee notes a discrepancy between the schematics and cross-sectional SEM image in Figures 4d and 4e, highlighting a lack of alignment between the two representations. Revise it.

Response:

We sincerely apologize for our oversight and appreciate the reviewer for pointing out our mistake. The precise location of the channel cross-section, as indicated in the STEM image, has been remarked. The mistake has been rectified in the revised manuscript, and detailed explanations have been provided to clearly demonstrate every layer, as depicted in Figure R7 (Figure 4d and e in the revised manuscript).

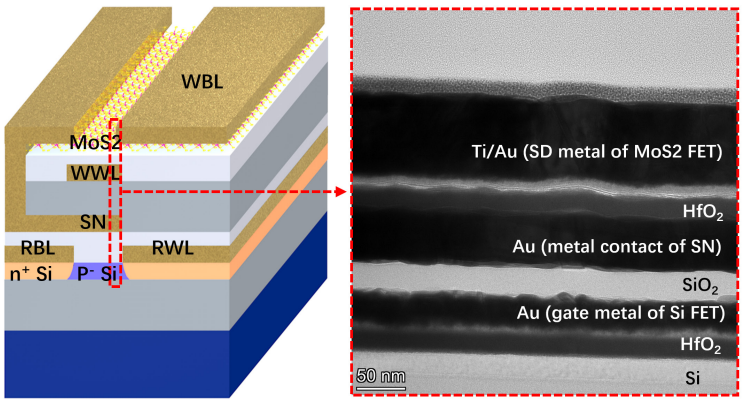

Figure R7. The updated *Figures 4d and 4e in the revised manuscript. The channel location of the schematic diagram is remarked to* correspond with the STEM image.

Comment 9

How many devices were fabricated? It is worth to note the reliability and reproducibility of the proposed fabricated process.

Response:

Thank you for the concern about the reliability and reproducibility of the proposed fabricated process. More than 100 devices are fabricated. However, due to the long retention times of the devices, which resulted in prolonged measurement durations, only a subset of devices was randomly selected for reliability and reproducibility studies. Figure R8 illustrates the retention performance of V_{SN} over time for seven devices. The storage node voltage variations across these devices during the 1000 s period are consistently below 0.1 V, indicating good reliability and reproducibility.

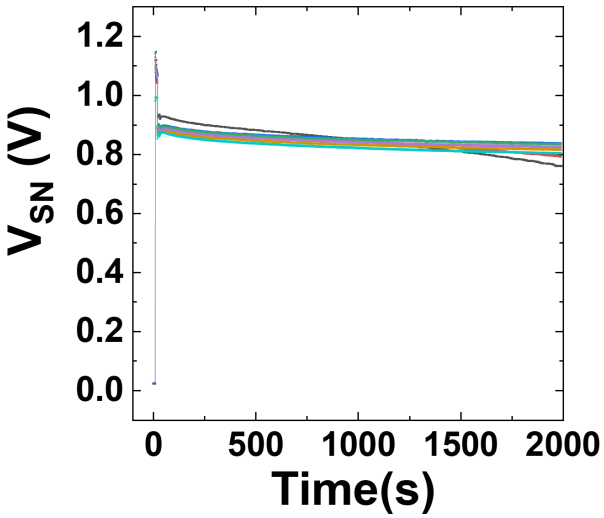

Figure R8. Time-dependent V_{SN} variation among seven devices.

Comment 10

Considering state-of-the-art non-volatile memories, a retention of 6000 seconds cannot be considered extremely long. Please avoid using "extremely" and its synonyms.

Response:

Thanks for pointing out the inappropriate description, such words have been modified in the revised manuscript.

Comment 11

Fig. 4a somewhat looks like a band structure under a negative gate voltage, which would be contradictory to the zero hold bias as claimed. To prevent misunderstanding, the band structure should be refined to reflect the real case in the proposed MoS_2 device. In addition, the definition/notation of leakage in the paper is not the same with that has been commonly used for field-effect transistors, where leakage is nominally referred to the current through the gate and drain terminals. This is something that needs to be noted in the paper.

Response:

Thanks for the reminder. In order to avoid confusion, we have revised the description in the article and substituted 'OFF current' for 'leakage'. And regarding the issue of energy band diagrams, although MoS_2 transistors are n-channel depletion devices, due to the difference in work function between the channel and gate materials, the device's energy band is not in a flat band state. As shown in Figure R9. a (Supplementary Figure 3), even at V_G= 0 V, 1 L and 2 L MoS_2 devices are in off state, which means there is a potential barrier in the channel to prevent the injection of carriers. To illustrate this point, we have revised the energy band diagram in Figure 4a in the revised manuscript to provide a detailed explanation of the bias state corresponding to the energy band diagram, as shown in Figure R9.

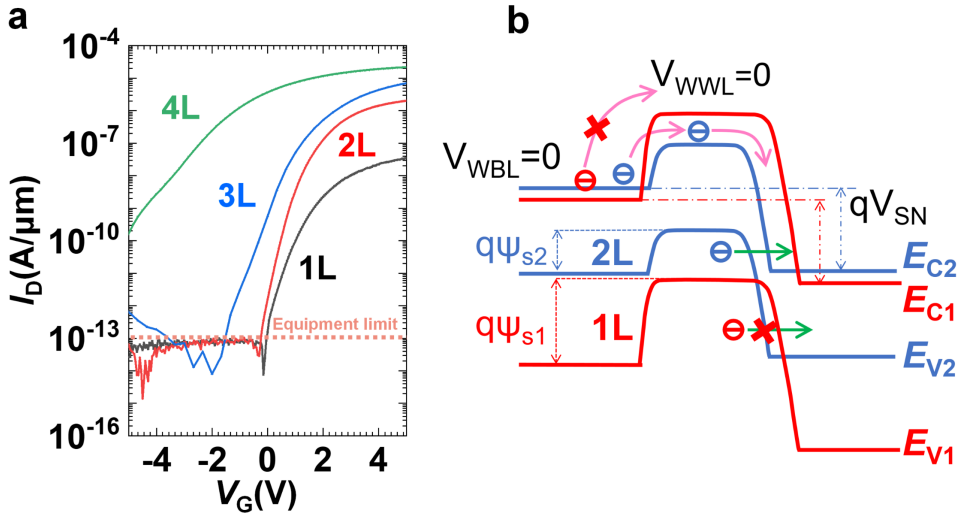

Figure R9. a. The Transfer curves of MoS_2 transistors with different layers. **b.** Revised energy band diagrams. The barrier in the channel is induced by the difference

in work function between the MoS_2 and gate materials.

Comment 12

The developed process was claimed to be a BEOL-compatible process. Through detailed literature searching, the referee found that in terms of 3D integration of 2D materials and Si technology, some manufacturing processes were recently reported and also appear to be promising like the one presented in the paper. For instance, [S. X. Guan, et al. npj 2D Mater. Appli. 2023, 7, 9] or [J. H. Kang, et al. Nat. Mater. 2023, 22, 1470-1477], to name a few. It would be great to involve a discussion about the technological merits between the current work and parallel research works.

Response:

Thanks for the suggestion. We have referenced the literature recommended by the reviewers and related literatures and discussed Si-2D integration. 2D materials, known for atomic thickness and layer-dependent electrical properties, are promising candidates for the future electrons[16]. Devices and circuits based on 2D materials have demonstrated exciting performance[2,17-19]. Meanwhile, due to the naturally passivated surface and weak van der Waals interaction, 2D materials can be integrated onto various substrates without lattices mismatch[20]. Considering the high compatibility of 2D materials and mature processes of silicon, integrating 2D materials with silicon rather than replacing it offers more economical and extensive prospects. Additionally, benefiting from low thermal budgets and stack ability, integrating silicon with 2D materials (2DMs) holds greater promise for 3D integration compared to traditional 3D integration technologies, which suffers from high parasitic capacitance and residual heat/mechanical stress during stacking[21,22]. As of now, milestone works have emerged, such as heterogeneous photonic devices[23], heterogeneous CFETs[21,24], and graphene-Si analog-digital circuits[25].

In the second paragraph on page 4 of the revised manuscript, we have added the discussion about Si-2D integration, with specific details as follows:

'Additionally, the combination of low thermal budgets and stack ability makes the integration of merging 2D material with mature Si technology a promising avenue for three-dimensional (3D) integration with high density, simple processing, and multifunctionality compared to traditional 3D integration of Si technologies, which suffer from high parasitic capacitance and residual heat/mechanical stress during stacking[21,22]. To date, milestone works have emerged, such as heterogeneous photonic devices[23], heterogeneous CFETs[21,24], and graphene-Si analog-digital circuits[25], exemplifying the potential for applications and industrialization.'

Typos and Minor comments 1: At Line 176 in Page 7, there is a typo in the sentence, directly quoted "Figure 1c exhibit three characteristic peaks of MoS_2:", though the presented spectra show only two peaks. Please correct the number of the Raman peaks.

Response:

Thank you for point out the issue. We have corrected the mistake in the revised manuscript, the corrected sentence is as follows:

The Raman spectra in Figure 1c exhibit two characteristic peaks of MoS_2: the in-plane E^1_{2g} vibrational mode at 383.0 cm^{-1}, and the out-of-plane A_{1g} vibrational mode at 407.0 cm^{-1}.

Typos and Minor comments 2: Kindly remind that the axis titles and units are missing in Supplementary Fig. 3. Fig. 6, Fig. 11 and Fig. 12. These are not professional figures.

Response:

Great thanks to the reviewer for kindly pointing out the mistake. All these figures have been revised to meet publication standards.

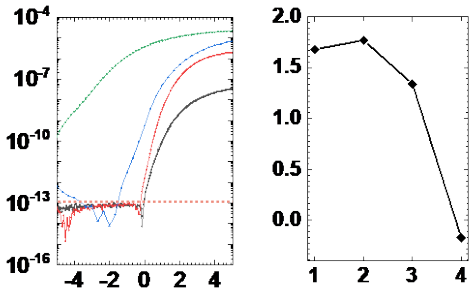

Figure R10. The revised *Supplementary Fig. 3. (Supplementary Fig. 3 in the revised manuscript.)*

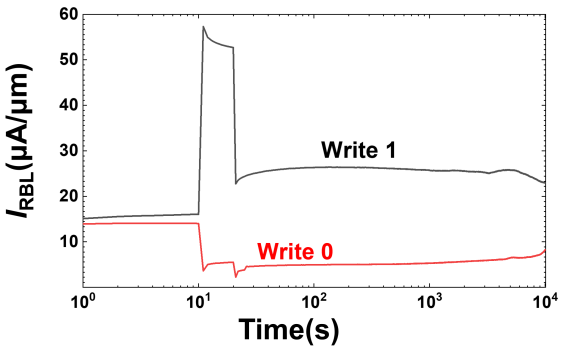

Figure R11. The revised *Supplementary Fig. 6. (Supplementary Fig. 7 in the revised manuscript.)*

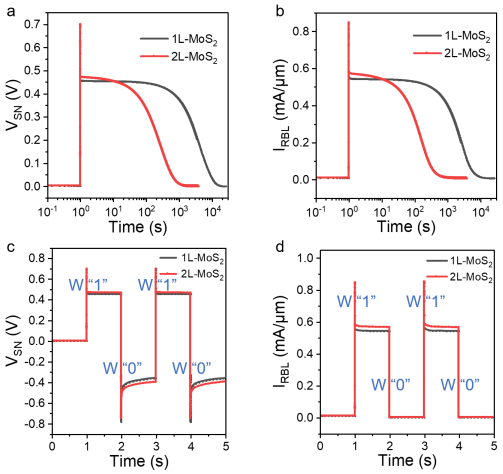

Figure R12. The revised *Supplementary Fig. 11. (Supplementary Fig. 13 in the revised manuscript.)*

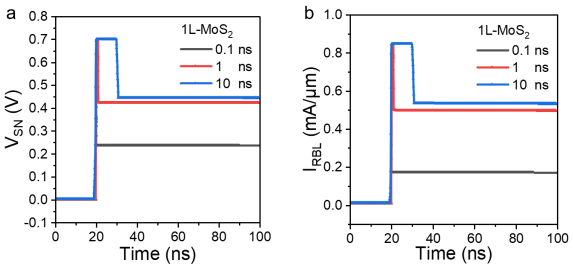

Figure R13. The revised *Supplementary Fig. 12. (Supplementary Fig. 14 in the revised manuscript.)*

Typos and Minor comments 3: At Line 226 in Page 9, the authors might have to add relevant references for the simplified model.

Response:

Thanks for the reminder and we have included references for the model in the revised manuscript. This model originates from the saturation current model of an ideal

MOSFET under ideal conditions[26], as shown in Equation (1), where the saturation current ideally depends only on V_{GS}.

$$I_D = \frac{u_0 \cdot C_{ox} \cdot W}{L} \cdot (V_{GS} - V_{th})^2 \quad (1)$$

Considering the parasitic resistance as depicted in Figure R14, we can derive the simplified model, as shown Equation (2) and (3).

$$V_{GS} = V_G - V_S = V_G - I_D R \quad (2)$$

$$I_D = \frac{u_0 \cdot C_{ox} \cdot W}{L} \cdot (V_{GS} - V_{th})^2 = I_D = \frac{u_0 \cdot C_{ox} \cdot W}{L} \cdot (V_G - V_{th} - I_D R)^2 \quad (3)$$

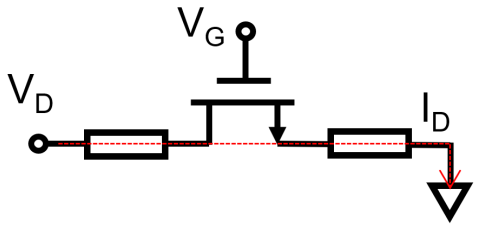

Figure R14. The simplified diagram of MOSFET with parasitic resistances

Typos and Minor comments 4: In what conditions were those devices measured (i.e. vacuum or ambient)? The info should be provided somewhere in the manuscript.

Response:

We are grateful for your helpful reminder. All these devices are measured under constant temperature of 25 ℃ in ambient atmosphere. We have supplied the measure condition at the first sentence in the first paragraph on page 10 of the revised manuscript. And the detailed modification is as below:

'After device fabrication, comprehensive electrical measurements are conducted under constant temperature of 25 ℃ in ambient atmosphere.'

Typos and Minor comments 5: At Line 332 in Page 13, The word "heterogeneous" seems not necessary and should be deleted. At 332 in the same page, in "MOS2" the O should be a lower case "o". Typos and inaccurate grammars are found in many places over the manuscript, which is distracting

during reading. It would be helpful to address the paper format more carefully and have a professional editor for proofreading before submitting the revised version.

Response:

Thanks for the suggestions, as they have greatly assisted in improving the manuscript. We have thoroughly checked and corrected the grammar and typos throughout the entire text.

Typos and Minor comments 6: Are Vsn and VSN the same? Please make it consistent if they are the same.

Response:

Yes, they are the same. In the revised manuscript, we have employed V_{SN} for consistent expression, and we have meticulously reviewed similar errors to ensure uniformity of abbreviations and symbols throughout the manuscript.

Typos and Minor comments 7: Symbols for authors contributed equally (*) and corresponding authors (†) are typos in the notation used in title page.

Response:

Thank you for your reminder. We have corrected the error and carefully checked the entire manuscript to avoid similar mistakes.

Typos and Minor comments 8: The referee suggests reorganizing Figure 2, 3 and 4, as each figure looks too crowded, making it difficult to distinguish each sub-figure.

Response:

Thanks for the suggestion. We have reorganized Figures 2, 3, and 4 to make the sub-figures easier to distinguish, as shown in Figure R15-R17.

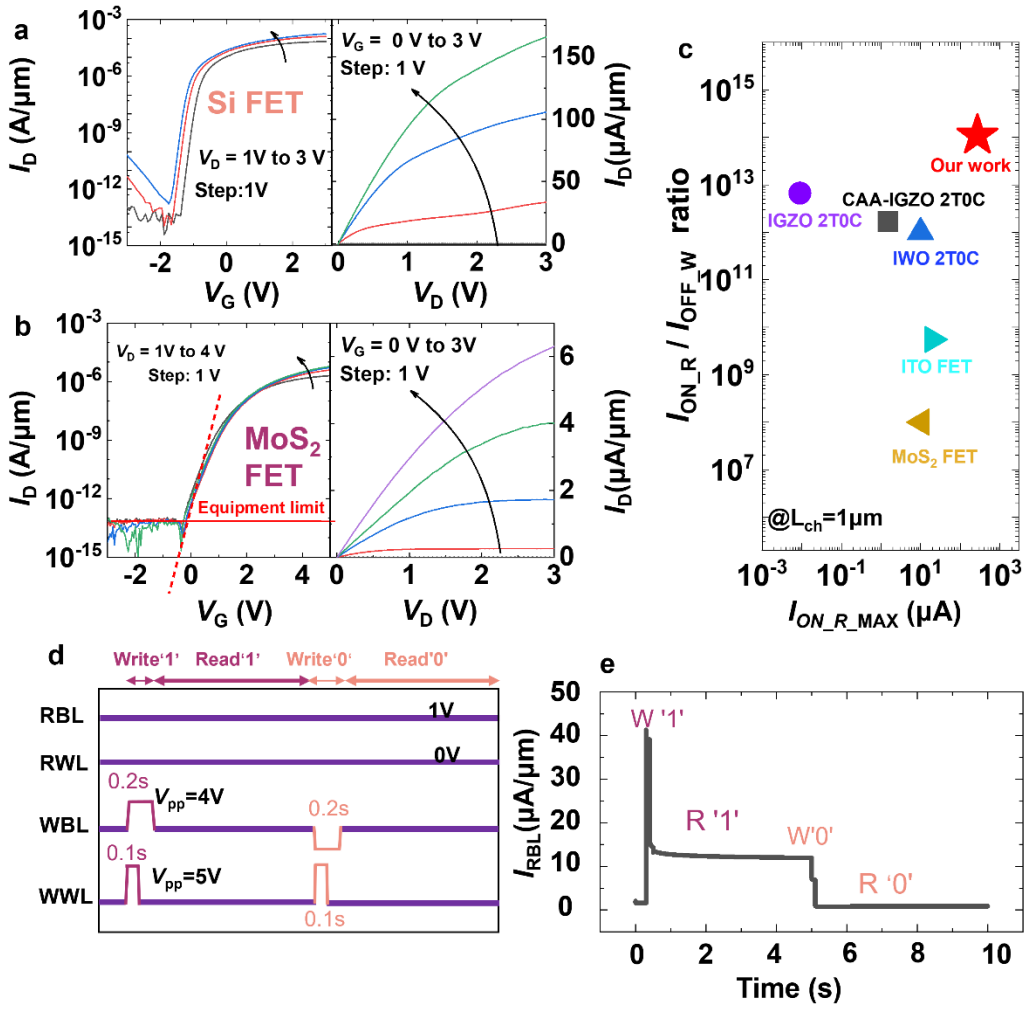

Figure R15. Reorganized Figure 2 in the revised manuscript.

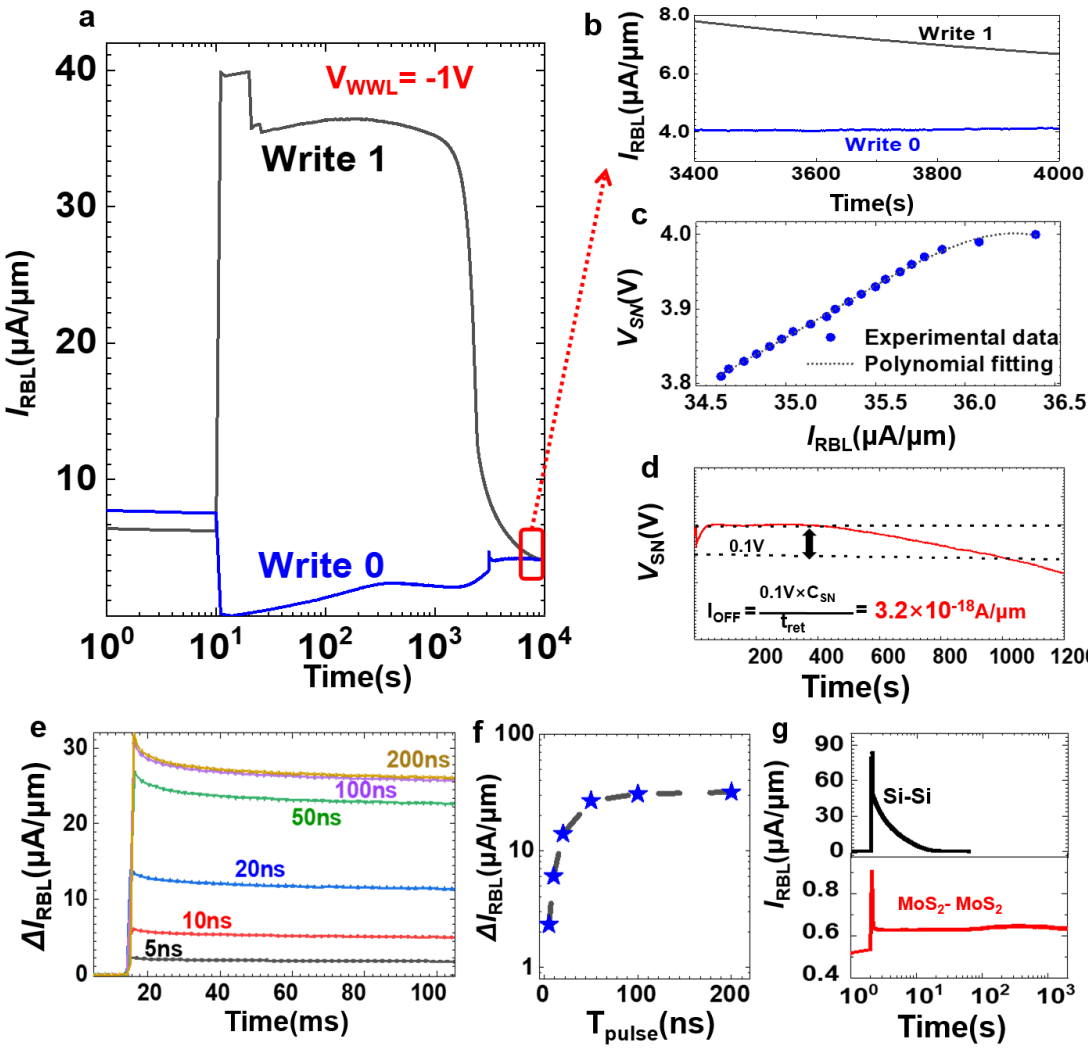

Figure R16. Reorganized Figure 3 in the revised manuscript.

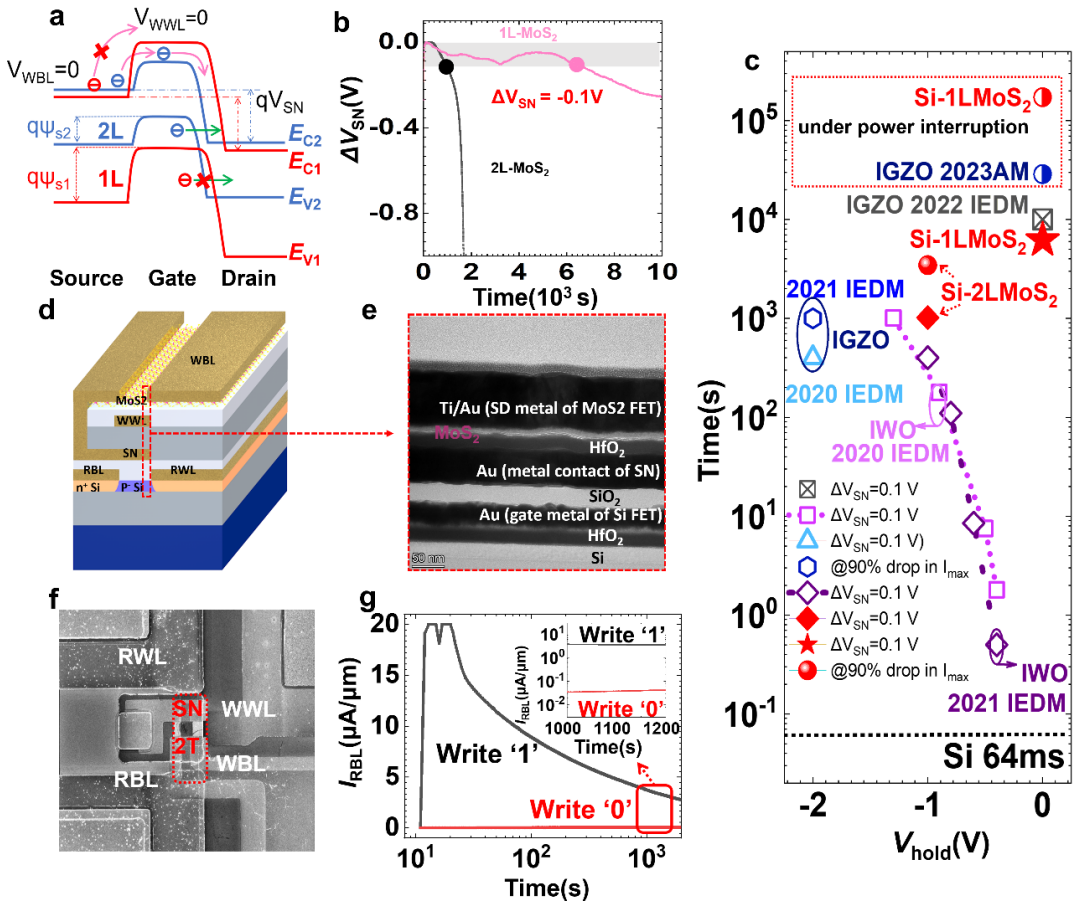

Figure R17. Reorganized Figure 4 in the revised manuscript.

Reviewer #2:

I co-reviewed this manuscript with one of the reviewers who provided the listed reports. This is part of the Nature Communications initiative to facilitate training in peer review and to provide appropriate recognition for Early Career Researchers who co-review manuscripts.

Response:

We sincerely appreciate the reviewer for taking the time to review our manuscript. We have carefully rechecked and revised the paper. The modifications are indicated with red strikethroughs for deletions and yellow highlights for additions in the revised manuscript. We believe the revised article now better meets the publication requirements of Nature Communications.

Reviewer #3：

The proposed research work based on Si-MoS_2 heterogenous eDRAM technology promises significant improvements in data retention and integration density.

Further, authors have addressed the challenges such as fabrication complexity, long-term stability, scalability, and compatibility issues practical implementation.

Minor comment:

I some places authors have used Fig and Figure, it would be better to be consistent with terminology. Also there is need of careful proof reading.

Response:

We do appreciate the reviewer for the positive feedback on our manuscript. Your recognition is greatly encouraging to our research. The challenges you mentioned, such as fabrication complexity, long-term stability, scalability, and compatibility issues for practical implementation, have always been our ongoing goals. We will continue to address these challenges in our future work. Additionally, regarding your minor comment, we have replaced "Fig" with "Figure" throughout and carefully checked the grammar and wording to better align with the publication requirements. The modifications are indicated with red strikethroughs for deletions and yellow highlights for additions in the revised manuscript.

Reviewer #4：

The authors report on the first demonstration of a heterogenous gain cell embedded DRAM (GC-eDRAM) combining silicon (Si) and molybdenum disulfide (MoS_2) to improve the data retention and integration density of GC-eDRAM.

This is realized in a 3D-integrated BEOL-compatible process, which offers great promise for integrating mixed Si-2D technology for embedded memory.

In particular, the memory behavior reported in this work is impressive and surpasses state-of-the-art reports for eDRAM based on full-Si CMOS, full-2D materials, and oxide semiconductor materials.

In particular, the Si-MoS_2 heterogenous eDRAM shows long data retention (up to 6000 s), high sense margin, fast operation (5 ns access time), and 3D integration capability.

Overall, this work is not only of great interest to embedded memory community, but also to the heterogenous Si-2D community, which will be of increasing importance going forward for next-generation high-performance computing and high-bandwidth memory paradigms. Therefore, this work is both timely and impactful .

I have the following minor comments. After these minor comments are addressed, I can recommend the manuscript for publication in Nature Communications.

Sincerely, Suraj Cheema

Response:

We sincerely appreciate the reviewer's affirmation and valuable suggestions. We have carefully revised the manuscript in response to your comments. The modifications are indicated with red strikethroughs for deletions and yellow highlights for additions in the revised manuscript. The specific modifications are as follows

Comment 1：

*ON-OFF and benchmarking (Figure 2). In Fig 2c, it is better to denote "I_{ON}/I_{OFF}" as "I_{ON_R}/I_{OFF_W}" to avoid confusions. Also, based on Figu 1a and 1b, the value of I_{ON_R}/I_{OFF_W} for the DRAM in this work seems it should be around 1e10 (around 100*1e-6 /1e-14) at 1V VD instead of 1e14. Could the authors clarify where the 1e14 number comes from? If the number is indeed 1e10, then it does not demonstrate much advantage in this metric over the other candidates, and the authors should clarify this.*

Response:

Thanks for the valuable suggestions. We have revised the title of Figure 2 as "I_{ON_R}/I_{OFF_W} ratio" to avoid confusion. Regarding the issue raised about 10^{14}, we have provided additional clarification in the revised manuscript. Due to limitations of the measuring equipment, there are inaccuracies in the assessment of I_{OFF} in the transfer curve in figure 2b as the minimum measurable current is around 10^{-13}A and currents below this level are masked by noises. This measurement limitation is prevalent in memory device researches, and actual off-state currents are usually calculated based on the retention time and capacitance[6-8]. The detailed derivation is provided below:

The variation of stored charges and V_{SN} over time during capacitor discharge can be described by equation (1) and (2):

$$Q_{SN}(t) = Q_{SN}(0) - \int_0^t I_{OFF}dt \tag{1}$$

$$V_{SN}(t) = \frac{Q_{SN}(t)}{C_{SN}} = V_{SN}(0) - \frac{1}{C_{SN}}\int_0^t I_{OFF}dt \tag{2}$$

$$I_{OFF}(t) = \frac{dQ_{SN}(t)}{dt} = \frac{C_{SN} \times dV_{SN}(t)}{dt} \tag{3}$$

To simplify calculations, I_{OFF} is assumed to remain constant. As retention time is defined as the duration during which the storage node voltage drops by 0.1V, the I_{OFF} can be calculated using equation (4):

$$I_{OFF} = \frac{Q_{SN}(0) - Q_{SN}(t_{ret})}{t_{ret}} = \frac{C_{SN} \times [V_{SN}(0) - V_{SN}(t_{ret})]}{t_{ret}} = \frac{C_{SN} \times 0.1V}{t_{ret}} \tag{4}$$

In the original manuscript submitted, we calculated C_{SN} using the formula for parallel plate capacitors and the calculated I_{OFF} is approximately 3.9×10^{-18} A/μm, which is reasonable but lacks precision. To improve the accuracy of I_{OFF} calculation, we performed CV measurement to obtain the precise capacitance of SN node and recalculated I_{OFF}, as illustrated in Figure R18 (supplementary Figure 4 in the revised manuscript) and described by equation (5) and (5):

$$I_{OFF(2L)} == \frac{C_{SN} \times 0.1V}{t_{ret}} = \frac{0.032pF/\mu m \times 0.1V}{1000s} = 3.2 \times 10^{-18} A/\mu m \qquad (5)$$

$$I_{OFF(1L)} == \frac{C_{SN} \times 0.1V}{t_{ret}} = \frac{0.032pF/\mu m \times 0.1V}{6000s} = 5.3 \times 10^{-19} A/\mu m \qquad (6)$$

As the I_{ON} of read transistor is around 10^{-4}A/μm, the I_{ON_R}/I_{OFF_W} of Si-2L MoS_2 2T-eDRAM is around 10^{14}. The detailed deviation and the C_{SN}-V_{SN} curve are supplied in supplementary Note 2 and supplementary Figure 4.

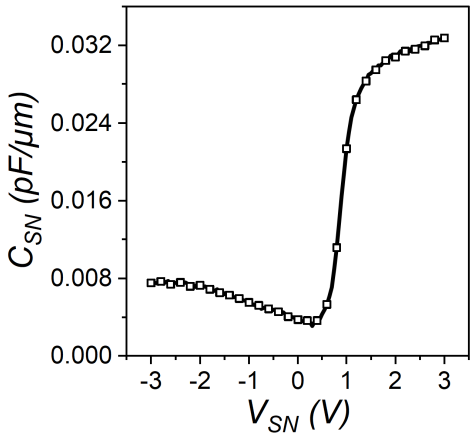

Figure R18. The measured CV curve of SN node.

Comment 2:

Parasitic and gate capacitance. How large is the parasitic capacitance at the SN node when stacking the MoS_2 transistor on top of the silicon transistor. The authors should provide a quantitative comparison with the gate capacitance of the silicon transistor.

Response:

Thanks for the suggestions. CV measurements are conducted to investigate the SN capacitance and parasitic capacitance between SN node and WWL of the vertical

stacked heterogeneous 2T-eDRAM. As the standard MIS CV characteristic shown in Figure R19 b, the SN capacitance is 0.28 pF while the parasitic capacitance is 0.033 pF.

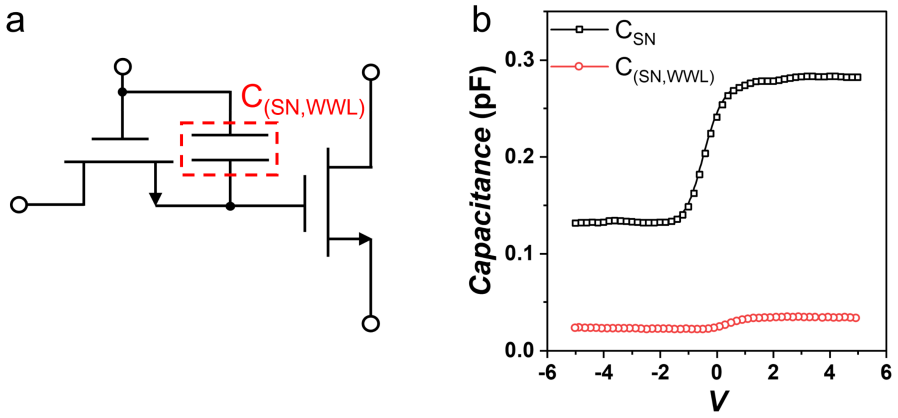

Figure R19. a. Schematic diagram of the parasitic capacitance in 2T-eDRAM. **b.** The measured CV curve of SN node and parasitic capacitance of the vertical stacked heterogeneous 2T-eDRAM.

Comment 3:

Comparison to Si 2T-eDRAM: The authors should please comment on the area and cost (e.g., additional lithography steps) of the heterogeneous 2T-eDRAM, compared with conventional silicon 2T-eDRAM, in a highly integrated case (i.e., without probing pads). [this can be conveyed in the comparison table mentioned in Comment 5].

Response:

We thank the reviewer for the suggestion of comparison. The proposed planar Si-MoS_2 2T-eDRAM in the article has the same area cost as conventional Si 2T-eDRAM. However, the vertical Si-MoS_2 2T-eDRAM, which is proposed to integrate both the read and write transistors in a 1T-layout through stacking, can reduces the area cost by 50%.

For homogeneous planar 2T-eDRAM devices, the write and read transistors are manufactured simultaneously and interconnected. In contrast, heterogeneous integrated devices and stacked devices require sequential manufacturing of the write and read

transistors. In order to illustrate the additional steps involved in the fabrication process, we take the Si-MoS_2 heterogeneous integrated 2T-eDRAM proposed in the article as an example. As can be seen in Figure R20 (Supplementary Figure 1), the fabrication process flow involves four additional steps:

1. Deposition of dielectric insulating layer and metal to form the gate electrode as MoS_2-FET.
2. Dielectric deposition to form the gate dielectric of MoS_2-FET, transfer of bilayer MoS_2 on top of the second dielectric, and etching of the dielectric on the gate of Si-FET using SF6.
3. Metal deposition to form the source/drain of MoS_2-FET and the interconnections of the upper and lower transistors.
4. Etching of unnecessary MoS_2 using CF4.

   The aforementioned four steps entail lithography for metal lift-off and defining etch regions as required. Additionally, we included an extra lithography step in our benchmark to better compare the associated process costs, as shown in Table RI (Table S1 in the revised supplementary information)

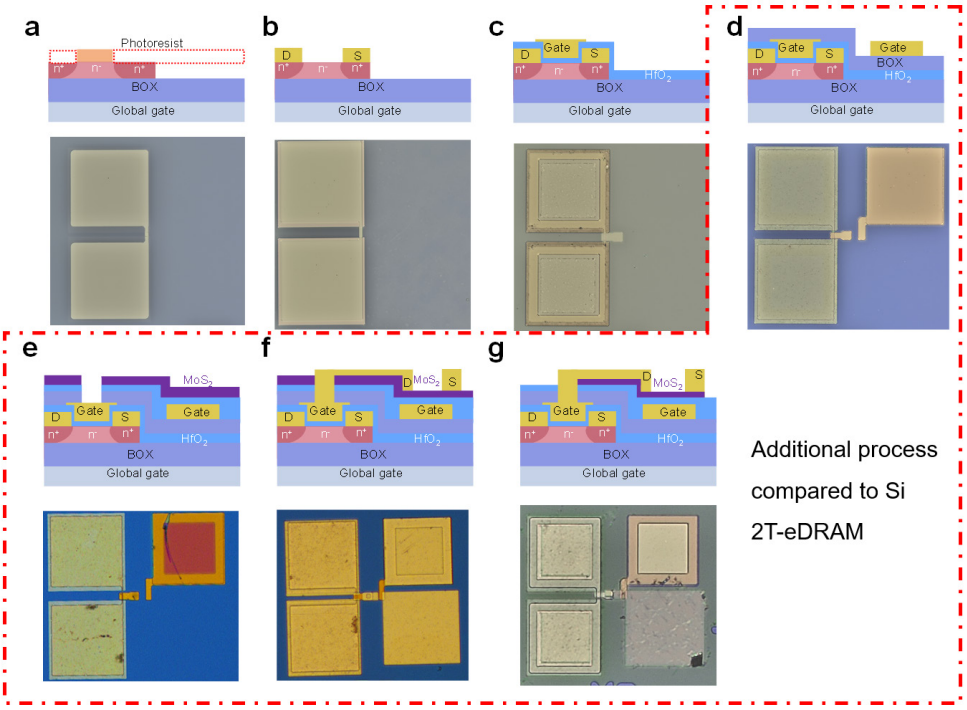

Figure R20. The process flow of fabricating 2T-DRAM. The parts circled in red indicate additional steps compared to conventional planar Si 2T-eDRAM

TABLE RI

Summarizes of The Major Parameters of Other Typical Related Work

Reference	2016[1]	2016[2]		2021[3]		2008[4]	2020[5]	2023[6]	2022[8]	2023[9]	2023[10]	This Work	
Structure	1T1C	1T1C	2T0C	1T1C	2T1C	2T0C	2T0C	2T0C	2T0C	Stacked 2T0C	Stacked 2T0C	Planer 2T0C	Stacked 2T0C
Material	Si	MoS_2		MoS_2		Si	IWO	ITO	IGZO	IGZO	IGZO	Si- MoS_2	
Write pulse width	8.75ns	0.2ms	-	20ms	140ms	8ns	3ns (simulation)	100 ns	10ns	-	5ns	5ns/1ns(simulation)	
Retention time	64ms	>251ms	>1s	>10s	>100s	~5us	1-10s	2250 s	>7000s	20s	75s	1000s(2L) 6000s(1L)	>1000s/ 65s(simulation)
$I_{OFF\ W}$ (A/μm)	-	10^{-15}-10^{-18}		<10^{-13}			10^{-15}	4×10^{-19}	<6×10^{-20}	-	<10^{-13}	3.2×10^{-18}(2L), 5.3×10^{-19}(1L)	
$I_{ON\ W}$ (A/μm)	-	10^{-6}		10^{-7}-10^{-8}		-	10^{-4}	22.6×10^{-6}	24×10^{-6}	-	10^{-5}– 10^{-6}	6.31×10^{-6}	
$I_{ON\ R}$ (A/μm)												166×10^{-6}	
Sense margin (μA/μm)	-	-		-	<0.01	-	-	-	~27		≤10	35	20
Additional lithography	-	-		-	-	-	1	-	-	4	4	4	
Compatibility	-	BEOL		BEOL		CMOS	BEOL	BEOL	BEOL	BEOL	BEOL	BEOL	
Feature size	1x (19-17nm) $6F^2$	0.5μm		20μm		50nm	50nm	50nm	70nm	75nm $4F^2$	65nm $4F^2$	3μm (10nm in simulation) $4F^2$ for stacked 2T0C	
"-" represents that the data is not available.													

Comment 4:

Discussion on 1T1C-eDRAM: The introduction states: "However, the 1T1C eDRAM needs high pillar capacitor whose fabrication is not compatible with CMOS logic process9. Thus, it is typically fabricated separately with DRAM process and bonded to the processing unit chip with 2.5D and 3D packaging technology". There are many examples of integrated 1T1C eDRAM where the trench process is directly fabricated over the CMOS logic, e.g. ref [R1]. So the authors should adjust this critique of 1T-1C and instead mention a different benefit of GC structure over 1T-1C [this benefit can be conveyed in the comparison table mentioned in Comment 5].

Response:

Thanks for the reviewer's reminders and suggestions. We have consulted the paper you referenced and other relevant researches, re-evaluated the 1T1C eDRAM cell, and revised our previous mischaracterizations as follows:

The original description:

'However, the 1T1C eDRAM needs high pillar capacitor whose fabrication is not compatible with CMOS logic process[27]. Thus, it is typically fabricated separately with

DRAM process and bonded to the processing unit chip with 2.5D and 3D packaging technology.'

The revised descript:

'However, due to charge sharing operation and the requirement for additional capacitors, 1T1C eDRAM suffers from limited voltage scaling down, destructive reading, and complex capacitor fabrication[27-30]*.'*

The detailed revision is in the last sentence on the first paragraph of the Introduction part on page 3 of the revised manuscript.

Comment 5:

Comparison Table: To help illustrate the benefits of this eDRAM platform, the authors should prepare a summary table comparing their performance against other emerging eDRAM paradigms. I would suggest some key metrics in the table should include (but not limited to): device structure (e.g. other 2T-eDRAM, some 1T-1C), speed (ns), retention or refresh rate, ION/IOFF ratio, density or bit cell size (n F2), channel materials (compare some oxide channels, poly-Si, 2D), and BEOL compatibility.

Response:

Thank you for your suggestions. We have supplemented the benchmark table to comprehensively compare our device with other relevant works, including all-Si, all-MoS_2, and AOS based 2T-eDRAMs, as shown in Table RI, and following factors are considered in our table:

1. Device structure, which determines its scalability.
2. Device materials, which determines process compatibility.
3. Write speed (write pulse width) of the device.
4. Retention time of the device.
5. OFF current and ON current of the write transistor, where the OFF current affects retention time and the ON current affects write speed.

6. ON current of the write transistor, which affects the sense margin.
7. Sense margin of the device. A larger sense margin is advantageous for distinguishing 0 and 1 states.
8. Additional lithography, which represents the process cost compared to the traditional all Si 2T-eDRAMs.
9. Process compatibility, which includes the BEOL compatibility.
10. Feature size and bit cell size, considering density is influenced not only by the device size itself but also by metal interconnect layout. For instance, in 1T1C cells, the transition from $8F^2$ to $6F^2$ primarily involves changes in wiring rules, while achieving $4F^2$ mainly through capacitor and transistor stacking. Therefore, for most single-device studies, we added a feature length option to indicate device scalability, aiding in illustrating its achievable density.

TABLE RI

Summarizes of The Major Parameters of Other Typical Related Work

Reference	2016[1]	2016[2]		2021[3]		2008[4]	2020[5]	2023[6]	2022[8]	2023[9]	2023[10]	This Work	
Structure	1T1C	1T1C	2T0C	1T1C	2T1C	2T0C	2T0C	2T0C	2T0C	Stacked 2T0C	Stacked 2T0C	Planer 2T0C	Stacked 2T0C
Material	Si	MoS_2		MoS_2		Si	IWO	ITO	IGZO	IGZO	IGZO	Si- MoS_2	
Write pulse width	8.75ns	0.2ms	-	20ms	140ms	8ns	3ns (simulation)	100 ns	10ns	-	5ns	5ns/1ns(simulation)	
Retention time	64ms	>251ms	>1s	>10s	>100s	~5us	1-10s	2250 s	>7000s	20s	75s	1000s(2L) 6000s(1L)	>1000s/ 65s(simulation)
$I_{OFF\ W}$ (A/μm)	-	10^{-15}-10^{-18}		<10^{-13}			10^{-15}	4×10^{-19}	<6×10^{-20}	-	<10^{-13}	3.2×10^{-18}(2L), 5.3×10^{-19}(1L)	
$I_{ON\ W}$ (A/μm)	-	10^{-6}		10^{-7}-10^{-8}		-	10^{-4}	22.6×10^{-6}	24×10^{-6}	-	10^{-5}– 10^{-6}	6.31×10^{-6}	
$I_{ON\ R}$ (A/μm)												166×10^{-6}	
Sense margin (μA/μm)	-	-		-	<0.01	-	-	-	~27		≤10	35	20
Additional lithography	-	-		-	-	-	1	-	-	4	4	4	
Compatibility	-	BEOL		BEOL		CMOS	BEOL	BEOL	BEOL	BEOL	BEOL	BEOL	
Feature size	1x (19-17nm) $6F^2$	0.5μm		20μm		50nm	50nm	50nm	70nm	75nm $4F^2$	65nm $4F^2$	3μm (10nm in simulation) $4F^2$ for stacked 2T0C	
"-" represents that the data is not available.													

Reviewer #5：

In this paper, the authors demonstrate a 2T gain-cell eDRAM using a hybrid MoS_2 write transistor/Si read transistor scheme, leveraging the low off-current of MoS_2 FET and the high on-current of Si transistor to achieve long retention and short read time, and demonstrates the potential of 3D stacking for even higher density. The eDRAM exhibits an excellent retention up to 6000 s and sense margin up to 40 μA/μm. Overall, the work is impressive and demonstrates a highly intriguing application of 2D materials for embedded memory, and it should merit publication in Nature Communication eventually. However, there are still several points that the reviewer would like to see the authors revise/clarify before a recommendation could be made:

Response:

Thank you very much for taking the time to review our manuscript. We are very encouraged by these positive comments on our work. In response to your constructive comments and suggestions, we have carefully made modifications and marked them in red in the revised manuscript. The modifications are indicated with red strikethroughs for deletions and yellow highlights for additions in the revised manuscript. And the detailed responses are listed below, which we hope can address your comments and suggestions.

Comment 1:

In the Introduction, the authors claim that compared with 2D material channel, amorphous oxide semiconductors suffer from low mobility and on-current due to percolation transport when V_{th} is shifted to the right. However, a recent paper on IEDM 2022 (Qianlan Hu, Qijun Li, Shenwu Zhu, Chengru Gu, Shiyuan Liu, Ru Huang and Yanqing Wu, "Optimized IGZO FETs for Capacitorless DRAM with Retention of 10 ks at RT and 7 ks at 85 °C at Zero Vhold with Sub-10 ns

Speed and 3-bit Operation," IEDM 2022, 26.6) demonstrates IGZO FETs for GC-eDRAM with very good performance, including an extremely low off-current of 6e-20 A/μm and a decently high on-current of 24 μA/μm at Vds=1V and Vg=V_{th}+1V, which is arguably even better than the MoS_2 FET in this work. In addition, apart from amorphous oxide semiconductors, there are also demonstrations of crystalline oxide semiconductors such as c-axis-aligned crystalline IGZO (CAAC-IGZO). Therefore, the reviewer suggests the authors tone down the statement, and also include the work mentioned above in the benchmark.

Response:

We are truly grateful for your kind reminders and suggestions. Qianlan Hu et al. have demonstrated an outstanding work based on IGZO 2T-eDRAM, especially with the long retention extended to 10,000 seconds. We have cited the work and incorporated it into our benchmark. In comparison, the proposed heterogenous Si-MoS_2 2T-eDRAM benefits from the higher mobility of silicon, offering the advantages of a higher sense margin and a higher on-state current for the read transistor. For example, the extracted sense margin of the IGZO 2T-eDRAM in the reference is around 27μA/μm while the sense margin of proposed device is 35μA/μm in a much larger channel length. For device with advanced Si CMOS technology, thanks to its high on-state current, the sense margin can be further augmented to the level of 0.58 mA/μm, as predicted by the calibrated simulation results shown in Figure R21.

We have also corrected our inappropriate description of amorphous oxide semiconductors. The specific modifications made are as follows:

'Nonetheless, AOS materials exhibit relatively low carrier mobility, leading to a reduced transistor on-state current. This results in narrow sense margin. Methods including Oxygen plasma annealing, reducing channel width, ultrathin film channels, and dual or triple gate electrostatic control have been proposed to optimized performance, albeit at the cost of additional processing steps or more complex fabrication[31-34].'

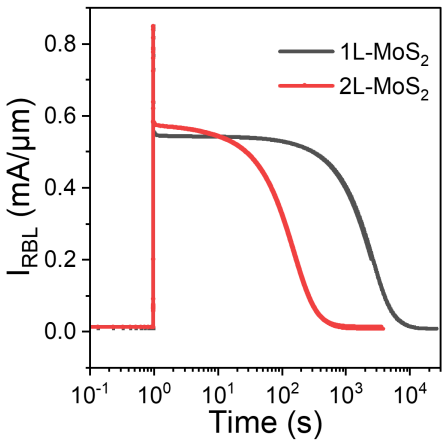

Figure R21. The retention characteristc of the simulated Si-MoS_2 2T-eDRAM. The device features high sense margin thanks to the high mobility of Si read transistor. The simulated sense margin is 0.58mA/μm and 0.55mA/μm for 2L and 1L device respectively. The difference of sense margin of different layer device is due to varying amounts of written charge caused by different write current under the same write pulse width (10 ns).

Comment 2:

The authors mentioned in the Introduction "As the size of the transistor scales down, the storage capacitance is reduced and the leakage current of the write transistor increases due to short channel effect (SCE). This significantly degrades the data retention of the GC-eDRAM to the level of microsecond." That said, the authors use very large size transistors (several μm) for their demonstration. Although it's understandable for an experimental prototype, the reviewer suggests the authors project the memory performance with scaled dimensions.

Response:

Thanks for the thoughtful suggestions. To better predict the scaling ability of the device, we used the Sentaurus TCAD simulation to forecast the scaling prospects of the device. Shockley-Read-Hall thermal generation-recombination with doping-dependent and lateral electric field-related carrier lifetime, and a multivalley orientation-dependent model were employed. The model parameters are calibrated based on existing experimental data to ensure accurate prediction. The simulated device features a 10nm

gate length for both write and read transistors. It shows significant improvement of sense margin. Though the retention of miniatured device is reduced significantly compared to the larger-scale devices demonstrated experimentally, a retention time up to 65 s for Si-2L MoS_2 2T-eDRAM is still achieved, which is enough for eDRAM application, as shown in Figure R22 (Supplementary Figure 12-13 in the revised supplementary information).

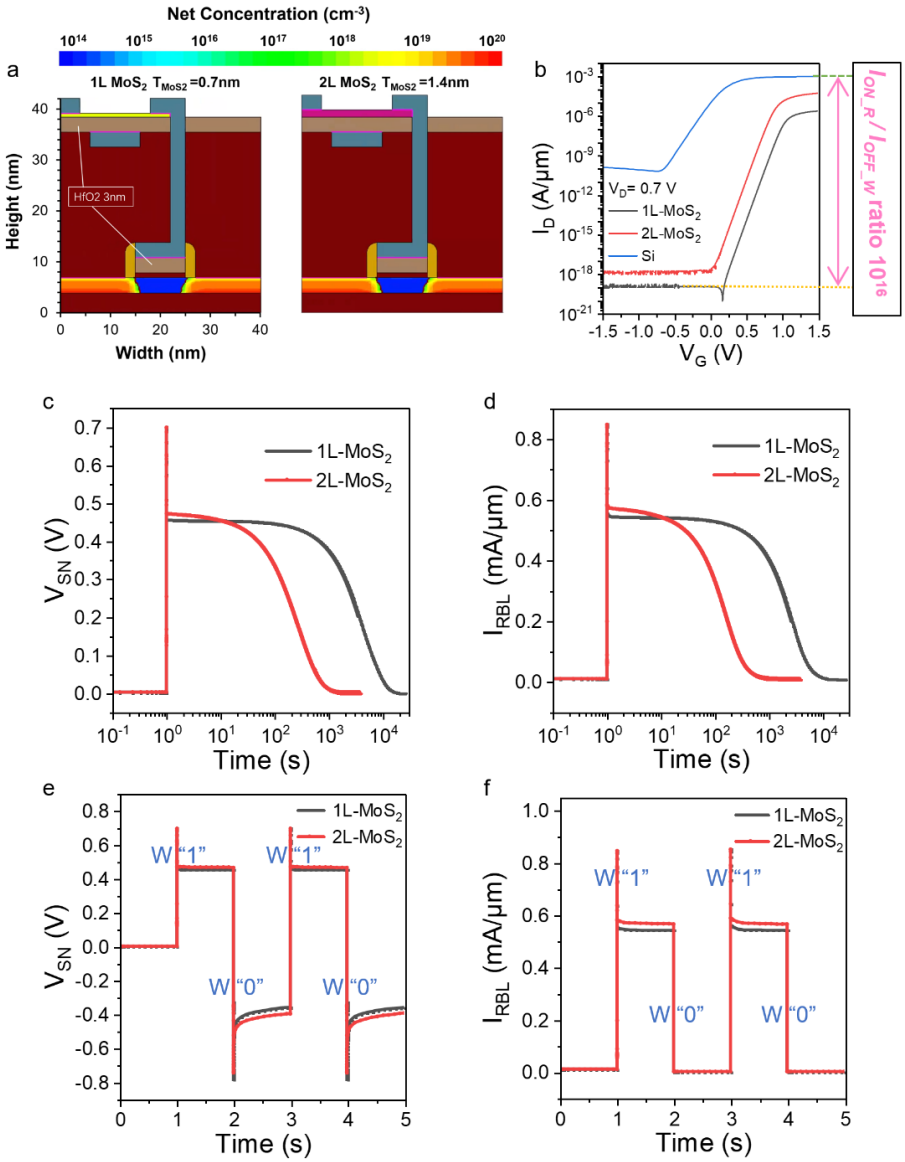

Figure R22. TCAD simulation results of the Si/MoS_2 FETs. a. Simulated device with 10 nm gate-length Si-MoS_2 2T-eDRAM. **b.** The simulated transfer curves of the MoS_2 /Si nFET at same V_D =0.7 V. **c**. V_{SN} -Time characteristics and **d.** I_{RBL} -Time characteristic after writing 1 (V_{WBL}= 0.7 V) of the simulated 2T-eDRAM. **e.** V_{SN} and **f.** I_{RBL} waveforms in "Write 1-Read 1-Write 0-Read 0" Timing sequence.

Comment 3:

*(Continuing from the comment above) judging from the fact that in Fig. 3g, even the full-Si eDRAM also exhibits a rather long retention of several seconds, it has to be concluded that the long retention time of MoS_2-Si hybrid eDRAM can at least be partially attributed to the large gate capacitance of the Si read transistor with a large μm size. If the device dimensions were scaled down to ~10nm, the capacitance (proportional to W*L) would be reduced by ~6-7 orders of magnitude and so would the retention, unless the off-state current can also be scaled accordingly, yet the raw off-current (before width normalization) would only reduce by ~3 orders of magnitude. The reviewer suggestes the authors address the issue by further reducing the off-state current or show a viable path for doing so (the 1L MoS_2 in SI seems to be in the right direction, but the on-state performance need serious improvement).*

Response:

We greatly appreciate the valuable suggestions from the reviewer. Your recommendations align perfectly with our ideas and represent our future research directions. Considering the reduced retention time as devices shrink, we have conducted TCAD simulation to investigate it. As shown in Figure R23. a, the device features 10nm gate length for both top MoS_2 FET and bottom Si FET. As the gate length decreases from 3μm in experiment to 10nm in simulation, and gate dielectric thickness decreases from 20 nm to 3 nm, the gate capacitance decreases by approximately 1-2 order of magnitude (The width is normalized to 1 μm aligning with the off state current density of write transistor). Indeed, due to process limitations in the gate dielectric depositing, the capacitance density measured in experiments for the same thickness is lower than the simulated results. Figures R23. b and c depict the measured C_{SN} in large size and simulated C_{SN} in small size. Considering the insignificant short-channel effects in MoS_2 transistors and further optimization of the write transistor, we reasonably assume that the OFF current of MoS_2 transistors remains low at small sizes. As the simulation results

shown in Figure R23. d, the retention time of Si-2L MoS_2 decrease to 65 s, while the Si-1L MoS_2 remain >1000s long retention time. Meanwhile, in small size, the on-current of write transistors based on 1L MoS_2 can be effectively enhanced, while the reduced capacitance of storage nodes facilitates high write speeds. As shown in Figure R23.e, the Si-1L MoS_2 in small size demonstrates high write speed. This provides further validation for our research direction.

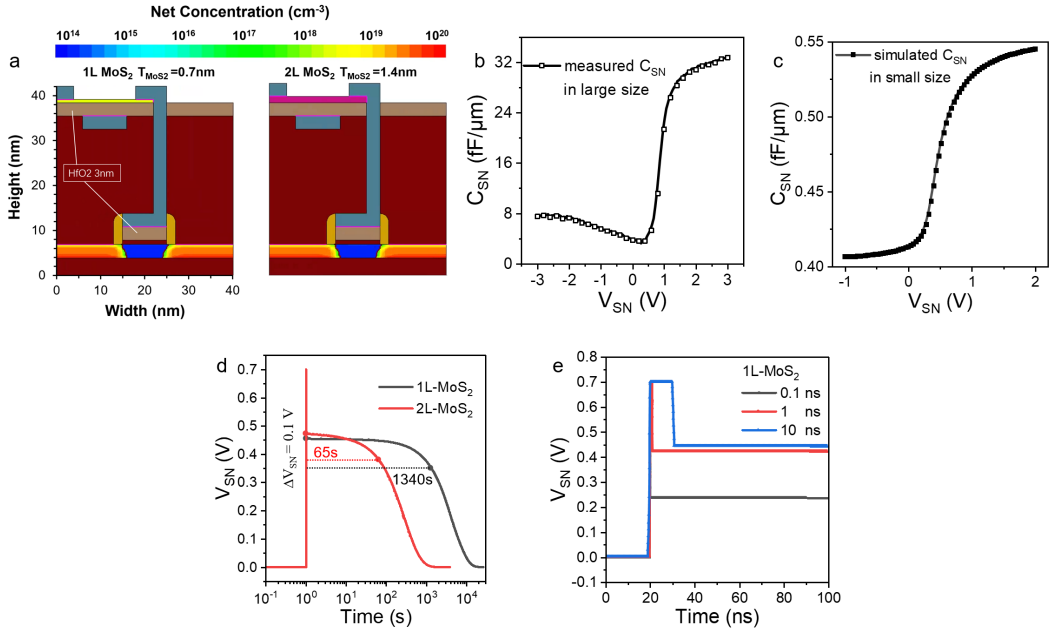

Figure R23. a. The simulated device structure in small size. **b.** The measured C_{SN} in large size. **c.** The simulated C_{SN} in small size. **d.** The simulated retention characteristic of Si-1L MoS_2 and Si-2L MoS_2 eDRAMs. **e.** The simulated result for Si-1L MoS_2 2T-eDRAM in various pulse width.

Comment 4:

The long retention and low off-current of 3.9e-18 A/um in Fig. 3d is achieved at V_WWL=-1V, which is also the exact same thing the authors argued against in the Introduction ("Moreover, it is noted that AOS achieves extremely high retention time only when an additional negative holding voltage is applied on the gate of the write transistor to reduce leakage"; and to be fair, some works such as the IEDM 2022 paper mentioned above have already achieved long retention with zero hold voltage, therefore the statement should be revised). The authors should at least discuss viable solutions to shift V_{th} to more positive

voltages to achieve long retention at zero hold voltage (again, the 1L MoS_2 in Si seems to be in the right direction, but the on-state performance need serious improvement).

Response:

We have conducted a thorough literature review and revised the erroneous description of AOS accordingly. The revised content is as follows (the sentences with red strikethroughs are deleted in the revised manuscript):

'~~*Moreover, it is noted that AOS achieves extremely high retention time only when an additional negative holding voltage is applied on the gate of the write transistor to reduce leakage of stored charges. When the holding gate voltage moves to 0V, the leakage OFF current of the AOS transistor gets high due to its intrinsically low threshold voltage (V_{th}), which leads to the data retention time to decrease exponentially when as the holding gate voltage is 0V. This can be optimized by Oxygen plasma annealing, reduced channel width, ultrathin film channels, and dual or triple gate electrostatic control*[31-34].~~ *Methods including Oxygen plasma annealing, reducing channel width, ultrathin film channels, and dual or triple gate electrostatic control have been proposed to optimize performance, albeit at the cost of additional processing steps and more complex fabrication*[31-34].'

And we appreciate the reviewer's recognition of the significance of more positive V_{th}.

As suggested by the reviewer, in order to achieve a longer retention time when V_{hold} is 0, it is essential to have a positively shifted threshold voltage (V_{th}) of the T_{write}. A positive shift of the V_{th} can be achieved by suppressing the N-type doping of the transistor. Defects at the interface of MoS_2 transistors, including sulfur vacancies in the channel, oxygen vacancies in the dielectric layer, and residual impurities resulting from the fabrication process, are the sources of doping. Additionally, the barrier in the contact region also affects the threshold voltage. More positive shift in V_{th} can be achieved by reducing the defects in the transistor, suppressing the effect of N-type doping, and increasing the contact region barrier. The following solutions for the MoS_2 transistors

under consideration are promising:

1. The formation of sulfur vacancy defects in the channels can be attributed to two primary factors: insufficient growth and the introduction of damage during the process. The formation of sulfur vacancies can be prevented during the growth stage by employing low-temperature MOCVD growth of MoS_2 or growth in sulfur-rich environments (e.g., an H_2S atmosphere)[35]. Additionally, sulfur vacancies at the interface can be diminished through annealing with sulfur-containing gases and by immersion in chemical solvents such as H_2O_2, (3-aminopropyl) triethoxysilane, etc.[36-38]. Positive shift of Vth can also be achieved by mild plasma treatment, for example, using PH_3, N_2 atmosphere to fill the sulfur vacancies[39,40].

2. Defects in the dielectric layer interface, such as oxygen vacancies, also provide electrons to the MoS_2, leading to N-type doping[41] Passivation of oxygen vacancies can be achieved by means of O_2 annealing and plasma oxygen treatment of the dielectric or seed layers of the device[42].

3. Following the completion of the process steps, the surface of MoS_2 can be cleaned by high-vacuum, inert-gas high-temperature annealing in order to avoid the presence of organic residues throughout the process. Furthermore, as the MoS_2 surface will be exposed to the atmosphere due to the transfer method used for device preparation, the adsorption of air impurities that could affect the V_{th} can be prevented by encapsulation (such a hBN), thereby enhancing the device's stability.

4. The contact between the source-drain electrode and the 2D material can be formed by means of vDW transfer and alloying [43]. By eliminating the Fermi pinning in the contact region, it is possible to modulate the contact barrier, which in turn shifts the device threshold voltage and reduces the leakage current.

We would like to express our gratitude to the reviewer for insightful comments on our monolayer MoS_2 devices. In response to your feedback, we are striving to further reduce the contact resistance of monolayer MoS_2 and enhance the ON current without the shift of V_{th} by optimizing the transfer method, adopting a mild contact and a more

suitable contact metal.

Comment 5:

Apart from retention and read margin, the authors should also comment on the write performance of the eDRAM.

Response:

Thank you for highlighting the write performance of the eDRAM. The write performance of the eDRAM is discussed in Figure 3 and the '**High performances of Si-MoS_2 2T-eDRAM'** part on page 13-15 of the revised manuscript. The experimental results is depicted in Figure R24 (Figure 3e and f in the revised manuscript) and detailed discussion are as follows:

"Concurrently, we performed a write-speed test for the 2T-eDRAM. In an ideal scenario, the amount of charge stored in SN node is determined by the ON current of the write FET and the write pulse time. Following a 5 ns write pulse (the limit of our testing apparatus), the I_{RBL} response for data "0" and data "1" exhibits a current difference exceeding a three orders of magnitude difference. The high sensing margin of Si FETs also results in different current levels of the read FET at different write times ranging from 5 ns to 200 ns, which can be utilized for multibit storage. Throughout the 100 ms measurement period, the output current (I_{RBL}) clearly exhibits distinct levels and remains stable. This significant state difference enables the potential for multi-level retention capability within the 2T-eDRAM, as illustrated in Fig. 3e. The variation of I_{RBL} saturates with write pulse longer than 100 ns, due to the full charge of the storage node, as shown in Fig. 3f."

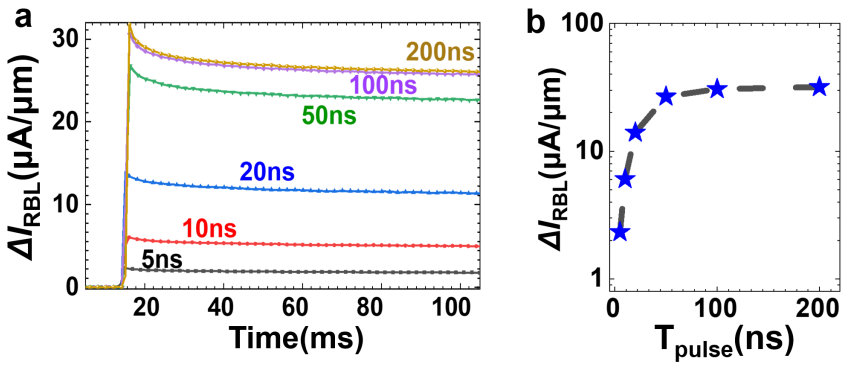

Figure R24 a. I_{RBL} -Time characteristics after writing 1 with pulse width ranging from 5ns to 200ns. **b.** Relation between ΔI_{RBL} and pulse width

Comment 6:

A prior work on using MoS_2 FET with ultra-low leakage for DRAM application (ACS Nano 2016, 10, 9, 8457–8464) should be included (although it's 1T1C DRAM).

Response:

Thank you for your suggestion. We have thoroughly reviewed and referenced the paper, and it has been included in our comparison table, as shown in the second column (Highlight with green background pattern) in Table RI.

TABLE RI

Summarizes of The Major Parameters of Other Typical Related Work

Reference	2016[1]	2016[2]		2021[3]		2008[4]	2020[5]	2023[6]	2022[8]	2023[9]	2023[10]	This Work	
Structure	1T1C	1T1C	2T0C	1T1C	2T1C	2T0C	2T0C	2T0C	2T0C	Stacked 2T0C	Stacked 2T0C	Planer 2T0C	Stacked 2T0C
Material	Si	MoS_2		MoS_2		Si	IWO	ITO	IGZO	IGZO	IGZO	Si- MoS_2	
Write pulse width	8.75ns	0.2ms	-	20ms	140ms	8ns	3ns (simulation)	100 ns	10ns	-	5ns	5ns/1ns(simulation)	
Retention time	64ms	>251ms	>1s	>10s	>100s	~5us	1-10s	2250 s	>7000s	20s	75s	1000s(2L) 6000s(1L)	>1000s/ 65s(simulation)
$I_{OFF\ W}$ (A/μm)	-	10^{-15}-10^{-18}		<10^{-13}			10^{-15}	4×10^{-19}	<6×10^{-20}	-	<10^{-13}	3.2×10^{-18}(2L), 5.3×10^{-19}(1L)	
$I_{ON\ W}$ (A/μm)	-	10^{-6}		10^{-7}-10^{-8}		-	10^{-4}	22.6×10^{-6}	24×10^{-6}	-	10^{-5}– 10^{-6}	6.31×10^{-6}	
$I_{ON\ R}$ (A/μm)												166×10^{-6}	
Sense margin (μA/μm)	-	-		-	<0.01	-	-	-	~27		≤10	35	20
Additional lithography	-	-		-	-	-	1	-	-	4	4	4	
Compatibility	-	BEOL		BEOL		CMOS	BEOL	BEOL	BEOL	BEOL	BEOL	BEOL	
Feature size	1x (19-17nm) $6F^2$	0.5μm		20μm		50nm	50nm	50nm	70nm	75nm $4F^2$	65nm $4F^2$	3μm (10nm in simulation) $4F^2$ for stacked 2T0C	
"-" represents that the data is not available.													

Reviewer #6

(Remarks to the Author):

I co-reviewed this manuscript with one of the reviewers who provided the listed reports. This is part of the Nature Communications initiative to facilitate training in peer review and to provide appropriate recognition for Early Career Researchers who co-review manuscripts.

Response:

We sincerely appreciate the reviewer for taking the time to review the manuscript. We have carefully rechecked and revised the article. The modifications are indicated with red strikethroughs for deletions and yellow highlights for additions in the revised manuscript. We believe the revised article now better meets the publication requirements of Nature Communications.

Reference:

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REVIEWERS' COMMENTS

Reviewer #1 (Remarks to the Author):

Minor revisions needed:
1. It might only happen on my side that the x,y axis titles in Supplementary Figure 3 cannot be seen. The figure legends are also missing. Please make sure that they are properly shown in the final version.

Reviewer #2 (Remarks to the Author):

I co-reviewed this manuscript with one of the reviewers who provided the listed reports. This is part of the Nature Communications initiative to facilitate training in peer review and to provide appropriate recognition for Early Career Researchers who co-review manuscripts.

Reviewer #4 (Remarks to the Author):

The authors have sufficiently addressed all my concerns. I can know fully recommend for publication in Nature Communications as-is.

-Suraj Cheema

Reviewer #5 (Remarks to the Author):

In the revised paper, the authors performed an extensive TCAD simulation of Si-eDRAM 2T0C eDRAM with scaled dimensions and more ideal material properties. Most of my comments from previous round of review have been addressed satisfactorily. I would suggest adding Si-AOS hybrid eDRAM as another candidate to combine the merit of two different material systems somewhere in the article. Other than that, I have no further comments and recommend publication.

Reviewer #6 (Remarks to the Author):

I co-reviewed this manuscript with one of the reviewers who provided the listed reports. This is part of the Nature Communications initiative to facilitate training in peer review and to provide appropriate recognition for Early Career Researchers who co-review manuscripts.

Authors' responses to the reviewers' comments

Reviewer #1:

Minor revisions needed:

1. *It might only happen on my side that the x,y axis titles in Supplementary Figure 3 cannot be seen. The figure legends are also missing. Please make sure that they are properly shown in the final version*

Response:

We sincerely appreciate the reviewer for thoroughly reviewing our manuscript. We carefully checked the manuscript with both PDF and word version. The issue of miss legends in Supplementary Figure 3 in the previous version may happened in the word-pdf transform process. We have checked the final manuscript and make sure it won't happened again. Great thanks again.

Reviewer #2:

I co-reviewed this manuscript with one of the reviewers who provided the listed reports. This is part of the Nature Communications initiative to facilitate training in peer review and to provide appropriate recognition for Early Career Researchers who co-review manuscripts.

Response:

We sincerely appreciate the reviewer for taking the time to review our manuscript. The positive feedback from the reviewers has encouraged us greatly. Once again, thank you, and best wishes.

Reviewer #4 :

The authors have sufficiently addressed all my concerns. I can know fully recommend for publication in Nature Communications as-is.

-Suraj Cheema

Response:

We sincerely appreciate the reviewer for taking the time to review our manuscript. Your positive feedback has greatly encouraged us and reaffirmed our efforts in this research. We are truly grateful for your insightful comments and suggestions, which have helped us improve our work. It is always motivating to receive such constructive criticism from knowledgeable peers. Thank you once again for your valuable insights and support throughout this process.

Reviewer #5 :

In the revised paper, the authors performed an extensive TCAD simulation of Si-eDRAM 2T0C eDRAM with scaled dimensions and more ideal material properties. Most of my comments from previous round of review have been addressed satisfactorily. I would suggest adding Si-AOS hybrid eDRAM as another candidate to combine the merit of two different material systems somewhere in the article. Other than that, I have no further comments and recommend publication.

Response:

Thanks for the great suggestion from the reviewer. We have added a discussion about Si-AOS hybrid eDRAM in the last sentence of the discussion part on page 17 in the final manuscript. The detailed description is :

Meanwhile, the core idea of combining the merits of two different material systems, utilizing innovative materials with low OFF current as write transistors and mature silicon with high ON current as read transistors, marks a significant milestone for

memory technology, offering insights for more heterogeneous DRAM candidates, such as Si-2D and Si-AOS hybrid DRAMs.

Reviewer #6

(Remarks to the Author):

I co-reviewed this manuscript with one of the reviewers who provided the listed reports. This is part of the Nature Communications initiative to facilitate training in peer review and to provide appropriate recognition for Early Career Researchers who co-review manuscripts.

Response:

We sincerely appreciate the reviewer for taking the time to review our manuscript. Your positive feedback has greatly encouraged us and reaffirmed our commitment to this research. We are truly grateful for your insightful comments and suggestions, which have significantly contributed to enhancing the quality of our work. It is incredibly motivating to receive such constructive criticism from someone with your expertise. Thank you once again for your valuable insights and support during this process.