nature portfolio

Peer Review File

Multifunctional 2D FETs Exploiting Incipient Ferroelectricity in Freestanding SrTiO3 Nanomembranes at Sub-Ambient Temperatures

Corresponding Author: Professor Saptarshi Das

This file contains all reviewer reports in order by version, followed by all author rebuttals in order by version.

Version 0:

Reviewer comments:

Reviewer #1

(Remarks to the Author)
This manuscript demonstrates ferroelectric field-effect transistors (FeFETs) by stacking large-area STO nanomembranes and a monolayer MoS2 film. These devices exhibit excellent ferroelectric properties with ultra-fast polarization switching, low-switching voltage, long nonvolatile retention, and competitive endurance. In addition, these devices have the ability to store 64 distinct synaptic weights or 6-bit memory storage at 100 K. Furthermore, these devices present not only an impressive nonvolatile polarization switching up to 200 K but also a functional adaptability by transitioning from an artificial synapse to a neuron based on temperature-dependent memory retention characteristics. These results are meaningful and impressive, and the manuscript was well organized. Therefore, it can be published after the following revisions:
Below are the detailed comments:
1. Why choose 80 nm STO nanomembranes in this manuscript? Have you compared the performance of STO with other thicknesses (such as 100 nm, 50nm)? From the characterization results in Figure 1, it can be seen that the quality of the grown STO film is relatively good. How large is the area of the film that can maintain its good quality? What's the advantages of STO over HZO (Advanced Functional Materials, 2020, 2003859)?
2. There are two gates in Figure 2b, which do not seem to correspond to the device schematic of Figure 2a. The authors claim that the mean value for subthreshold slope (SS) of these STO-gated MoS2 FETs is 220 mV/decade. For ferroelectric transistors, why is this SS so large?
3. From Figure 3a, it can be seen that the hysteresis window is relatively small. It is suggested to add the Ig-Vg curve to further prove that the hysteresis window is caused by ferroelectric polarization?
4. Why are the trends of HCS and LCS different as the switching time changes in Figure h? Especially, why does LCS significantly decrease below 102 ns? Can the multistate characteristics be applied for other types neuromorphic computing, e.g., reinforcement learning (Advanced Materials, 2022, 2107754-1-11)?
5. The authors claim that the projected retention was found to be more than 10 years. How did they draw this conclusion?

Reviewer #2

(Remarks to the Author)
The work proposed by the authors deal with the integration of single-crystalline STO nanomembranes with monolayer MoS2 films to target back end of line (BEOL) compatible FeFETs, demonstrating rapid polarization switching, nonvolatile retention, and notable endurance within a low thermal budget. There is a certain novelty in the work and a large number of very interesting experimental results and their interpretations. But finally, the paper fails to demonstrate that the expected good properties of FeFETs based on single-crystalline STO nanomembranes with monolayer MoS2 films are maintained at room temperature. Indeed, the goal of building neuromorphic hardware integrated on CMOS needs room temperature operation and this is the main roadblock that the paper is not solving. The study remains interesting and valuable but the main claim that would generate true impact for a paper in Nature journal is finally not full achieved neither a clear path about what optimization could be clearly foreseen to address this gap.
Therefore, a number of important questions that the authors should carefully address before any consideration for publication, remain as it follows:

1) Most important: the authors essentially demonstrate useful STO-gated MoS2 FeFETs with nonvolatile polarization switching up to 200 K, with the performance degrading with increasing temperature (best performance reported rather at 100K - STO-gated MoS2 FeFET at T = 100 K in Fig. 4). The authors also conclude that Increasing the temperature leads to increased thermal fluctuations, that accelerate the destabilization of the polar order, a thermal decay of ferroelectricity in their material devices. A neuromorphic chip at 100K is certainly not very attractive for Edge AI applications. What mechanism engineering the authors think can be used to bring such polar order usable at room temperature and, especially, what proof they have this can be controlled, optimized and used in building efficient/competitive synapses and neurons operating at room temperature? Otherwise the study remains of interest but the impact is significantly reduced.

2) The authors essentially performed experiments of ferroelectric behavior and retention on transistor like structures. Building and testing, for instance, dedicated capacitive structures with STO membranes of various thicknesses on 2D semiconducting films could offer very interesting proof and insights into the retention mechanisms, together with the extraction of some key data from the ferroelectric capacitors such remnant polarization, coercive fields, and leakage. This information of such key parameters in not explored and not reported sufficiently in the paper. Measuring the characteristics of fabricated FETs based on freestanding membranes on 2D channels is certainly a great achievement but complementary characterization and confirmation of quantitative ferroelectric figures of merit and their degradation with temperature, appears as a must for publication. In addition, the authors can try to perform PFM measurements on the 3D STO membranes, as another complementary experiment aiming at ferroelectricity characterization.

3) It would be also of interest to extract and discuss the variability of transfer characteristics ID-VG (like in Fig. 2 (f)) and the related hysteresis as a function of temperature and derive a semi-quantitative physics-based model to explained the observed dependency. The authors have here the good points that they have a statistical testing on micrometer scale devices, with variability attributed to residues and wrinkles introduced during the 3D and 2D membrane transfer processes involving PDMS and PMMA. Have the authors double-checked the uniformity of the thickness of the membranes and interfacial defects to exclude them as source of variability?

4) Finally, as there are many new candidate technologies for FeFETs for building neuromorphic blocks as synapses and neurons, with many of them operating already at room temperature, a table comparing the main merits of the proposed device architecture with other technologies will be useful, at least as additional material.

Reviewer #3

(Remarks to the Author)
The manuscript "Stacking of Ferroelectric and Freestanding 3D SrTiO3 and 2D MoS2 Nanomembranes for Reconfigurable Neuromorphic Hardware" by D Sen et al. presents a compelling exploration of ferroelectricity in freestanding SrTiO3 (STO) nanomembranes, integrated with monolayer MoS2 to develop reconfigurable neuromorphic devices. The study is timely, and the combination of complex oxides with 2D materials for non-volatile systems addresses current challenges in neuromorphic applications. Indeed, the manuscript explores a cutting-edge area, where freestanding nanomembranes of 3D single crystals, particularly STO, are combined with 2D materials like MoS2 for neuromorphic devices. The quality of the devices presented in the manuscript is commendable. The reported ultra-fast polarization switching, low-switching voltage, nonvolatile retention, and endurance metrics make the proposed STO-gated MoS2 FeFETs promising for practical applications. The reconfigurable neuromorphic device functionality is particularly appealing.The manuscript highlights the potential of integrating these materials into the back end of silicon complementary metal oxide semiconductor technology (due to the low temperature needed in the fabrication process), opening up opportunities for addressing challenges associated with compute-in-memory architectures and neuromorphic applications.

The main weakness lies in the description of the state-of-the-art in the introduction. The references provided by the author are not comprehensive, and several relevant works about the isolation of freestanding perovskite oxide layers and the combination of perovskite oxides with MoS2 and other semiconductors, which may have been consulted by the authors, are not mentioned. Improving the introduction by incorporating these references would enhance the overall quality of the manuscript.

Version 1:

Reviewer comments:

Reviewer #1

(Remarks to the Author)
The authors have responsed the reviewers' questions in a satisfactory manner. It is suitable for the publication.

Reviewer #2

(Remarks to the Author)
The paper is well-written and presents clear novelty in both material and device research. The experiments and discussions are very informative. However, it is clear that this is not yet a technology ready for neuromorphic computing at room temperature. The cryogenic performance of STO-based FeFETs is very good. Nonetheless, the applicability of this

technology for mainstream memory applications remains limited unless further important improvements can be achieved at room temperature.

*Comment and Question #1:
Lack of Room Temperature Synaptic Operation – Neuromorphic computing hardware for autonomous systems requires operation at room temperature. While the authors' demonstration of pseudo-nonvolatile polarization switching at room temperature is noteworthy, the absence of stable ferroelectricity at 300 K significantly weakens the overall impact of the work, especially for edge AI applications.
Question #1: How do the authors plan to address in the future the instability of ferroelectric domains in STO at room temperature? Can the authors elaborate more on what specific strategies or mechanisms do they plan to pursue to ensure room temperature synaptic operation in future work? Including more discussion on this direction may help compensate for the lack of room-temperature data. I would also suggest reflecting this in the paper's title to avoid any misleading impressions. Something along the lines of "Multifunctional 2D FETs Exploiting Incipient Ferroelectricity in Freestanding $SrTiO_3$ Nanomembranes at Sub-Ambient Temperatures" might be more appropriate.
*
Comment and Question #2:
Material and Device Characterization at Varying Temperatures and Thicknesses – More systematic characterization of the material and device performance, especially in terms of hysteresis at varying temperatures and thicknesses, would help elucidate the scaling limits of these parameters.
Incorporating more details on key ferroelectric parameters, such as remnant polarization, coercive fields and leakage over varying thickness and temperature, could significantly strengthen the manuscript. This would offer a clearer picture of the ferroelectric properties and their degradation with respect to thickness and temperature. Such an analysis should also include a discussion on how variations in membrane thickness uniformity and interfacial defects could impact electrical characteristics and hysteresis.
Question #2: Based on such an analysis, can the authors better elaborate on the scaling limits of their proposed freestanding 3D $SrTiO_3$ and 2D MoS_2 nanomembranes for neuromorphic hardware, particularly with respect to thickness, voltage, and temperature? I appreciate that the authors have already compared their material and devices with the state of the art in table, which is a very good and convincing step.

*Comment and Question #3:
Demonstrating Neuromorphic Functionality at Low and Room Temperatures – It would be helpful if the authors could more convincingly support neuromorphic functions of the STO-gated MoS_2 FET at both low and room temperatures.
Question #3: I appreciate the authors' effort in exploiting room-temperature non-retentive polarization switching in the STO-gated MoS_2 FET to construct a physical reservoir for accelerating reservoir computing (RC). As the authors have shown excellent retention and ferroelectric behavior at 100 K, could they also demonstrate whether the STO-gated MoS_2 FET can provide potentiation and depression current plots for use as a synaptic ferroelectric device at 100 K? Have the authors attempted such experiments to strengthen their claim for neuromorphic hardware, even if the device only works at low temperatures? A bit more detailed and critical description and discussion of the potential applications, if any, of the proposed material not limited to RC, would be useful.

Reviewer #3

(Remarks to the Author)
The authors revision of the state of the art in the introduction, although improved, is still lacking quite some breakthroughs in this field.

Version 2:

Reviewer comments:

Reviewer #2

(Remarks to the Author)
I am satisfied by all the answers and corrections made by the authors, especially as now, the title: "Multifunctional 2D FETs Exploiting Incipient Ferroelectricity in Freestanding $SrTiO_3$ Nanomembranes at Sub-Ambient Temperatures" includes the "sub-ambient" keyword, which is reflecting well the status of the technology.
I recommend the paper for publication in current form.

Reviewer #3

(Remarks to the Author)

Reviewer#1:

This manuscript demonstrates ferroelectric field-effect transistors (FeFETs) by stacking large-area STO nanomembranes and a monolayer MoS2 film. These devices exhibit excellent ferroelectric properties with ultra-fast polarization switching, low-switching voltage, long nonvolatile retention, and competitive endurance. In addition, these devices have the ability to store 64 distinct synaptic weights or 6-bit memory storage at 100 K. Furthermore, these devices present not only an impressive nonvolatile polarization switching up to 200 K but also a functional adaptability by transitioning from an artificial synapse to a neuron based on temperature-dependent memory retention characteristics. These results are meaningful and impressive, and the manuscript was well organized. Therefore, it can be published after the following revisions:

The authors appreciate the reviewer's encouraging comments. We highly value your recognition of our significant and impressive findings on the development of a 2D FET using freestanding STO membranes. Note that the abstract and the introduction of the manuscript has been thoroughly revised to highlight the unique nature of incipient ferroelectricity in STO nanomembranes by integrating them with monolayer and semiconducting MoS_2, to develop solid-state devices for computing and cryogenic storage applications.

1. Why choose 80 nm STO nanomembranes in this manuscript? Have you compared the performance of STO with other thicknesses (such as 100 nm, 50nm)? From the characterization results in Figure 1, it can be seen that the quality of the grown STO film is relatively good. How large is the area of the film that can maintain its good quality? What's the advantages of STO over HZO (Advanced Functional Materials, 2020, 2003859).

The authors would like to thank the reviewer for highlighting an important aspect concerning the thickness of the STO nanomembranes. The selection of an 80 nm STO nanomembrane is primarily due to its impact on the leakage current in STO-gated MoS_2 FETs. It is important to note that the band gap of STO is quite small, ranging from 3.2 to 3.4 eV [1]. A thicker ferroelectric layer is beneficial in reducing the leakage current, even with a material that has a small band gap serving as the gate dielectric, as illustrated in **Fig. R1a-b**.

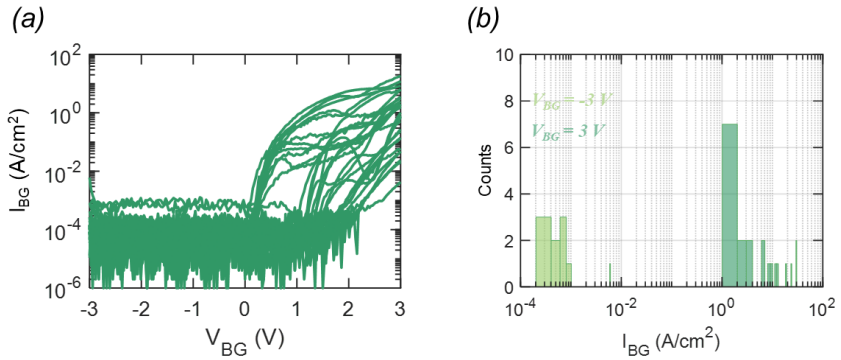

Figure R1. Gate leakage current density in STO-gated MoS_2 FETs. *a) The back-gate leakage current density (I_{BG}) as a function of the back-gate voltage (V_{BG}) for a constant source-to-drain bias of V_{DS} = 1 V, for 30 STO-gated MoS_2 FETs. b) I_{BG} extracted at V_{BG}=-3V (light green) and V_{BG}=-3V (shown in dark green) for 30 STO-gated MoS_2 FETs.*

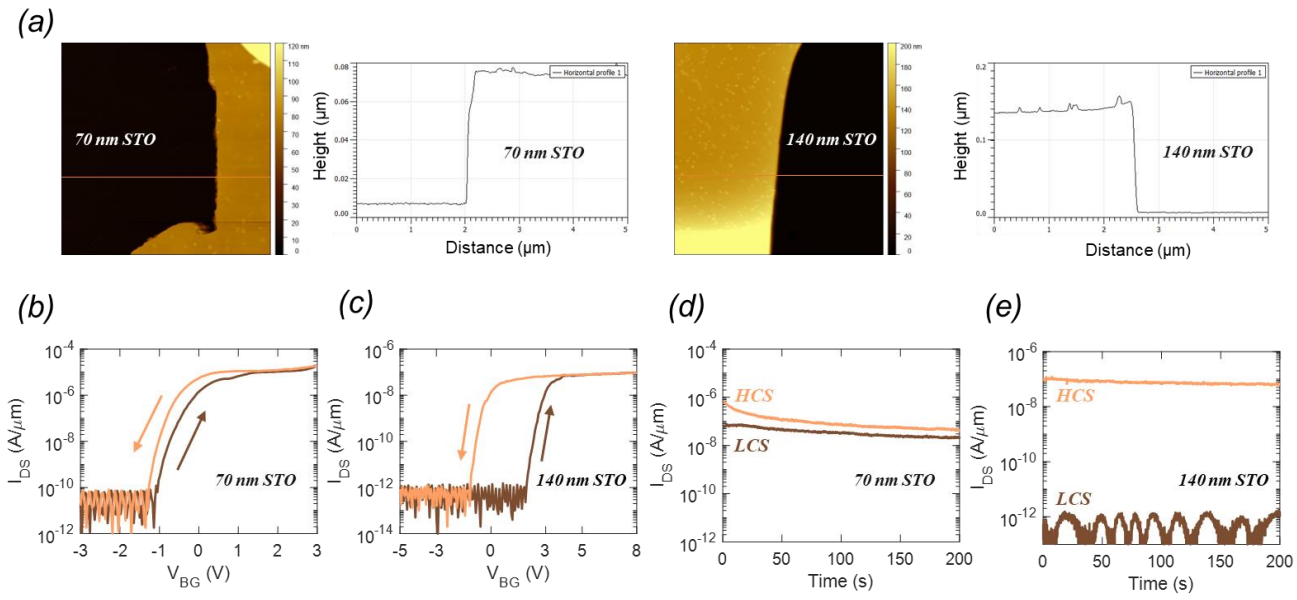

Figure R2. Ferroelectric-like MoS_2 FETs with varying STO thicknesses. *a) The atomic force microscopy (AFM) images of the as-grown STO membranes with thicknesses of 70 nm and 140 nm. Dual sweep transfer characteristics of a representative MoS_2 FET measured at T = 300 K, using STO membranes with thicknesses of b) 70 nm and c) 140 nm. Note that, the transfer characteristics shows counterclockwise hysteresis window for both 70 nm and 140 nm STO-gated MoS_2 FETs, owing to the polarization switching in the STO membrane. d-e) Non-volatile retention of memory states for STO-gated MoS_2 FET at T = 300 K, for different STO thicknesses. The 70 nm STO-gated FETs clearly exhibit non-volatile retention, although a steady decline in the memory ratio is noted. However, the 140 nm thick STO-gated 2D FET shows a larger hysteresis window (> 3 V) and a relatively stable non-volatile retention.*

Additionally, following the reviewer's suggestion, a 70 nm and 140 nm STO membrane has been grown epitaxially using hybrid MBE. The atomic force microscopy (AFM) images shown in **Fig. R2a,** reveal the physical thicknesses of these membranes. Furthermore, we have performed electrical characterization on MoS_2 FETs equipped with STO nanomembranes of varying thicknesses (70 nm and 140 nm) as shown in **Fig. R2b-c**. Note that, the transfer characteristics (I_{DS} *vs* V_{BG}) shows counterclockwise hysteresis window for both 70 nm and 140 nm STO-gated MoS_2 FETs, owing to the polarization switching in the STO membrane. The variation in the positive and negative back-gate voltage (V_{BG}) ranges can be attributed to the thickness of the STO membrane. Similar to the 80 nm STO-gated MoS_2 FETs, the 70 nm STO-gated FETs clearly exhibit non-volatile retention, although a steady decline in the memory ratio is noted as depicted in **Fig. R2d**. This likely results from the incipient ferroelectric [2, 3] nature of the STO film at room temperature. However, the 140 nm thick STO-gated 2D FET shows a larger hysteresis window (> 3 V) and a relatively stable non-volatile retention as shown in **Fig. R2e**, owing to a significantly less depolarization field and a higher coercive field in a thicker ferroelectric film [4]. It is expected that long-term retention can be achieved for the different thicknesses of STO based 2D FETs at lower temperatures, as already shown in the manuscript for an 80 nm STO ferroelectric-like FET.

We also want to thank the reviewer for inquiring about the large area quality of the freestanding STO membrane. A hybrid MBE system was employed to grow an epitaxial and single-crystalline SrO (002) sacrificial layer, followed by an STO (001) film on a $LaAlO_3$ (001) substrate. Note that the epitaxially grown STO membrane maintains purity in phase and single crystalline nature over an area of 5 mm x 5 mm [5]. Despite the challenges of handling complex sacrificial layers in the growth of freestanding membranes, which can cause microcracks, wrinkles, and bubbles in large-area membranes, it has been demonstrated in [5], that using SrO as the sacrificial layer allows the transfer of the entire 5 mm × 5 mm film onto a substrate with minimal introduction of cracks. However, in our work, using PDMS to transfer the STO membrane onto the local back-gated substrate resulted in a considerable proportion of cracks, which reduced the uniform coverage of the freestanding membrane across the entire substrate to approximately ($\sim 100\ \mu m \times 100\ \mu m$). Hence, a PMMA assisted transfer of these membrane holds the potential of achieving uniform coverage, as it has been already shown in case 2D channel materials [6].

We would like to highlight a few points regarding the benefits of using STO over HZO as a gate dielectric/ferroelectric material. Firstly, a single-crystal STO features a high dielectric constant, surpassing 300 at room temperature [7]. This high- κ nature of STO helps in scaling the EOT in 2D FETs, achieving high-performance devices. Moreover, freestanding and incipient ferroelectric STO membranes can be integrated with MoS_2 devices through van der Waals forces, enabling the development of more compact and efficient devices within the CMOS back-end. Recently, a multilayer MoS_2 FET was demonstrated with STO as the top-gate dielectric, exhibiting a near ideal SS of 66 mV/decade, suggesting a defect-free MoS_2/STO interface. Note that, by utilizing only van der Waals forces for integration, it is possible to forego pretreatment when merging the dielectric with the 2D material [8], eliminating the necessity for chemical bonding during in situ growth. These findings indicate a simplified process and maintains the integrity of the interface between the dielectric and the 2D channel. It is also important to highlight that STO membranes do not require any annealing to attain the incipient ferroelectric phase. Although substantial progress has been made in incorporating STO into 2D FETs, significant efforts must be focused on efficiently transferring these freestanding membranes to achieve larger coverage and higher yield. Additionally, given that HZO has demonstrated superior device performance at sub-10 nm thicknesses, the scaling down of STO films needs to be further optimized and examined in greater detail.

2. There are two gates in Figure 2b, which do not seem to correspond to the device schematic of Figure 2a. The authors claim that the mean value for subthreshold slope (SS) of these STO-gated MoS_2 FETs is 220 mV/decade. For ferroelectric transistors, why is this SS so large?

The authors wish to clarify that the device schematic has been updated in the revised manuscript and apologize for the inconsistency between Fig. 2a and Fig. 2b.

The reviewer is absolutely correct in pointing out that the subthreshold slope (SS) value is large in our STO based ferroelectric transistors. The large SS values of the STO-gated MoS_2 FETs can be attributed to the presence of interface trap states at the MoS_2/STO interface, which leads to a finite capacitance (C_{IT}) worsening the SS following Equation 1.

$$SS = (ln10)\left(\frac{k_B T}{q}\right)\left(1 + \frac{C_{IT}}{C_{OX}}\right); C_{it} = qD_{it} \quad (1)$$

In Eq. 1, k_B, T, q, C_{OX} are the Boltzmann constant, ambient temperature, elementary charge and the oxide capacitance of STO, respectively. For an 80 nm thick STO membrane with a dielectric constant of ~ 40 [5], the C_{OX} was found to be 4.4×10^{-7} F/cm^2. Hence, following Eq.1, the extracted value of C_{IT} was 1.2×10^{-6} F/cm^2 for a SS of 220 mV/decade. Furthermore, the interface trap density, D_{it}, can be extracted from the SS using Eq.1. Note that the calculated D_{it} was found to be 7.4×10^{12} eV^{-1} cm^{-2}. Additionally, the Schottky barrier height at the Ni/MoS_2 interface can also worsen the SS [9, 10].

3. From Figure 3a, it can be seen that the hysteresis window is relatively small. It is suggested to add the Ig-Vg curve to further prove that the hysteresis window is caused by ferroelectric polarization?

The authors would like to thank the reviewer for the pertinent suggestion. The reviewer accurately noted that the hysteresis window in the STO-gated MoS_2 FET is relatively narrow, as demonstrated in Fig. 3a. To further elucidate on the incipient ferroelectric polarization in the STO membranes, the characteristics of the back-gate leakage current (I_{BG}) as a function of the back-gate voltage (V_{BG}) is illustrated in **Fig. R3a**. Note that I_{BG} exhibits a weak switching current peak, owing to incipient polarization at V_{BG} = 3 V. However, the absence of a switching current peak at V_{BG} = -3 V can be attributed to the incipient ferroelectric behavior of the STO membranes, which tend to introduce weak ferroelectric orders at room temperature, leading to an unstable polarization switching. While at a lower temperature (T = 100 K or below), I_{BG} displays switching current peaks at both positive (V_{BG} = 5 V) and negative (V_{BG} = -3 V) gate biases, as depicted in **Fig. R3b**, suggesting that stable polarization switching in the STO nanomembrane is more effective at lower temperatures.

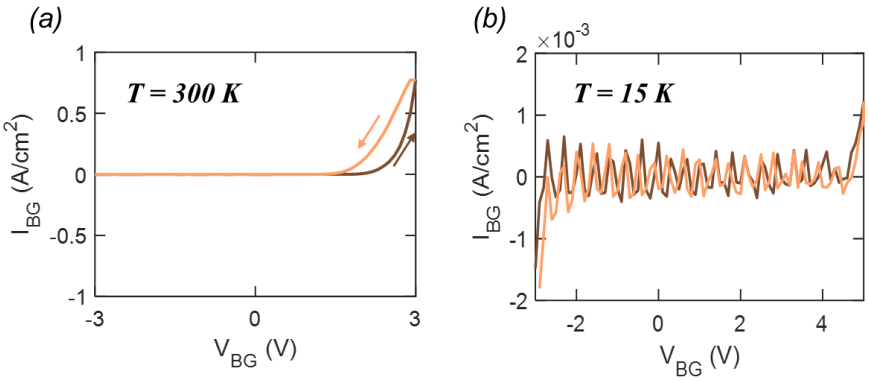

Figure R3. Dual sweep leakage current characteristics in STO-gated MoS_2 FETs. *a) Back-gate leakage current density (I_{BG}) as a function of the back-gate voltage (V_{BG}) for a constant source-to-drain bias of V_{DS} = 1 V, measured at T = 300 K. I_{BG} displays a switching current peak at V_{BG} = 3 V due to incipient polarization switching, whereas the absence of such a peak at V_{BG} = -3 V is attributed to the relaxor ferroelectric behavior of STO membranes, which induce weak and unstable ferroelectric orders at room temperature. b) I_{BG} extracted at T= 15 K shows switching current peaks at both positive (V_{BG} = 5 V) and negative (V_{BG} = -3 V) gate biases.*

4. Why are the trends of HCS and LCS different as the switching time changes in Figure h? Especially, why does LCS significantly decrease below 102 ns? Can the multistate characteristics be applied for other types neuromorphic computing, e.g., reinforcement learning (Advanced Materials, 2022, 2107754-1-11)?

The authors appreciate the reviewers' concern regarding the high conductance state (HCS) and low conductance state (LCS) being different as a function of the switching pulse-width (τ_{SW}). We employed V_{BG} = 5 V and V_{BG} = -3 V to switch the ferroelectric domains in the STO film between HCS and LCS, with τ_{SW} varying from 10 ms to 20 ns at T = 100 K. We observed that the STO film could switch as quickly as 60 ns without noticeable degradation in the memory ratio (MR). However, shorter pulses led to a steady decline in MR. Notably, using higher magnitude V_{BG} pulses, MR was restored even when τ_{SW} was as short as 20 ns. Additionally, we also demonstrated that a τ_{SW} of 10 ns can be achieved at cryogenic temperatures (T = 15 K), with a V_{BG} = 6 V and -6 V, without any degradation in the MR.

Furthermore, it must be mentioned that, there is an inverse relationship between pulse width and pulse amplitude during the switching of ferroelectric polarization: a shorter pulse width requires a higher pulse amplitude, while a lower amplitude can be offset by using a longer pulse width [4, 11]. In essence, the ferroelectric domains in STO may encounter partial/full polarization switching as a function of the applied pulse having a certain width and amplitude.

The reviewer correctly identifies the potential to use multi-bit memory in STO-based 2D FETs across different neuromorphic computing applications, including reinforcement learning. To address this more directly, the multi-state capabilities of STO-gated FETs can be harnessed to act as multi-bit synapses, capable of storing multiple weights (conductance states) in brain-inspired reinforcement learning scenarios, as shown in [12]. We have discussed the possible application of multi-bit memory citing the referred article in our revised manuscript.

5. The authors claim that the projected retention was found to be more than 10 years. How did they draw this conclusion?

The authors wish to clarify that the projection of retention up to 10 years is based on an extrapolation from the observed retention time. As demonstrated in the manuscript, the retention of HCS and LCS were measured over 10^4 seconds without any noticeable decline in the MR. Given the stable non-volatile memory performance at 15 K and 100 K, the retention is extrapolated to exceed 10 years. **Fig. R4a-b** displays the long-term retention, including fitting and projection for up to 10 years. It must be highlighted that a reduction in the MR can be observed beyond 10^6 seconds based on the extrapolated results. Notably, many FeFET [4, 13] demonstrations have projected retention times for up to 10 years as a way to gauge the suitability of these devices for non-volatile memory applications.

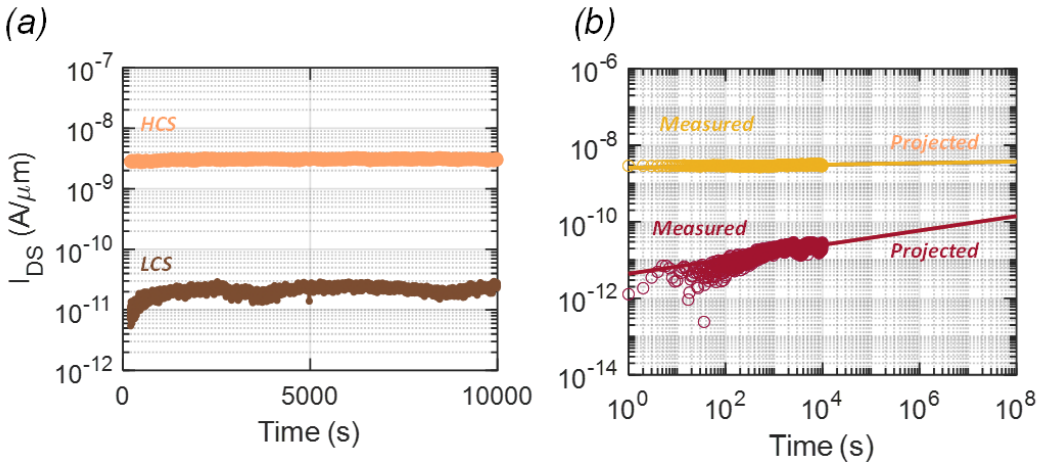

Figure R4. Long-term memory retention at T=15 K. *a) Memory retention measured for 1×10^4 s at T =15 K. b) the long-term retention, including fitting and projection for up to 10 years. 10^8 seconds corresponds to approximately 10 years.*

Reviewer#2:

The work proposed by the authors deal with the integration of single-crystalline STO nanomembranes with monolayer MoS2 films to target back end of line (BEOL) compatible FeFETs, demonstrating rapid polarization switching, nonvolatile retention, and notable endurance within a low thermal budget. There is a certain novelty in the work and a large number of very interesting experimental results and their interpretations. But finally, the paper fails to demonstrate that the expected good properties of FeFETs based on single-crystalline STO nanomembranes with monolayer MoS2 films are maintained at room temperature. Indeed, the goal of building neuromorphic hardware integrated on CMOS needs room temperature operation and this is the main roadblock that the paper is not solving. The study remains interesting and valuable but the main claim that would generate true impact for a paper in Nature journal is finally not full achieved neither a clear path about what optimization could be clearly foreseen to address this gap. Therefore, a number of important questions that the authors should carefully address before any consideration for publication, remain as it follows:

The authors want to thank the reviewer for the thoughtful comments and insights regarding our study. We appreciate the reviewers' recognition of the novelty and the comprehensive experimental results presented in our manuscript.

The reviewer is correct in pointing out that our study does not conclusively show the effectiveness of single-crystalline STO nanomembranes with monolayer MoS_2 films as synapses at room temperature, owing to the presence of weak ferroelectric domains in STO. Our primary focus was to explore the potential of integrating freestanding STO nanomembranes with 2D films at BEOL-compatible temperatures for novel functionalities. While room temperature synaptic weight storage operation was not achieved, we successfully utilized pseudo-nonvolatile polarization switching to create a neuromorphic hardware operational at room temperature. More specifically, the dynamic polarization switching in STO films has been exploited as a "fading memory to construct a physical reservoir for reservoir computing at room temperature. This advancement indicates that even with a limited number of FETs, the reservoir can effectively store a broad range of input patterns, highlighting the possibility of recognizing an even larger array of unique patterns by increasing the number of FETs in the reservoir.

At low temperatures (T = 15 K), we achieved non-volatile memory with retention projected for 10 years from the same device, suitable for the development of a cryogenic memory. We also demonstrated ultra-fast polarization switching in under 10 ns with a switching voltage below 6 V and showed more than 10,0000 cycles of endurance. Additionally, our findings include a 5-bit storage capacity, equating to 32 distinct memory states in a single device. We believe these results are substantial for this manuscript to be considered for publication in Nature Communications.

However, we acknowledge the reviewer's concern regarding room temperature synapse operation. Achieving this will require engineering a stable ferroelectric phase in the STO nanomembranes, which, according to earlier reports, can be accomplished by imposing out-of-plane strain [14] and introducing Sr/O or Ti/O vacancies in the STO lattice [15, 16]. This will be the focus of our future work.

1) Most important: the authors essentially demonstrate useful STO-gated MoS2 FeFETs with

nonvolatile polarization switching up to 200 K, with the performance degrading with increasing temperature (best performance reported rather at 100K – STO-gated MoS2 FeFET at T = 100 K in Fig. 4). The authors also conclude that increasing the temperature leads to increased thermal fluctuations, that accelerate the destabilization of the polar order, a thermal decay of ferroelectricity in their material devices. A neuromorphic chip at 100K is certainly not very attractive for Edge AI applications. What mechanism engineering the authors think can be used to bring such polar order usable at room temperature and, especially, what proof they have this can be controlled, optimized, and used in building efficient/competitive synapses and neurons operating at room temperature? Otherwise, the study remains of interest, but the impact is significantly reduced.

As mentioned in our response to your general comment, this work demonstrates a neuromorphic inference engine or can also operate as a physical reservoir for reservoir computing, that exploits pseudo-nonvolatile polarization switching in STO nanomembranes at room temperature, as well as a cryogenic memory device at lower temperatures. It is important to clarify that stable ferroelectric orders at room temperature were not achieved in STO, as these materials exhibit a polar soft mode that does not fully transition to ferroelectricity due to quantum effects that prevent the transition [17]. Our future work will focus on engineering strain and/or defects in the STO nanomembrane for room temperature synaptic devices [14-16]. Alternatively, other nanomembranes, such as BTO, may also be considered.

2) The authors essentially performed experiments of ferroelectric behavior and retention on transistor like structures. Building and testing, for instance, dedicated capacitive structures with STO membranes of various thicknesses on 2D semiconducting films could offer very interesting proof and insights into the retention mechanisms, together with the extraction of some key data from the ferroelectric capacitors such remnant polarization, coercive fields, and leakage. This information about such key parameters is not explored and not reported sufficiently in the paper. Measuring the characteristics of fabricated FETs based on freestanding membranes on 2D channels is certainly a great achievement but complementary characterization and confirmation of quantitative ferroelectric figures of merit and their degradation with temperature, appears as a must for publication. In addition, the authors can try to perform PFM measurements on the 3D STO membranes, as another complementary experiment aiming at ferroelectricity characterization.

The authors concur with the reviewers' observation about dedicated capacitive structures featuring STO membranes of differing thicknesses. In this regard, it is important to note that the incipient ferroelectric nature of STO acted as a barrier to characterizing the capacitors in terms of measuring remnant polarization, coercive fields etc. Unlike traditional ferroelectric materials such as HZO and BTO having stable ferroelectric domains, freestanding STO membranes display a weaker long-range correlation among pre-existing nano polar regions, which thermally decay over time [2], leading to unstable polarization switching at 300 K. Hence, to accurately capture the spontaneous polarization using PE loop measurements, it is crucial to establish stable long-range correlations among the ferroelectric domains throughout the film, a condition that is unlikely to be achieved in incipient ferroelectric STO films.

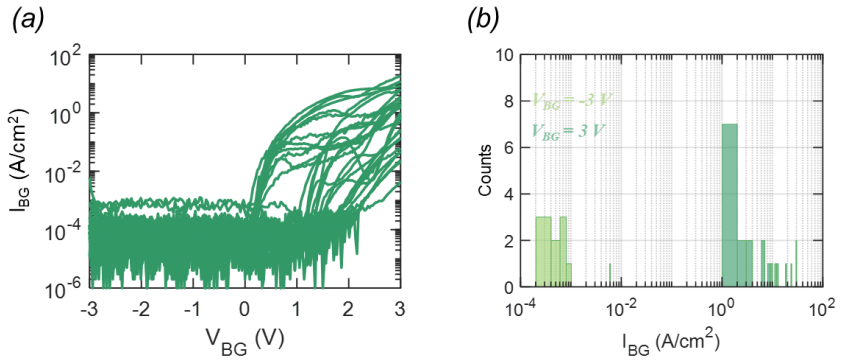

Figure R5. Gate leakage current density in STO-gated MoS_2 FETs. *a) The back-gate leakage current density (I_{BG}) as a function of the back-gate voltage (V_{BG}) for a constant source-to-drain bias of V_{DS} = 1 V, for 30 STO-gated MoS_2 FETs. b) I_{BG} extracted at V_{BG}=-3V (light green) and V_{BG}=-3V (shown in dark green) for 30 STO-gated MoS_2 FETs.*

In order to investigate the leakage current density in STO-gated MoS_2 FETs, we assessed the characteristics of the back-gate leakage current (I_{BG}) as a function of the back-gate voltage (V_{BG}) is illustrated in **Fig. R5a**. Note that, despite having a relatively small bandgap of approximately ranging from 3.2 to 3.4 eV [1], the 80 nm STO nanomembrane exhibited relatively low I_{BG}, as indicated by the corresponding histograms extracted for V_{BG} = 3 V and -3 V in **Fig. R5b**.

Additionally, the authors do understand the importance of characterizing the incipient ferroelectric STO nanomembranes. In this context, we have obtained piezo force microscopy (PFM) images of the STO film after it was transferred onto a gold-plated substrate at room temperature. **Fig. R6a-c** displays the topography, PFM amplitude, and PFM phase images, respectively. These images reveal details about the local electromechanical properties and the arrangement of weak ferroelectric domains in the out-of-plane direction. **Fig. R6d** depicts domain switching, whereas the unsaturated ferroelectric phase demonstrates its instability, reaffirming the incipient nature of ferroelectricity at room temperature in STO nanomembranes. Therefore, a low temperature PFM [18] would be the ideal choice to depict the stable ferroelectric orders, both in amplitude and phase.

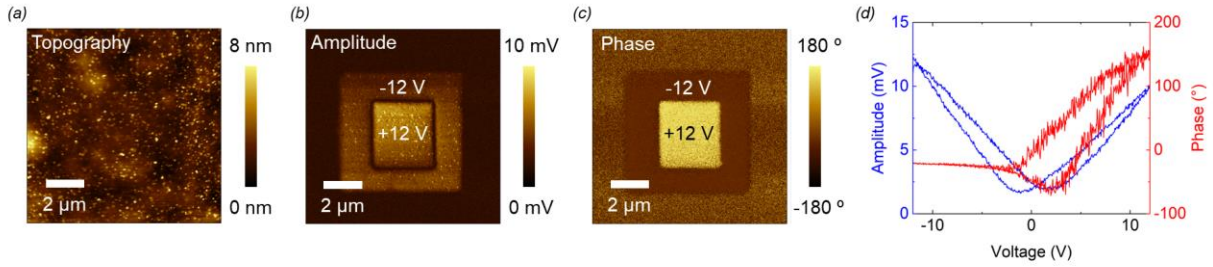

Figure R6. Piezo force microscopy (PFM) of STO nanomembrane. *a) Topography, b) amplitude, and c) phase images of STO film, transferred onto a gold-plated substrate, captured using piezo force microscopy (PFM) at room temperature. These images provide insights into the local electromechanical behavior and the distribution of ferroelectric domains in the out-of-plane direction. d) Amplitude and phase hysteresis loops observed in the STO film on the gold-plated substrate, indicating incipient ferroelectricity at room temperature.*

Additionally, to verify the presence of nano-polar domains in the STO film at room temperature, we acquired cross-sectional atomic resolution STEM-HAADF images of the STO layer along the [001] zone axis in the area beneath the electrode, as illustrated in **Fig. R7a**. These atomic resolution images were analyzed using the Atomap software package [19] to locate the positions of Sr and Ti. The polarization in the STO is assessed by measuring the displacement of Ti atoms from the center of the surrounding four Sr atoms. Note that multiple nanodomains have been observed in the STEM image, owing to the presence of Ti/O point defects. A vector plot, originating from the Ti atom positions, demonstrates the magnitude and direction of polarization, as shown in **Fig. R7b-d**. The polarization of the STO is mostly along the same direction, pointing from top to bottom, with varying magnitudes forming several nanodomain consistent with our observations from SHG and electrical measurements.

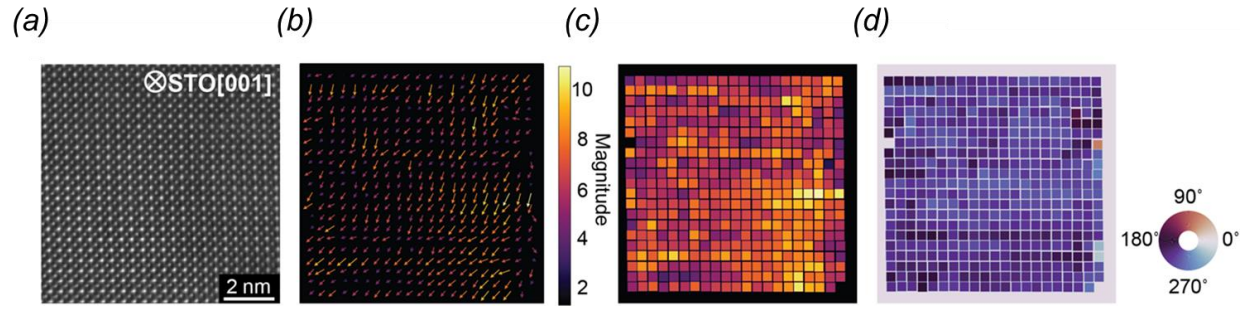

Figure R7. Origin of incipient ferroelectricity in STO nanomembrane. *a) Atomic resolution HAADF STEM image of the STO film under the contact electrode. Corresponding maps of b) the polarization vector, and its c) magnitude and d) phase.*

Besides, following the reviewer's suggestion, a 70 nm and 140 nm STO membrane has been grown epitaxially using hybrid MBE. The atomic force microscopy (AFM) images shown in **Fig. R8a** reveal the physical thickness of these membranes. Notably, we have performed electrical characterization on MoS_2 FETs equipped with STO nanomembranes of varying thicknesses (70 nm and 140 nm) as shown in **Fig. R8b-c**. The transfer characteristics ($I_{DS}\ vs\ V_{BG}$) shows counterclockwise hysteresis window for both 70 nm and 140 nm STO-gated MoS_2 FETs, owing to the polarization switching in the STO membrane. The variation in the positive and negative back-gate voltage (V_{BG}) ranges can be attributed to the thickness of the STO membrane, which in turn affects the coercive voltage of the material. Similar to the 80 nm STO-gated 2D FETs, the 70 nm STO-gated 2D FET clearly exhibits non-volatile retention, although a steady decline in the memory ratio is noted as depicted in **Fig. R8d**. This likely results from the incipient ferroelectric [3, 18] nature of the STO film at room temperature. However, the 140 nm thick STO-gated 2D FET shows a larger hysteresis window (> 3 V) and a relatively stable non-volatile retention as shown in **Fig. R8e**, owing to a significantly less depolarization field and a higher coercive field in a thicker ferroelectric film [4]. It is expected that long-term retention can be achieved for the different thicknesses of STO based MoS_2 FETs at lower temperatures, as already shown in the manuscript for an 80 nm STO-gated 2D FETs.

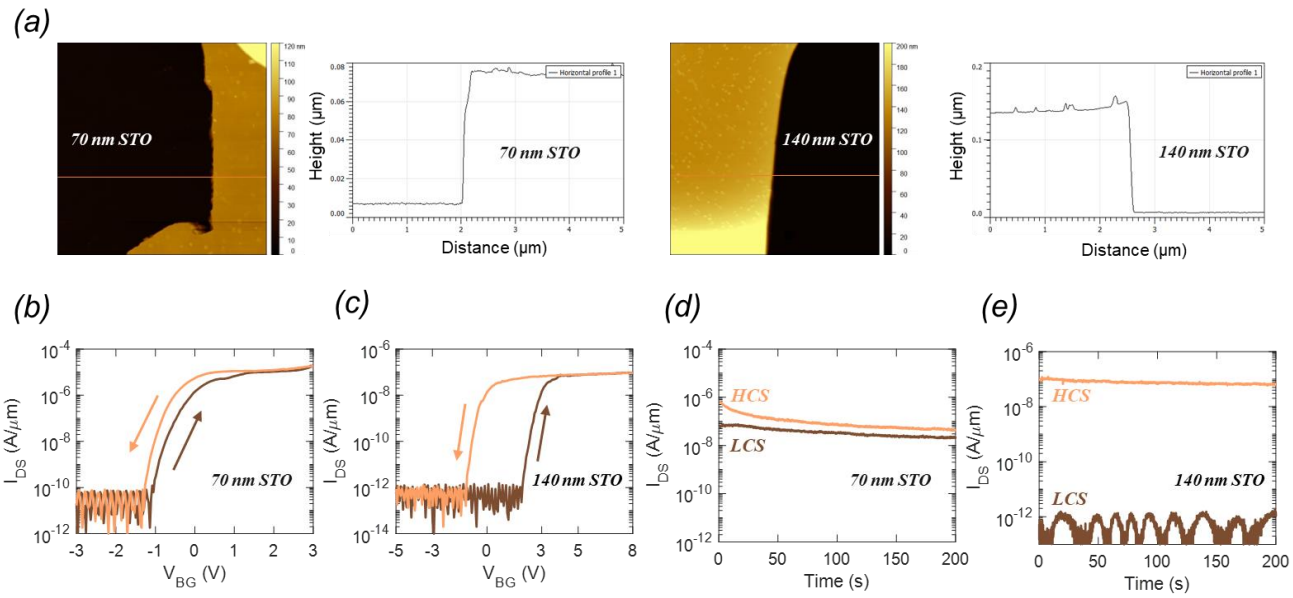

Figure R8. Ferroelectric-like MoS_2 FETs with varying STO thicknesses. *a) The atomic force microscopy (AFM) images of the as-grown STO membranes with thicknesses of 70 nm and 140 nm. Dual sweep transfer characteristics of a representative MoS_2 FET measured at T = 300 K, using STO membranes with thicknesses of b) 70 nm and c) 140 nm. Note that, the transfer characteristics shows counterclockwise hysteresis window for both 70 nm and 140 nm STO-gated MoS_2 FETs, owing to the polarization switching in the STO membrane. d-e) Non-volatile retention of memory states for STO-gated MoS_2 FET at T = 300 K, for different STO thicknesses. The 70 nm STO-gated FETs clearly exhibit non-volatile retention, although a steady decline in the memory ratio is noted. However, the 140 nm thick STO-gated 2D FET shows a larger hysteresis window (> 3 V) and a relatively stable non-volatile retention.*

3) It would be also of interest to extract and discuss the variability of transfer characteristics ID-VG (like in Fig. 2 (f)) and the related hysteresis as a function of temperature and derive a semi-quantitative physics-based model to explain the observed dependency. The authors have here the good points that they have a statistical testing on micrometer scale devices, with variability attributed to residues and wrinkles introduced during the 3D and 2D membrane transfer processes involving PDMS and PMMA. Have the authors double-checked the uniformity of the thickness of the membranes and interfacial defects to exclude them as source of variability?

The authors would like to thank the reviewer for the valuable remark. Based on the reviewers' advice, we have performed electrical characterization on STO-gated MoS_2 FETs for varying temperatures (50 K, 100 K, 200 K and 300 K) as shown in **Fig. R9a**. The transfer characteristics displays a positive shift in the threshold voltage (V_{th}) as the temperature is reduced to lower values. These findings can be attributed to the reduced carrier concentration (n_s) at lower temperatures, leading to an increase in the V_{th}. Additionally, a counterclockwise hysteresis displaying minimal variations in the hysteresis window, also referred to as the memory window, is evident and illustrated in **Fig. R9b**. Furthermore, the temperature-dependent measurements suggest that the stability in polarization switching is predominantly due to the reduced thermal fluctuations at lower temperatures. Note that, in traditional ferroelectric materials like HZO, where remnant polarization (P_r) decreases with increasing temperature, the memory window similarly reduces [20]. However, in an incipient ferroelectric film such as STO, there is no P_r present, which prevents the establishment of a correlation between temperature and P_r. Hence, based on the experimental data presented in **Fig. R9b** for a representative STO-gated MoS_2 FET, it can be concluded that the memory window remains relatively stable across different temperatures. Therefore, modeling the relationship between the memory window and temperature is not feasible without comprehending how P_r varies with changes in temperature in an incipient ferroelectric material.

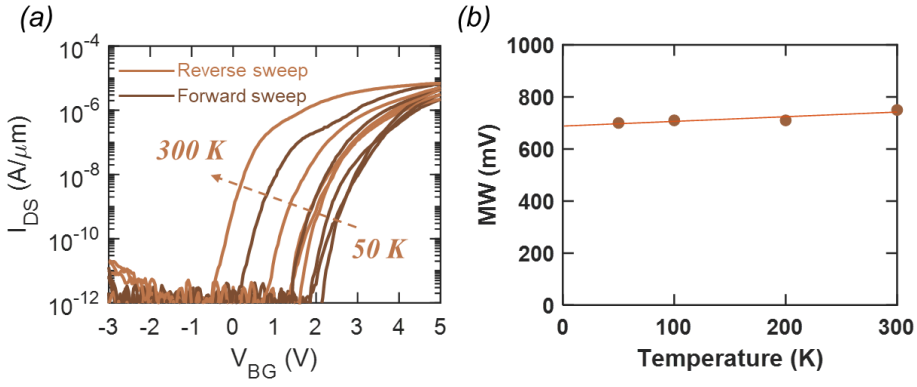

Figure R9. Dependence of memory window on temperature. *a) Dual sweep transfer characteristics of a representative STO-gated MoS_2 FET, measured at T = 50 K, 100 K, 200 K and 300 K. b) MW measured at T = 50 K, 100 K, 200 K and 300 K.*

The authors would also like to mention that a hybrid MBE system was employed to grow an epitaxial and single-crystalline SrO (002) sacrificial layer, followed by an STO (001) film on a $LaAlO_3$ (001) substrate. It is well known that, epitaxially grown thin films have uniform thicknesses as shown in [5]. However, to verify the uniformity of the thicknesses of STO nanomembranes, we have conducted atomic force microscopy (AFM) on a few representative devices having 80 nm STO film. Furthermore, the AFM images are shown in **Fig. R10,** which reveal that the physical thicknesses of these membranes are nearly uniform throughout all the devices. Additionally, the large *SS* values of the STO-gated MoS_2 FETs suggests that a significant number of interfacial defects are present at the MoS_2/STO interface.

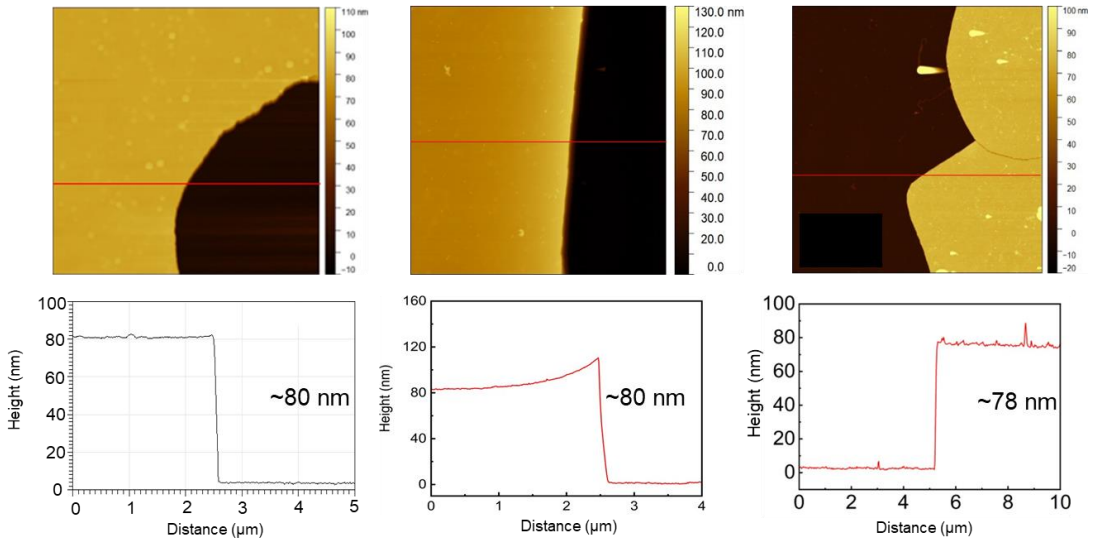

Figure R10. *The atomic force microscopy (AFM) images of the transferred STO membranes show a consistent physical thickness across multiple devices.*

4) Finally, as there are many new candidate technologies for FeFETs for building neuromorphic blocks as synapses and neurons, with many of them operating already at room temperature, a table comparing the main merits of the proposed device architecture with other technologies will be useful, at least as additional material.

The authors would like to thank the reviewer for the valuable suggestion. **Extended Data Fig. 12** illustrates a benchmarking table in our manuscript. Based on the reviewers' remark, a modified benchmarking table has been added to the revised manuscript, as shown in **Fig. R11,** which outlines and compares the performance metrics of our STO-based MoS_2 FET against those of leading state-of-the-art FeFET candidates. This table provides a clear and concise comparison, highlighting the competitive advantages and unique characteristics of our STO-based FeFETs in relation to other ferroelectric devices in the field.

Ferroelectric Thin Films	**Thickness (nm)**	**Switching voltage, $\|V_{SW}\|$ (V)**	**Switching speed, t_{SW} (s)**	**Number of memory states**	**Retention**		**Operating temperature (K)**	**Endurance (cycles)**	**Ref.**
					Measured (s)	**Projected (years)**			
AlScN	100	~ 40	$< 2 \times 10^{-7}$	2	10^5	--	300	10^4	[21]
AlScN	45	40	5×10^{-7}	16	10^5	> 10	300	$> 10^4$	[4]
AlScN	45	10	10^{-1}	16	10^5	> 10	300	$> 10^4$	[4]
PZT/IGZO	230	5.2	--	2	10^3	--	> 420	--	[22]
PZT	100	2.3	10^{-3}	2	10^4	--	--	5×10^2	[23]
PZT	500	2.5	10^{-5}	2	$> 10^4$	10 (days)	300	4×10^2	[24]
BST	300	3	1	2	10^3	--	300	--	[25]
BTO	290	6	10^{-1}	2	10^3	10^5 (s)	300	5×10^5	[26]
$CuInP_2S_6$	87	10	10^{-7}	16	$> 10^3$	> 10	300	10^4	[13]
P(VDF-TrFE)	300	> 30	5×10^{-5}	2	$> 10^3$	--	300	$> 10^4$	[27]
BFLMO	200	25	$< 5 \times 10^{-2}$	4	$> 10^3$	--	300	10^3	[28]
STO	**80**	**< 5**	**2×10^{-8}**	**64**	**$> 10^4$**	**> 10**	**100**	**10^4**	**This work**
STO	**80**	**< 6**	**1×10^{-8}**	**32**	**10^4**	**> 10**	**15**	**10^5**	**This work**

Figure R11. *Benchmarking table.*

Reviewer#3:

The manuscript "Stacking of Ferroelectric and Freestanding 3D SrTiO3 and 2D MoS2 Nanomembranes for Reconfigurable Neuromorphic Hardware" by D Sen et al. presents a compelling exploration of ferroelectricity in freestanding SrTiO3 (STO) nanomembranes, integrated with monolayer MoS2 to develop reconfigurable neuromorphic devices. The study is timely, and the combination of complex oxides with 2D materials for non-volatile systems addresses current challenges in neuromorphic applications. Indeed, the manuscript explores a cutting-edge area, where freestanding nanomembranes of 3D single crystals, particularly STO, are combined with 2D materials like MoS2 for neuromorphic devices. The quality of the devices presented in the manuscript is commendable. The reported ultra-fast polarization switching, low-switching voltage, nonvolatile retention, and endurance metrics make the proposed STO-gated MoS2 FeFETs promising for practical applications. The reconfigurable neuromorphic device functionality is particularly appealing. The manuscript highlights the potential of integrating these materials into the back end of silicon complementary metal oxide semiconductor technology (due to the low temperature needed in the fabrication process), opening up opportunities for addressing challenges associated with compute-in-memory architectures and neuromorphic applications.

The main weakness lies in the description of the state-of-the-art in the introduction. The references provided by the author are not comprehensive, and several relevant works about the isolation of freestanding perovskite oxide layers and the combination of perovskite oxides with MoS2 and other semiconductors, which may have been consulted by the authors, are not mentioned. Improving the introduction by incorporating these references would enhance the overall quality of the manuscript.

The authors appreciate the reviewers' recognition of the manuscript's merits and the detailed experimental results it presents. Following the reviewers' comments about the state-of-the-art description in the introduction, we have comprehensively addressed the relevant studies on freestanding perovskite oxides and their combination with 2D materials in the revised manuscript.

References

[1] A. J. Yang *et al.*, "Van der Waals integration of high-κ perovskite oxides and two-dimensional semiconductors," *Nature Electronics,* vol. 5, no. 4, pp. 233-240, 2022.

[2] Y. Zhang *et al.*, "Room-temperature electric field-induced out-of-plane ferroelectric polarization in strain-free freestanding 2D SrTiO3 membranes," *APL Materials,* vol. 11, no. 4, 2023.

[3] I. Sokolović, M. Schmid, U. Diebold, and M. Setvin, "Incipient ferroelectricity: A route towards bulk-terminated SrTiO 3," *Physical Review Materials,* vol. 3, no. 3, p. 034407, 2019.

[4] K.-H. Kim *et al.*, "Scalable CMOS back-end-of-line-compatible AlScN/two-dimensional channel ferroelectric field-effect transistors," *Nature Nanotechnology,* pp. 1-7, 2023.

[5] S. Varshney *et al.*, "Hybrid Molecular Beam Epitaxy for Single-Crystalline Oxide Membranes with Binary Oxide Sacrificial Layers," *ACS nano,* 2024.

[6] A. Dodda *et al.*, "Active pixel sensor matrix based on monolayer MoS2 phototransistor array," *Nature Materials,* vol. 21, no. 12, pp. 1379-1387, 2022.

[7] R. Neville, B. Hoeneisen, and C. Mead, "Permittivity of strontium titanate," *Journal of Applied Physics,* vol. 43, no. 5, pp. 2124-2131, 1972.

[8] J.-K. Huang *et al.*, "High-κ perovskite membranes as insulators for two-dimensional transistors," *Nature,* vol. 605, no. 7909, pp. 262-267, 2022.

[9] S. Das *et al.*, "Transistors based on two-dimensional materials for future integrated circuits," *Nature Electronics,* vol. 4, no. 11, pp. 786-799, 2021.

[10] D. S. Schulman, A. J. Arnold, and S. Das, "Contact engineering for 2D materials and devices," *Chemical Society Reviews,* vol. 47, no. 9, pp. 3037-3058, 2018.

[11] H. Mulaosmanovic, E. T. Breyer, S. Dünkel, S. Beyer, T. Mikolajick, and S. Slesazeck, "Ferroelectric field-effect transistors based on HfO2: a review," *Nanotechnology,* vol. 32, no. 50, p. 502002, 2021.

[12] Y. Zhou *et al.*, "A reconfigurable two-WSe2-transistor synaptic cell for reinforcement learning," *Advanced Materials,* vol. 34, no. 48, p. 2107754, 2022.

[13] X. Wang *et al.*, "Van der Waals engineering of ferroelectric heterostructures for long-retention memory," *Nature communications,* vol. 12, no. 1, p. 1109, 2021.

[14] R. Xu *et al.*, "Strain-induced room-temperature ferroelectricity in SrTiO3 membranes," *Nature communications,* vol. 11, no. 1, p. 3141, 2020.

[15] J. Liu *et al.*, "Room-Temperature Ferroelectricity of Paraelectric Oxides Tailored by Nano-Engineering," *ACS Applied Materials & Interfaces,* vol. 15, no. 3, pp. 4226-4233, 2023.

[16] T. Li *et al.*, "Superfine Nanodomain Engineering Unleashing Ferroelectricity in Incipient Ferroelectrics," *Journal of the American Chemical Society,* 2024.

[17] M. Jiang *et al.*, "The origin of incipient ferroelectricity in lead telluride," *Nature Communications,* vol. 7, no. 1, p. 12291, 2016.

[18] Y. Lee *et al.*, "Wafer-scale synthesis and transfer of graphene films," *Nano Lett,* vol. 10, no. 2, pp. 490-3, Feb 10 2010, doi: 10.1021/nl903272n.

[19] M. Nord, P. E. Vullum, I. MacLaren, T. Tybell, and R. Holmestad, "Atomap: a new software tool for the automated analysis of atomic resolution images using two-dimensional Gaussian fitting," *Advanced structural and chemical imaging,* vol. 3, pp. 1-12, 2017.

[20] S. Chatterjee, S. Kumar, A. Gaidhane, C. K. Dabhi, Y. S. Chauhan, and H. Amrouch, "Temperature- and variability-aware compact modeling of ferroelectric FDSOI FET for memory and emerging applications," *Solid-State Electronics,* p. 108954, 2024.

[21] X. Liu *et al.*, "Post-CMOS compatible aluminum scandium nitride/2D channel ferroelectric field-effect-transistor memory," *Nano Letters,* vol. 21, no. 9, pp. 3753-3761, 2021.

[22] C. Besleaga *et al.*, "Ferroelectric field effect transistors based on PZT and IGZO," *IEEE Journal of the Electron Devices Society,* vol. 7, pp. 268-275, 2019.

[23] A. Lipatov, P. Sharma, A. Gruverman, and A. Sinitskii, "Optoelectrical Molybdenum Disulfide (MoS2) ‧ Ferroelectric Memories," *ACS nano,* vol. 9, no. 8, pp. 8089-8098, 2015.
[24] C. Ko *et al.*, "Ferroelectrically gated atomically thin transition-metal dichalcogenides as nonvolatile memory," *Advanced materials,* vol. 28, no. 15, pp. 2923-2930, 2016.
[25] Y. Jeong *et al.*, "Low Voltage and Ferroelectric 2D Electron Devices Using Lead-Free BaxSr1-xTiO3 and MoS2 Channel," *Advanced Functional Materials,* vol. 30, no. 7, p. 1908210, 2020.
[26] Z. Wang *et al.*, "Reconfigurable Quasi-Nonvolatile Memory/Subthermionic FET Functions in Ferroelectric–2D Semiconductor vdW Architectures," *Advanced Materials,* vol. 34, no. 15, p. 2200032, 2022.
[27] X. Wang *et al.*, "Ferroelectric FET for nonvolatile memory application with two-dimensional MoSe2 channels," *2D Materials,* vol. 4, no. 2, p. 025036, 2017.
[28] Q. Zhang *et al.*, "Tunable Multi-Bit Nonvolatile Memory Based on Ferroelectric Field-Effect Transistors," *Advanced Electronic Materials,* vol. 8, no. 5, p. 2101189, 2022.

Reviewer #1 (Remarks to the Author):

The authors have responded to the reviewers' questions in a satisfactory manner. It is suitable for the publication.

The authors are grateful for the reviewer’s supportive feedback and wish to thank him/her for recommending the work for publication.

Reviewer #2 (Remarks to the Author):

The paper is well-written and presents clear novelty in both material and device research. The experiments and discussions are very informative. However, it is clear that this is not yet a technology ready for neuromorphic computing at room temperature. The cryogenic performance of STO-based FeFETs is very good. Nonetheless, the applicability of this technology for mainstream memory applications remains limited unless further important improvements can be achieved at room temperature.

We appreciate the reviewers' recognition of the novelty, and the comprehensive experimental results presented in our manuscript.

However, we respectfully disagree with reviewers opinion that the technology is not yet ready for neuromorphic computing at room temperature. We have clearly shown reservoir computing using STO-gated MoS_2 FETs at room temperature. Kindly note that neuromorphic computing extends beyond the demonstration of synapses or memory devices; it also includes neurons, which serve as computing units without inherent memory. Furthermore, the shift towards more biologically-inspired computing models opens up opportunities to explore systems that leverage transient, fading memory—such as reservoir computing. In such systems, the emphasis is on dynamic, time-dependent processing rather than long-term memory storage, allowing for more efficient computation in tasks like pattern recognition and temporal data processing. This approach aligns more closely with the principles of biological neural systems, where memory and computation are not distinct processes.

We are also not sure if the reviewer have carefully read our revised manuscript. We have clearly articulated under the section "Construction of cryogenic memory and neuromorphic hardware", the use of STO-based FeFETs as cryogenic memory. It is quite well known that cryogenic computing and memory components are crucial, particularly in the context of space electronics and in developing quantum computers. Note that conventional superconducting memories often fall short in terms of higher memory density and energy efficiency. Recently, a Si-doped HfO_2 FeFET based cryogenic memory has been demonstrated, operating at 6.9 K with large memory window even at lower temperatures [1]. In this context, we explore the possibility of developing a cryogenic memory system exploiting the stable ferroelectric order in STO-gated MoS_2 FETs at low temperature.

*Comment and Question #1:
Lack of Room Temperature Synaptic Operation – Neuromorphic computing hardware for autonomous systems requires operation at room temperature. While the authors' demonstration of pseudo-nonvolatile polarization switching at room temperature is noteworthy, the absence of stable ferroelectricity at 300 K significantly weakens the overall impact of the work, especially for edge AI applications.

We respectfully disagree with the reviewer's opinion that neuromorphic hardware always requires room-temperature synaptic or memory operation. Neuromorphic computing encompasses more than just synapses or memory devices; it also includes neurons, which function as computing units

without intrinsic memory. Moreover, the move toward more biologically-inspired computing models opens the door to exploring systems that utilize transient, fading memory—such as in reservoir computing (RC). In these systems, the focus is on dynamic, time-dependent processing rather than long-term memory retention, enabling more efficient computation for tasks like pattern recognition and temporal data processing. This perspective aligns more closely with biological neural systems, where memory and computation are often integrated rather than separate processes. This is precisely why we have used STO-gated MoS_2 FETs to develop a RC platform.

Question #1: How do the authors plan to address in the future the instability of ferroelectric domains in STO at room temperature? Can the authors elaborate more on what specific strategies or mechanisms do they plan to pursue to ensure room temperature synaptic operation in future work? Including more discussion on this direction may help compensate for the lack of room-temperature data. I would also suggest reflecting this in the paper's title to avoid any misleading impressions. Something along the lines of "Multifunctional 2D FETs Exploiting Incipient Ferroelectricity in Freestanding SrTiO3 Nanomembranes at Sub-Ambient Temperatures" might be more appropriate.

The authors would like to thank the reviewer for the remark. It is important to clarify that stable ferroelectric orders at room temperature were not achieved in STO, as these materials exhibit a polar soft mode that does not fully transition to ferroelectricity due to quantum effects that prevent the transition [2]. Furthermore, unlike traditional ferroelectric materials such as HZO and BTO having stable ferroelectric domains, freestanding STO membranes display a weaker long-range correlation among pre-existing nano polar regions, which thermally decay over time [3], leading to unstable polarization switching at 300 K. Hence, to accurately capture the spontaneous polarization, it is crucial to establish stable long-range correlations among the ferroelectric domains throughout the film, a condition that is unlikely to be achieved in incipient ferroelectric STO films. In this context, our future work will focus on engineering strain and/or defects [4-6] in the STO nanomembrane for room temperature memory devices. To elucidate further on the room temperature ferroelectricity in STO films, it must be highlighted that superfine nanodomain engineering method as shown in [6], has successfully induced strong room-temperature ferroelectricity in a $SrTiO_3$-based thin film, a notable example of an incipient ferroelectric system. This achievement was made possible through straightforward modifications in stoichiometry and the introduction of Fe substitution. Moreover, the characterization reveals that the strategic creation of Ti/O vacancies and Fe doping markedly disrupts local symmetry, resulting in high-density, ultrafine polar nanodots. This alteration effectively shifts the intrinsic cubic nonpolar state to a non-centrosymmetric polar state. Hence, the introduction of defects and dopants facilitated a transition from a nonpolar to a polar state, underpinning the ferroelectric transformation. As a part of our future work with STO nanomembranes and integration with MoS_2 FETs, we would introduce Ti/O vacancies and/or Fe doping to attain stable ferroelectric domains in STO.
We have also revised the title of the manuscript to "Multifunctional 2D FETs Exploiting Incipient Ferroelectricity in Freestanding $SrTiO_3$ Nanomembranes at Sub-Ambient Temperatures" as suggested by the reviewer.

*Comment and Question #2:
Material and Device Characterization at Varying Temperatures and Thicknesses – More systematic characterization of the material and device performance, especially in terms of hysteresis at

varying temperatures and thicknesses, would help elucidate the scaling limits of these parameters. Incorporating more details on key ferroelectric parameters, such as remnant polarization, coercive fields and leakage over varying thickness and temperature, could significantly strengthen the manuscript. This would offer a clearer picture of the ferroelectric properties and their degradation with respect to thickness and temperature. Such an analysis should also include a discussion on how variations in membrane thickness uniformity and interfacial defects could impact electrical characteristics and hysteresis.

The authors would like to thank the reviewer for the valuable remark. Based on the reviewers' advice, we have performed electrical characterization on 80 nm thick STO-gated MoS_2 FETs for varying temperatures (50 K, 100 K, 200 K and 300 K) as shown in **Fig. R1a**. The transfer characteristics displays a positive shift in the threshold voltage (V_{th}) as the temperature is reduced to lower values. These findings can be attributed to the reduced carrier concentration (n_s) at lower temperatures, leading to an increase in the V_{th}. Additionally, a counterclockwise hysteresis displaying minimal variations in the hysteresis window, also referred to as the memory window, is evident and illustrated in **Fig. R1b**. Furthermore, the temperature-dependent measurements suggest that the stability in polarization switching is predominantly due to the reduced thermal fluctuations at lower temperatures. Note that, in traditional ferroelectric materials like HZO, where remnant polarization (P_r) decreases with increasing temperature, the memory window similarly reduces [7]. However, in an incipient ferroelectric film such as STO, there is no P_r present, which prevents the establishment of a correlation between temperature and P_r. Hence, based on the experimental data presented in **Fig. R1b** for a representative STO-gated MoS_2 FET, it can be concluded that the memory window remains relatively stable across different temperatures. Notably, as the temperature decreased, we observed a gradual enhancement in the retention of the two memory states as shown in **Fig. 3e-f** in the main manuscript. This suggests that stable polarization switching within the STO nanomembrane becomes more reliable at lower temperatures.

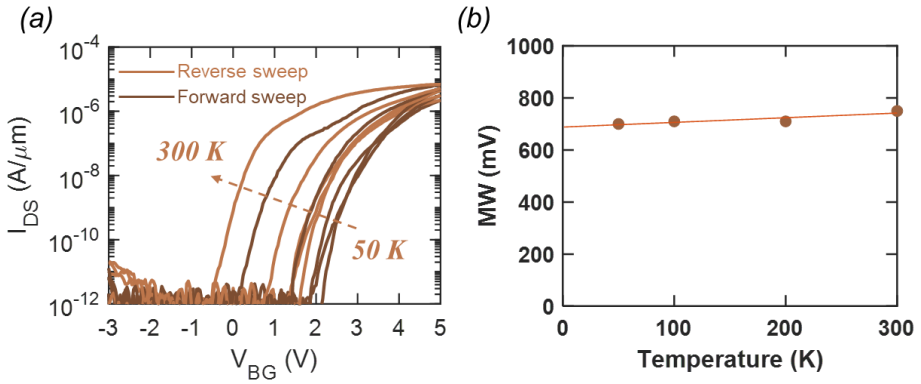

Figure R1. Dependence of memory window on temperature. *a) Dual sweep transfer characteristics of a representative STO-gated MoS_2 FET, measured at T = 50 K, 100 K, 200 K and 300 K. b) MW measured at T = 50 K, 100 K, 200 K and 300 K.*

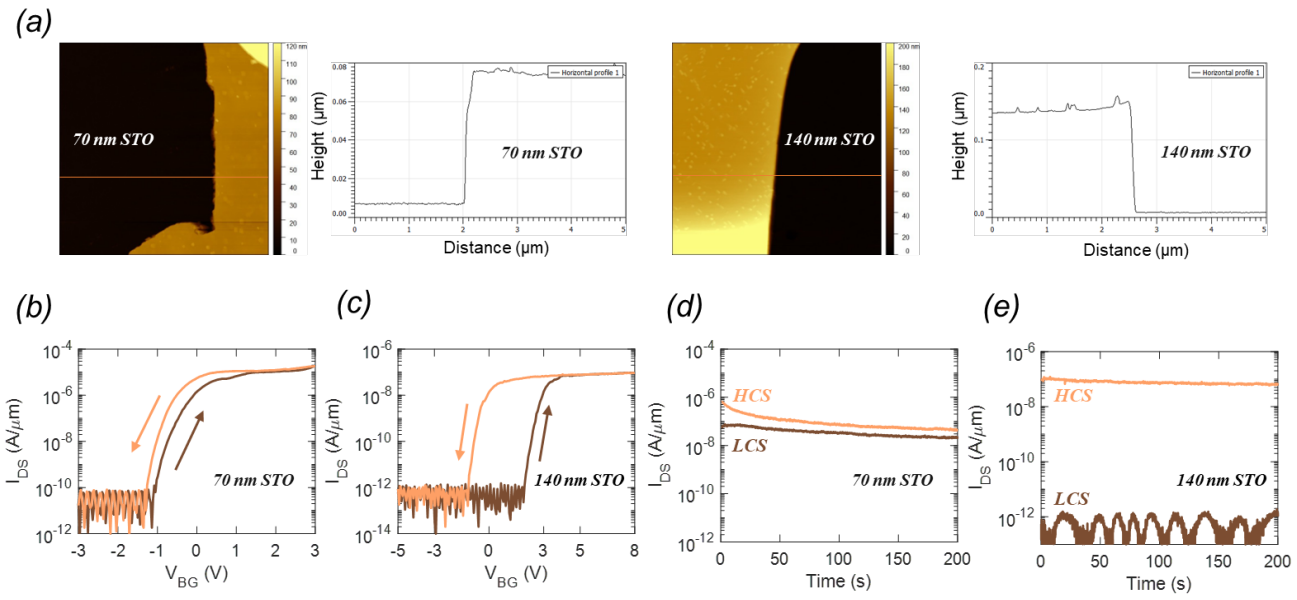

Figure R2. Ferroelectric-like MoS_2 FETs with varying STO thicknesses. *a) The atomic force microscopy (AFM) images of the as-grown STO membranes with thicknesses of 70 nm and 140 nm. Dual sweep transfer characteristics of a representative MoS_2 FET measured at T = 300 K, using STO membranes with thicknesses of b) 70 nm and c) 140 nm. Note that, the transfer characteristics shows counterclockwise hysteresis window for both 70 nm and 140 nm STO-gated MoS_2 FETs, owing to the polarization switching in the STO membrane. d-e) Non-volatile retention of memory states for STO-gated MoS_2 FET at T = 300 K, for different STO thicknesses. The 70 nm STO-gated FETs clearly exhibit non-volatile retention, although a steady decline in the memory ratio is noted. However, the 140 nm thick STO-gated 2D FET shows a larger hysteresis window (> 3 V) and a relatively stable non-volatile retention.*

Additionally, following the reviewer's suggestion regarding the electrical performance with varying membrane thicknesses, a 70 nm and 140 nm STO membrane has been grown epitaxially using hybrid MBE. The atomic force microscopy (AFM) images shown in **Fig. R2a** reveal the physical thicknesses of these membranes. Furthermore, we have performed electrical characterization on MoS_2 FETs equipped with STO nanomembranes of varying thicknesses (70 nm and 140 nm) as shown in **Fig. R2b-c**. Note that, the transfer characteristics (I_{DS} *vs* V_{BG}) shows counterclockwise hysteresis window for both 70 nm and 140 nm STO-gated MoS_2 FETs, owing to the polarization switching in the STO membrane. The variation in the positive and negative back-gate voltage (V_{BG}) ranges can be attributed to the thickness of the STO membrane. Similar to the 80 nm STO-gated MoS_2 FETs, the 70 nm STO-gated FETs clearly exhibit non-volatile retention, although a steady decline in the memory ratio is noted as depicted in **Fig. R2d**. This likely results from the incipient ferroelectric [3, 8] nature of the STO film at room temperature. However, the 140 nm thick STO-gated 2D FET shows a larger hysteresis window (> 3 V) and a relatively stable non-volatile retention as shown in **Fig. R2e**, owing to a significantly less depolarization field, usually observed in a thicker ferroelectric film [9]. It is expected that long-term retention can be achieved for the different thicknesses of STO based 2D FETs at lower temperatures, as already shown in the manuscript for an 80 nm STO ferroelectric-like FET.

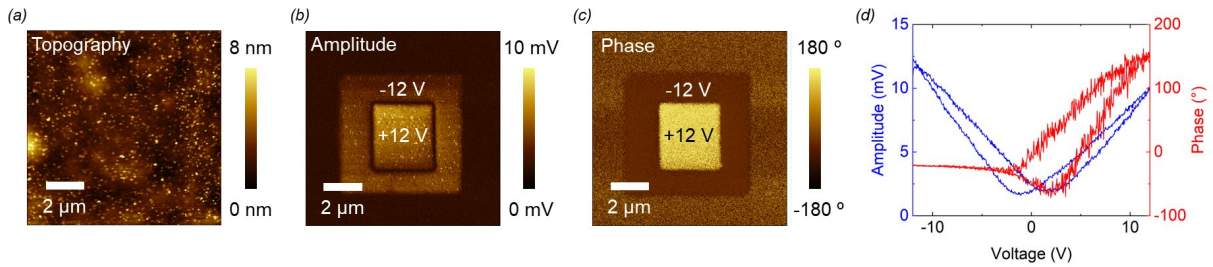

Figure R3. Piezo force microscopy (PFM) of STO nanomembrane. *a) Topography, b) amplitude, and c) phase images of STO film, transferred onto a gold-plated substrate, captured using piezo force microscopy (PFM) at room temperature. These images provide insights into the local electromechanical behavior and the distribution of ferroelectric domains in the out-of-plane direction. d) Amplitude and phase hysteresis loops observed in the STO film on the gold-plated substrate, indicating incipient ferroelectricity at room temperature.*

The authors concur with the reviewers' suggestion about elucidating on the key ferroelectric parameters of STO. In this regard, it is important to note that the incipient ferroelectric nature of STO acted as a barrier to characterizing the capacitors in terms of measuring remnant polarization, coercive fields etc. Unlike traditional ferroelectric materials such as HZO and BTO having stable ferroelectric domains, freestanding STO membranes display a weaker long-range correlation among pre-existing nano polar regions, which thermally decay over time [3], leading to unstable polarization switching at 300 K. Hence, to accurately capture the spontaneous polarization using PE loop measurements, it is crucial to establish stable long-range correlations among the ferroelectric domains throughout the film, a condition that is unlikely to be achieved in incipient ferroelectric STO films. To reaffirm the weak ferroelectric nature of STO, we have obtained piezo force microscopy (PFM) images of the STO film after it was transferred onto a gold-plated substrate at room temperature. **Fig. R3a-c** displays the topography, PFM amplitude, and PFM phase images, respectively. These images reveal details about the local electromechanical properties and the arrangement of weak ferroelectric domains in the out-of-plane direction. **Fig. R3d** depicts domain switching, whereas the unsaturated ferroelectric phase demonstrates its instability, confirming the incipient nature of ferroelectricity at room temperature in STO nanomembranes.

Additionally, to investigate the leakage current in STO-gated MoS_2 FETs, we assessed the characteristics of the back-gate leakage current (I_{BG}) as a function of the back-gate voltage (V_{BG}) is illustrated in **Fig. R4a**. Note that, despite having a relatively small bandgap of approximately ranging from 3.2 to 3.4 eV [10], the 80 nm STO nanomembrane exhibited relatively low I_{BG}, as indicated by the corresponding histograms extracted for V_{BG} = 3 V and -3 V in **Fig. R4b**.
It is noteworthy to mention that epitaxially grown thin films have uniform thicknesses as shown in [11]. However, to verify the uniformity of the thicknesses of STO nanomembranes, we have conducted atomic force microscopy (AFM) on a few representative devices having 80 nm STO film. Furthermore, the AFM images are shown in **Fig. R5,** which reveal that the physical thicknesses of these membranes are nearly uniform throughout all the devices. The observed device-to-device variation in the transfer characteristics of the 2D FETs shown in **Fig. 2f** can be

attributed to residues and wrinkles introduced during the 3D and 2D membrane transfer processes involving PDMS and PMMA, respectively.

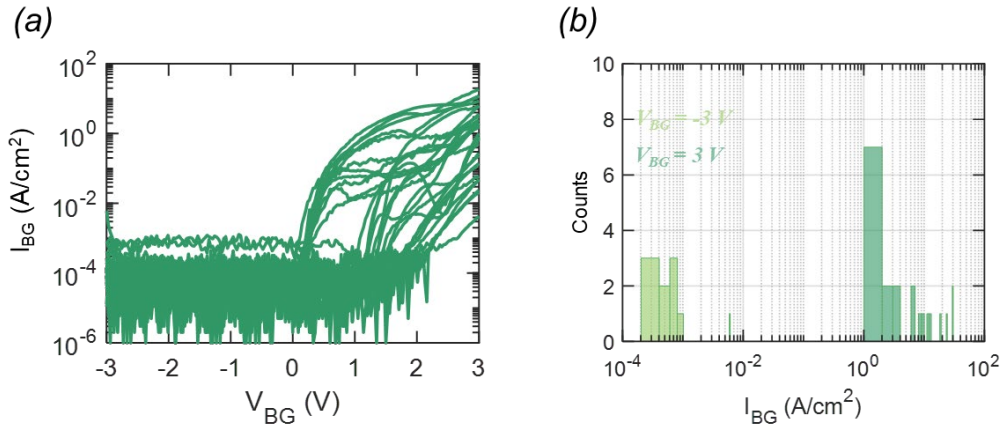

Figure R4. Gate leakage current in STO-gated MoS_2 FETs. *a) The back-gate leakage current density (I_{BG}) as a function of the back-gate voltage (V_{BG}) for a constant source-to-drain bias of V_{DS} = 1 V, for 30 STO-gated MoS_2 FETs. b) I_{BG} extracted at V_{BG}=-3V (light green) and V_{BG}=-3V (shown in dark green) for 30 STO-gated MoS_2 FETs.*

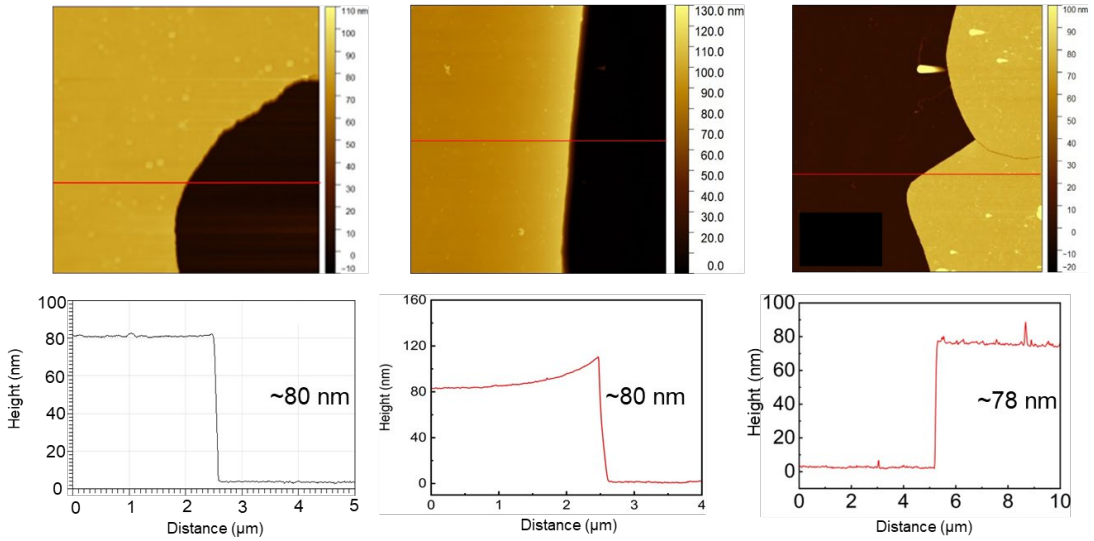

Figure R5. *The atomic force microscopy (AFM) images of the transferred STO membranes show a consistent physical thickness across multiple devices.*

Additionally, the large *SS* values of the STO-gated MoS_2 FETs suggests that a significant number of interfacial defects are present at the MoS_2/STO interface. To further elucidate on the interfacial defects and its impact on the hysteresis, we conducted voltage sweep-rate (t_{sweep}) dependent measurements on these FETs. **Fig. R6a** shows the transfer characteristics at different temperatures, T = 200 K, 100 K and 15 K with t_{sweep} varying from 2 ms (fastest) to 10 s (slowest). The hysteresis dependency on t_{sweep} indicates whether the width of hysteresis is influenced by slow or fast traps, present at the MoS_2/STO interface. Note that reducing the t_{sweep} leads to an increase in V_{Hyst}, suggesting that traps with slower time constants, play a more significant role in charge trapping [12]. On the contrary, if the gate insulator exhibits ferroelectric order, the hysteresis window would

remain, as polarization switching is not strongly dependent on t_{sweep}. **Fig. R6b** shows the memory or hysteresis window as a function of t_{sweep} for T = 200 K, 100 K and 15 K. It is evident that the memory window predominantly remains constant as the t_{sweep} varied. Hence, it can be stated that the counterclockwise hysteresis in the STO-gated MoS_2 FETs has originated from the incipient ferroelectric nature of the STO nanomembranes.

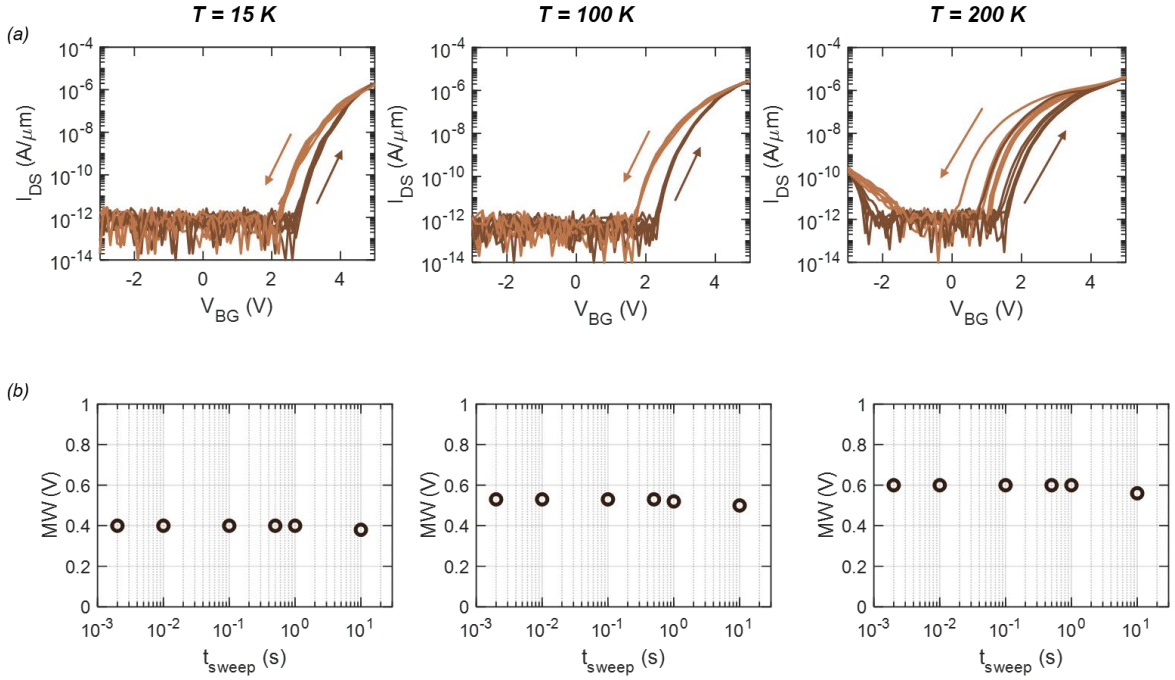

Figure R6. Sweep-rate dependent measurement of STO-gated MoS_2 FET. a) *Transfer characteristics at different temperatures with a t_{sweep} range varying from 2 ms to 10 s.* ***b)*** *MW as a function of t_{sweep} for T = 15 K, 100 K and 200 K, respectively.*

Comment and Question #3: Based on such an analysis, can the authors better elaborate on the scaling limits of their proposed freestanding 3D $SrTiO_3$ and 2D MoS_2 nanomembranes for neuromorphic hardware, particularly with respect to thickness, voltage, and temperature? I appreciate that the authors have already compared their material and devices with the state of the art in table, which is a very good and convincing step.

The authors would like to thank the reviewer for the valuable remark. It is important to note that there is a direct correlation between scaling down the voltage and reducing the thickness of the membrane. STO membranes of 70 nm and 140 nm thickness have been epitaxially grown using hybrid molecular beam epitaxy (MBE). Electrical characterizations were conducted on MoS_2 field-FETs incorporating STO nanomembranes of these specific thicknesses, as illustrated in **Fig. R2b-c**. The transfer characteristics of both the 70 nm and 140 nm STO-gated MoS_2 FETs exhibit a counterclockwise hysteresis window, indicative of polarization switching within the STO membrane. **Fig. R2b-c** illustrates that the switching voltages required for maximum MW decreases from 8 V in 140 nm thick STO to 3 V in 70 nm thick STO. Consequently, the MW also reduces from 4 V to 0.5 V, respectively. However, for neuromorphic hardware, we have utilized the minor

loops observed in the transfer characteristics of STO-gated MoS_2 FETs to demonstrate multi-bit memory storage in a single device. The emergence of these minor loops shown in **Fig. 4a-b** in the manuscript, is due to the partial polarization switching of ferroelectric domains under the semiconducting channel, which can be attributed to the random domain switching dynamics in ferroelectric materials. Nevertheless, it is important to mention that these freestanding STO membranes can be further thinned down to thicknesses of 20 nm or even less [13]. Additionally, incorporating these thin STO membranes with large area 2D materials will be a focus of our future research. As a part of our future work with STO nanomembranes and integration with MoS_2 FETs, we would introduce Ti/O vacancies and/or Fe doping to attain stable ferroelectric domains in STO [6]. Hence, understanding the ferroelectric properties of a stable STO membrane will be enhanced by clearly defining the scaling limits of thickness and voltage.
Furthermore, as we scale down the temperature up to 15 K, we have observed a gradual enhancement in the retention of the two memory states. This suggests that stable polarization switching within the STO nanomembrane becomes more reliable at lower temperatures, supported by the temperature dependent SHG results as shown in **Fig. 3e-g**. We also thank the reviewer for the appreciation towards the benchmarking table.

*Comment and Question #4:
Demonstrating Neuromorphic Functionality at Low and Room Temperatures – It would be helpful if the authors could more convincingly support neuromorphic functions of the STO-gated MoS_2 FET at both low and room temperatures.

The authors value the reviewer's insights regarding the neuromorphic functions of the STO-gated MoS_2 FET at both low and room temperatures. In this context, we have added a concise discussion on the current plots for potentiation and depression of the STO-gated MoS_2 FET at 100 K and 15 K, which are sub-ambient temperatures. Additionally, we provide a detailed discussion on the RC hardware functioning at room temperature to further elaborate on the neuromorphic functions.

*Comment and Question #5: I appreciate the authors' effort in exploiting room-temperature non-retentive polarization switching in the STO-gated MoS_2 FET to construct a physical reservoir for accelerating reservoir computing (RC). As the authors have shown excellent retention and ferroelectric behavior at 100 K, could they also demonstrate whether the STO-gated MoS_2 FET can provide potentiation and depression current plots for use as a synaptic ferroelectric device at 100 K? Have the authors attempted such experiments to strengthen their claim for neuromorphic hardware, even if the device only works at low temperatures? A bit more detailed and critical description and discussion of the potential applications, if any, of the proposed material not limited to RC, would be useful.

We appreciate the reviewers' recognition of the effort in constructing RC hardware by exploiting room-temperature non-retentive polarization switching, and the comprehensive experimental results presented in our manuscript.
We want to clarify that we are not proposing the use of this device as a neuromorphic computing primitive at low temperatures. Instead, we believe STO-based FeFETs can serve as cryogenic memory devices at low temperatures. We have provided all the necessary characterization to validate their use as cryogenic memory devices. Therefore, we do not see the need to demonstrate

long-term potentiation (LTP) and depression (LTD) in STO-gated MoS_2 FETs at lower temperatures. It is well established that cryogenic computing and memory components are vital, especially in space electronics and quantum computing development. Conventional superconducting memories often face limitations in terms of memory density and energy efficiency. Recently, a Si-doped HfO_2 FeFET cryogenic memory was demonstrated, operating at 6.9 K with a large memory window even at lower temperatures [1]. In this context, we explore the potential of developing a cryogenic memory system by leveraging the stable ferroelectric properties in STO-gated MoS_2 FETs at low temperatures.

Reviewer #3 (Remarks to the Author):

The authors revision of the state of the art in the introduction, although improved, is still lacking quite some breakthroughs in this field.

The authors would like to thank the reviewer for the remark. We have now added all the appropriate references to the revised manuscript and highlighted the breakthroughs in the field.

References:

[1] Z. Wang, H. Ying, W. Chern, S. Yu, M. Mourigal, J. D. Cressler*, et al.*, "Cryogenic characterization of a ferroelectric field-effect-transistor," *Applied Physics Letters,* vol. 116, 2020.

[2] M. Jiang, M. Trigo, I. Savić, S. Fahy, É. D. Murray, C. Bray*, et al.*, "The origin of incipient ferroelectricity in lead telluride," *Nature Communications,* vol. 7, p. 12291, 2016.

[3] Y. Zhang, J. Li, K. Yang, F. Zheng, Y. Zhou, Y. Zhang*, et al.*, "Room-temperature electric field-induced out-of-plane ferroelectric polarization in strain-free freestanding 2D SrTiO3 membranes," *APL Materials,* vol. 11, 2023.

[4] R. Xu, J. Huang, E. S. Barnard, S. S. Hong, P. Singh, E. K. Wong*, et al.*, "Strain-induced room-temperature ferroelectricity in SrTiO3 membranes," *Nature communications,* vol. 11, p. 3141, 2020.

[5] J. Liu, Y. Cao, Y.-L. Tang, Y.-L. Zhu, Y. Wang, N. Liu*, et al.*, "Room-Temperature Ferroelectricity of Paraelectric Oxides Tailored by Nano-Engineering," *ACS Applied Materials & Interfaces,* vol. 15, pp. 4226-4233, 2023.

[6] T. Li, J. Yang, S. Deng, Z. Wang, M. Tang, H. Luo*, et al.*, "Superfine Nanodomain Engineering Unleashing Ferroelectricity in Incipient Ferroelectrics," *Journal of the American Chemical Society,* 2024.

[7] S. Chatterjee, S. Kumar, A. Gaidhane, C. K. Dabhi, Y. S. Chauhan, and H. Amrouch, "Temperature-and variability-aware compact modeling of ferroelectric FDSOI FET for memory and emerging applications," *Solid-State Electronics,* p. 108954, 2024.

[8] I. Sokolović, M. Schmid, U. Diebold, and M. Setvin, "Incipient ferroelectricity: A route towards bulk-terminated SrTiO 3," *Physical Review Materials,* vol. 3, p. 034407, 2019.

[9] K.-H. Kim, S. Oh, M. M. A. Fiagbenu, J. Zheng, P. Musavigharavi, P. Kumar*, et al.*, "Scalable CMOS back-end-of-line-compatible AlScN/two-dimensional channel ferroelectric field-effect transistors," *Nature Nanotechnology,* pp. 1-7, 2023.

[10] A. J. Yang, K. Han, K. Huang, C. Ye, W. Wen, R. Zhu*, et al.*, "Van der Waals integration of high-κ perovskite oxides and two-dimensional semiconductors," *Nature Electronics,* vol. 5, pp. 233-240, 2022.

[11] S. Varshney, S. Choo, L. Thompson, Z. Yang, J. Shah, J. Wen*, et al.*, "Hybrid Molecular Beam Epitaxy for Single-Crystalline Oxide Membranes with Binary Oxide Sacrificial Layers," *ACS nano,* 2024.

[12] N. H. Patoary, F. A. Mamun, J. Xie, T. Grasser, and I. Sanchez Esqueda, "Analysis and EOT Scaling on Top-and Double-Gate 2D CVD-Grown Monolayer MoS2 FETs," *Advanced Electronic Materials,* p. 2400152.

[13] J.-K. Huang, Y. Wan, J. Shi, J. Zhang, Z. Wang, W. Wang*, et al.*, "High-κ perovskite membranes as insulators for two-dimensional transistors," *Nature,* vol. 605, pp. 262-267, 2022.

Reviewer #3

In the confidential remarks to the editor, Reviewer #3 raises concerns on lacking references published by European authors in this field of freestanding complex oxides. Please consider including the relevant references inferred by Reviewer #3.

We thank the reviewer for the suggestions. In the revised final version of the manuscript, we have included relevant references for freestanding complex oxides published by European authors.

References:

[10] Y. Li *et al.*, "Stacking and twisting of freestanding complex oxide thin films," *Advanced materials,* vol. 34, no. 38, p. 2203187, 2022.

[11] R. T. Dahm *et al.*, "Size-controlled spalling of LaAlO3/SrTiO3 micromembranes," *ACS applied materials & interfaces,* vol. 13, no. 10, pp. 12341-12346, 2021.

[12] Z.-D. Luo, J. J. Peters, A. M. Sanchez, and M. Alexe, "Flexible memristors based on single-crystalline ferroelectric tunnel junctions," *ACS applied materials & interfaces,* vol. 11, no. 26, pp. 23313-23319, 2019.

[13] B. Zhang, C. Yun, and J. L. MacManus-Driscoll, "High yield transfer of clean large-area epitaxial oxide thin films," *Nano-Micro Letters,* vol. 13, pp. 1-14, 2021.