Supplementary Information for

High-density three-dimensional integration of dynamic random-access memory using vertical dual-gate IGZO TFTs

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#These authors contributed equally to this work.

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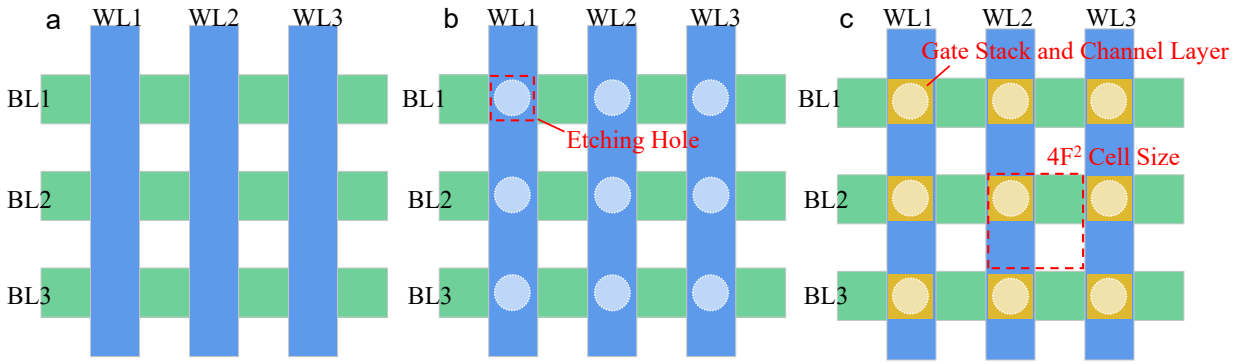
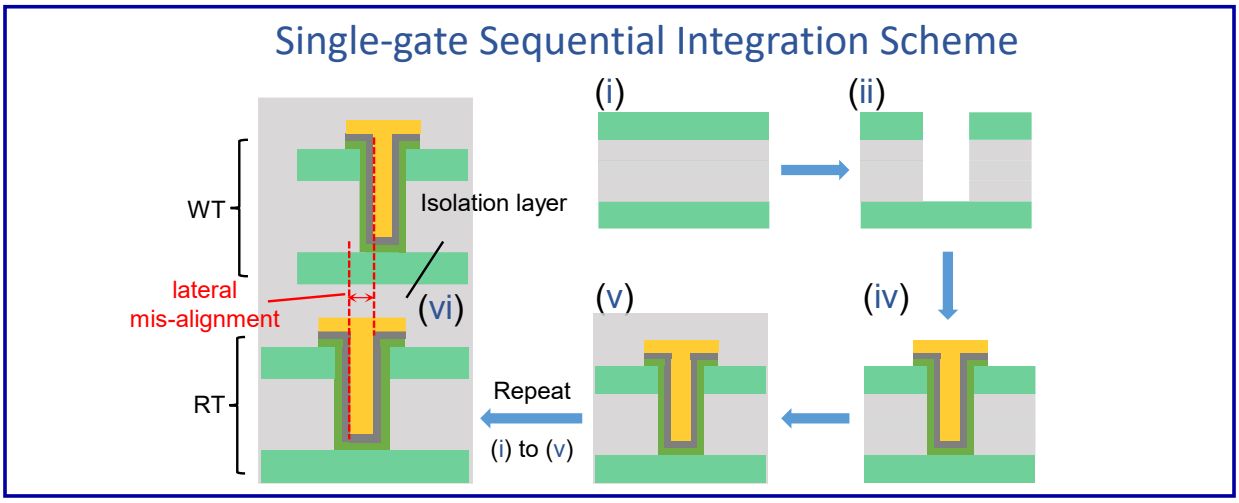
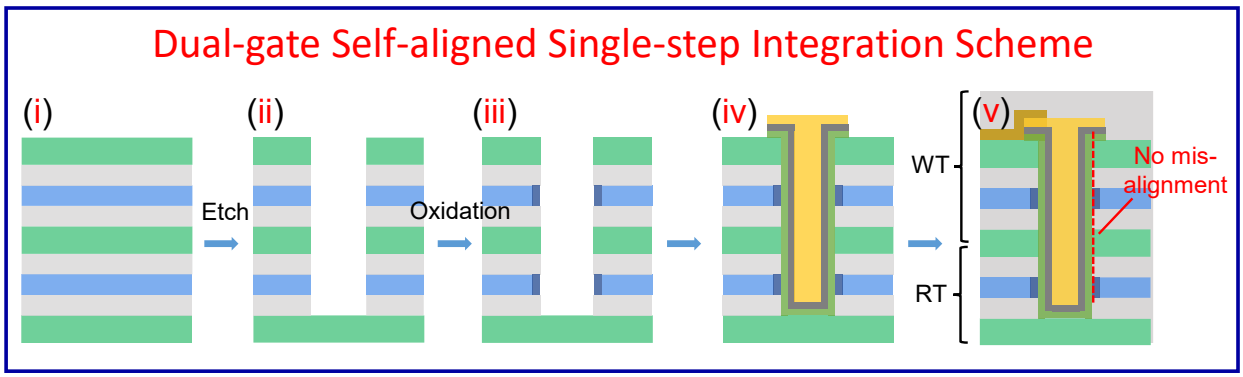
Supplementary Figure:

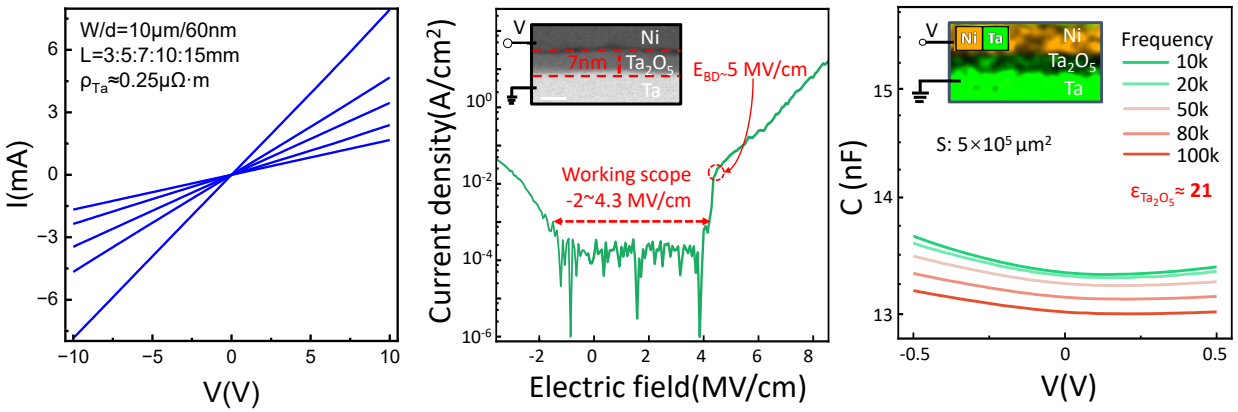


Supplementary Figure 1. Layout design of vertical DG 2T0C array. a, the array framework of the crossbar structure. **b,** the etching holes define the circular channel area. **c,** the deposition for the gate stack and channel layer along the etching hole. The layout design of the array shows that two WLs and BLs form a crossbar structure, with the etching holes defining the sidewalls at the intersections. The gate stack and channel layer (IGZO/HfO_2/IZO) are deposited in single ALD process and patterning under one mask which is shown in the yellow region.

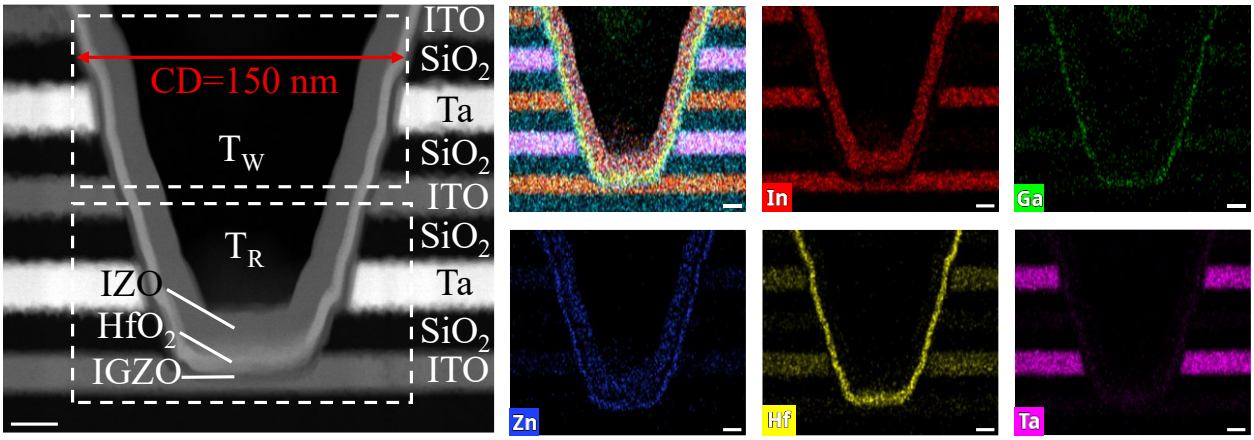




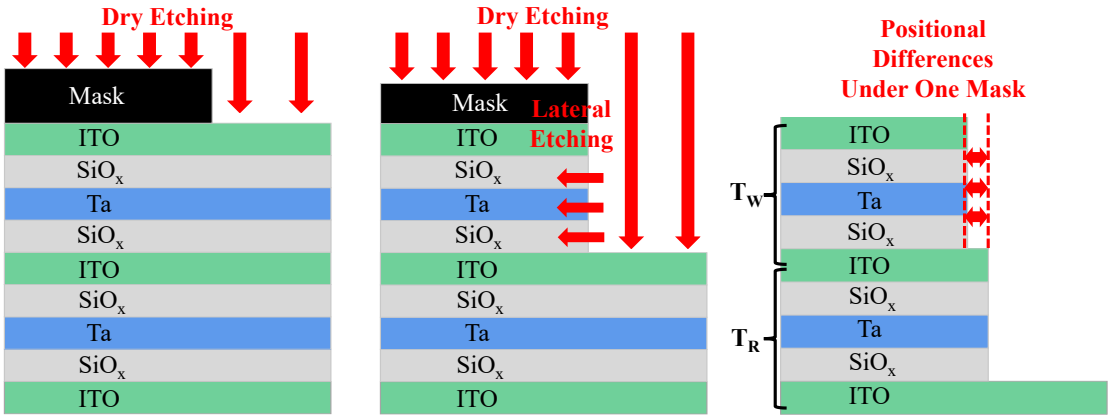
Supplementary Figure 2. Schematic and fabrication flow of 3D-stack DRAM scheme. a, Single-gate sequential integration scheme with lateral misalignment result from photolithography deviation. **b,** DG SASS process flow without lateral misalignment.



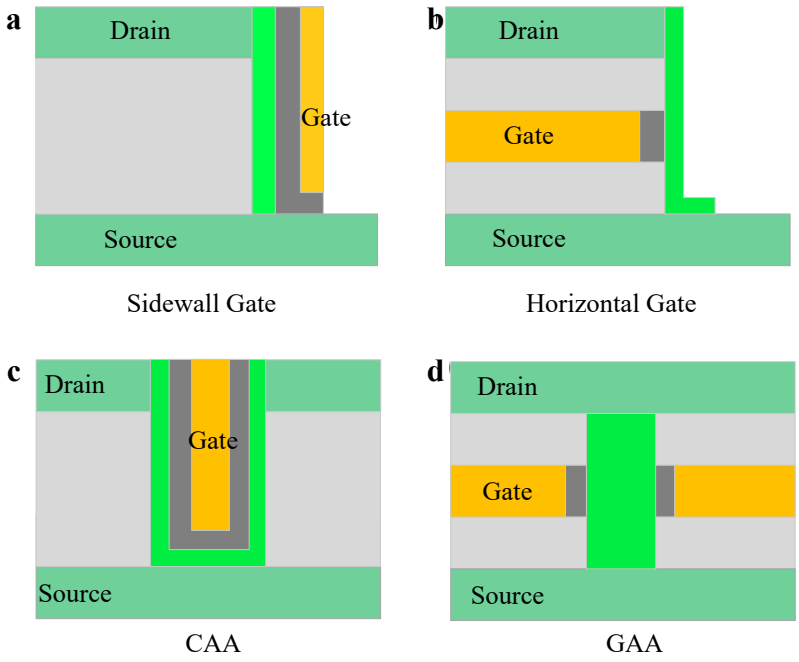
Supplementary Figure 3. Electrical characterization of Ta metal gate and Ta_2O_5 gate oxide. **a,** I-V test for Ta metal line. Low resistivity of 25μΩ.cm is achieved. **b,** I-V test on flat capacitors with 7nm in-situ O_3 oxidation Ta_2O_5 as insulator indicating low leakage current and high breakdown field. **c,** C-V test show high-k of 25 for in-situ O_3 oxidation Ta_2O_5 with ~1.5 nm EOT.



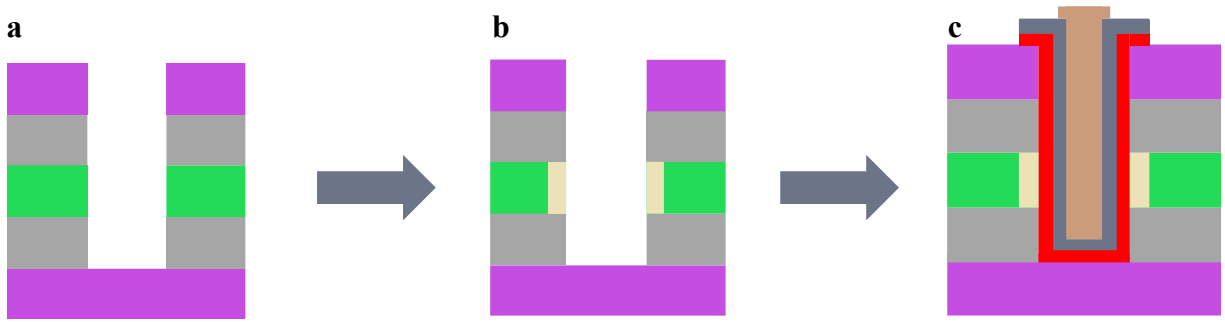
Supplementary Figure 4. a, b TEM images and EDX mappings for the DRAM cell in **Fig. 1b**. Scale bar, 20 nm.



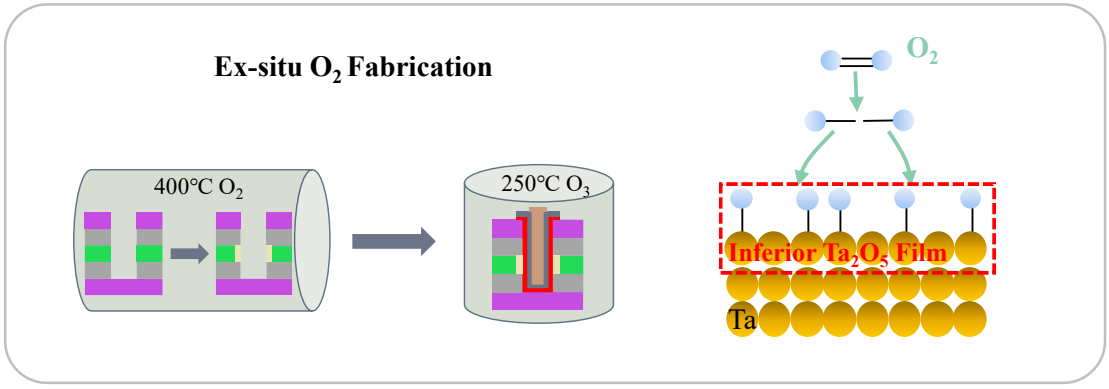
Supplementary Figure 5. Detailed process steps for vertical DG 2T0C cell which clarify the positional differences observed in the **Fig. 1e**. The positional differences between T_R/T_W possibly originate from the sidewall dry etching process. Specifically, we use one mask to etch both T_R and T_W. When the etching process goes to the bottom layer device, there exists a slight lateral over etching to the upper layer because of the small etching selectivity which results in the positional differences between T_R and T_W. This issue could be addressed by optimizing the dry etch process like applying a large etching selectivity process in the up/bottom layer.



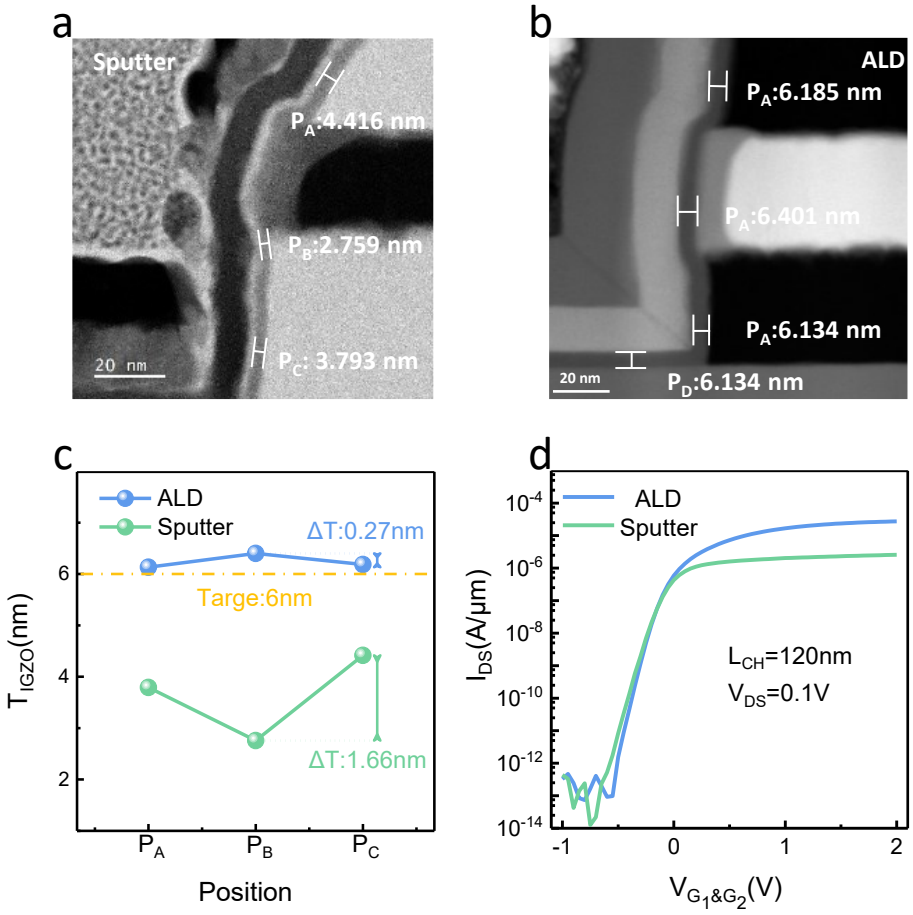
Supplementary Figure 6. Gate structures in vertical TFTs. a, sidewall gate. **b**, horizontal gate. **c**, CAA. **d**, GAA. For comparisons between gate-all-around geometries and SG, DG structure, there exist a trade-off between channel control ability and fabrication complexity. Although vertical GAA structure can achieve the best performance with its gate-all-around topology, the fabrication cost of vertical devices make it hard to scale to large arrays. On the other hand, our vertical DG 2T0C cell enabled by the self-aligned single step process proposed in this work can be fabricated with less cost and achieves more reliable read operation by the DG control which the GAA cannot offer.



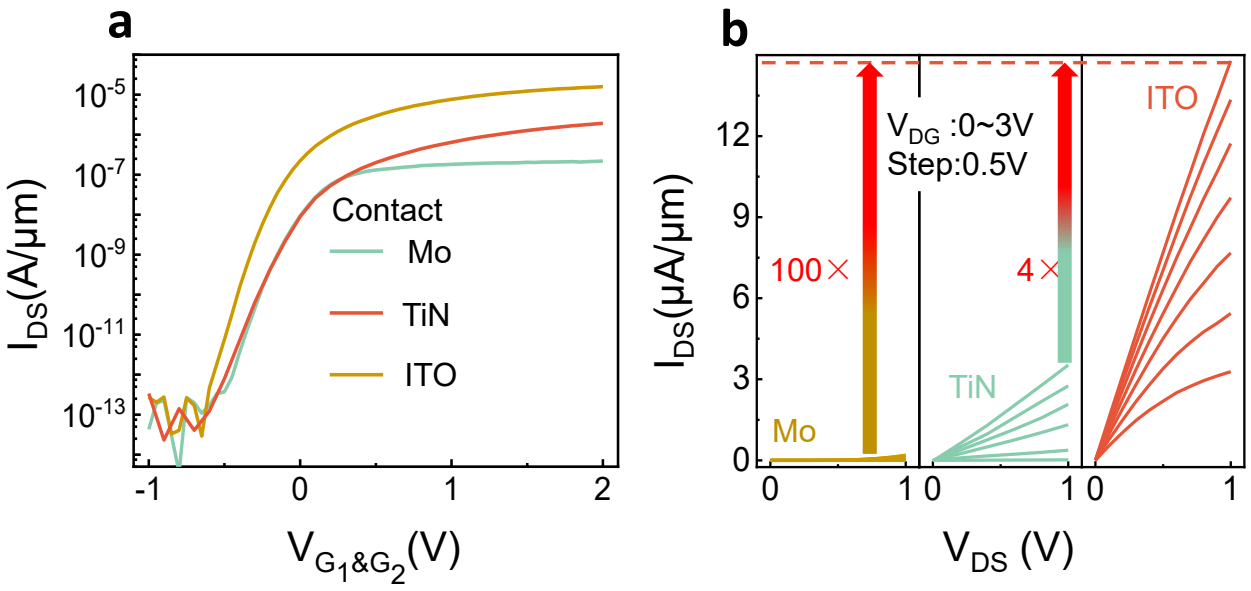
Supplementary Figure 7. Self-oxidation fabrication process. a, multi-layer depositing and hole etching. **b,** Ta metal gate self-oxidation to form High-k Ta_2O_5 insulator. **c,** ALD IGZO and second gate stack.



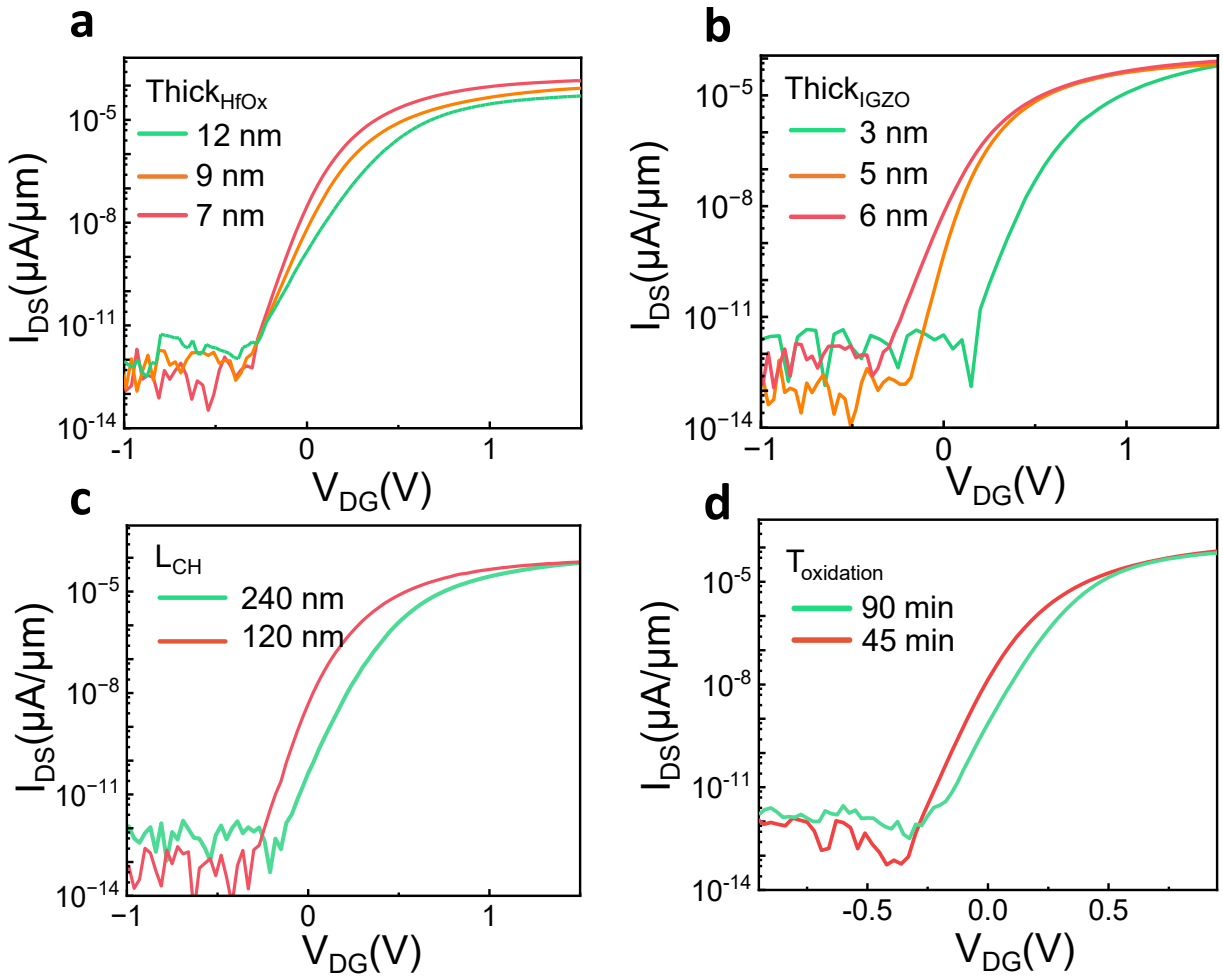
Supplementary Figure 8. Flow of ex-situ self-oxidation fabrication process. The self-oxidation and ALD step are performed separately and ex-situ result in an unsatisfactory interface quality.



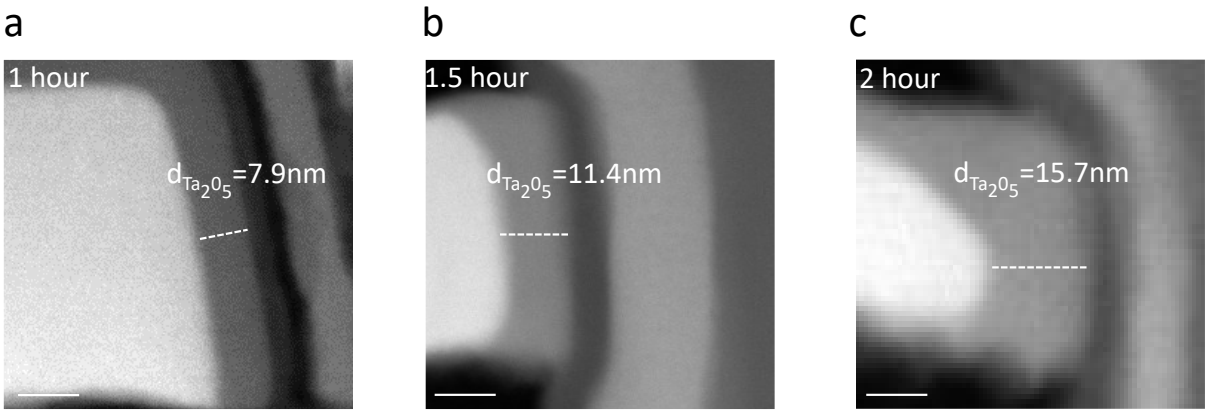
Supplementary Figure 9. The impact of channel deposition methods on device performance. TEM image of morphology of 6nm IGZO film deposited by **a,** putter and b**,** ALD **c**, Extracted thickness of IGZO film along the channel direction on sidewall. ALD deposited IGZO layer shows more uniform thickness and the actual thickness shows no decreases compared to the target thickness. **d**, corresponding transfer curves with channel deposited by ALD and sputter.



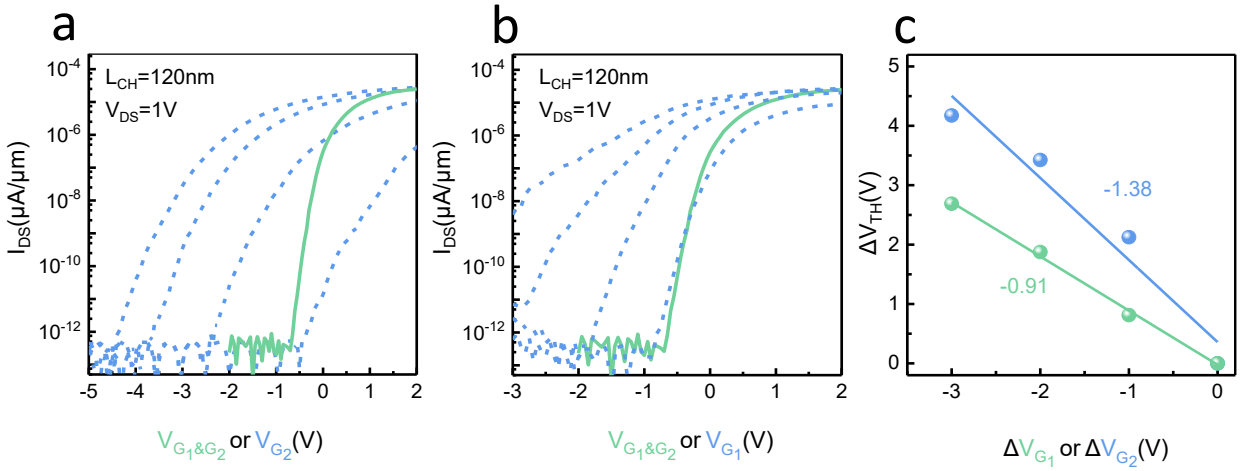
Supplementary Figure 10. Contact optimized of DG IGZO VCT. a,b, Transfer and out characteristic of DG IGZO VCTs fabricated with different contact metal. The device with ITO S/D contact exhibits remarkable improvement in I_{ON} by 100x and 4x compared to the Mo and TiN, respectively. The possible reason is that ITO effectively prevents further oxidation during SASS heat treatment and the following ALD process.



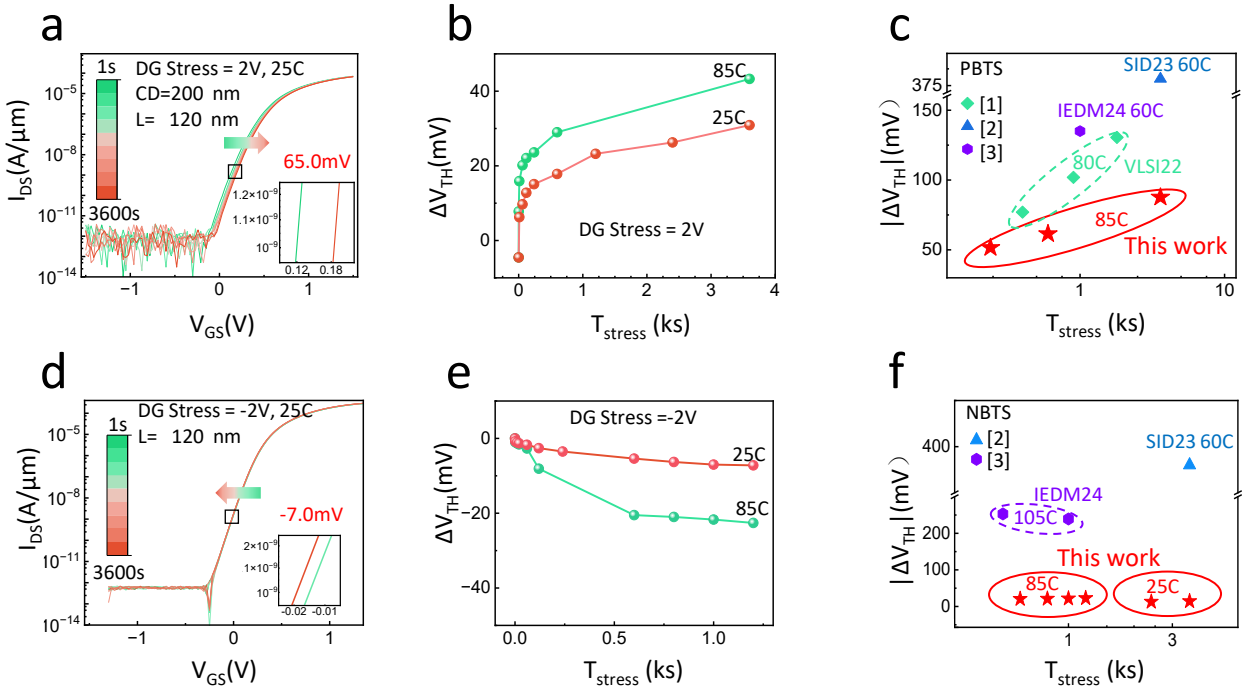
Supplementary Figure 11. Device scaling of **a,** channel length **b,** channel width, gate insulator of **c,** ALD HfO_2 and **d,** self-oxidation Ta_2O_5. The performance changes during the scaling process are universal, which indicates the good scalability.



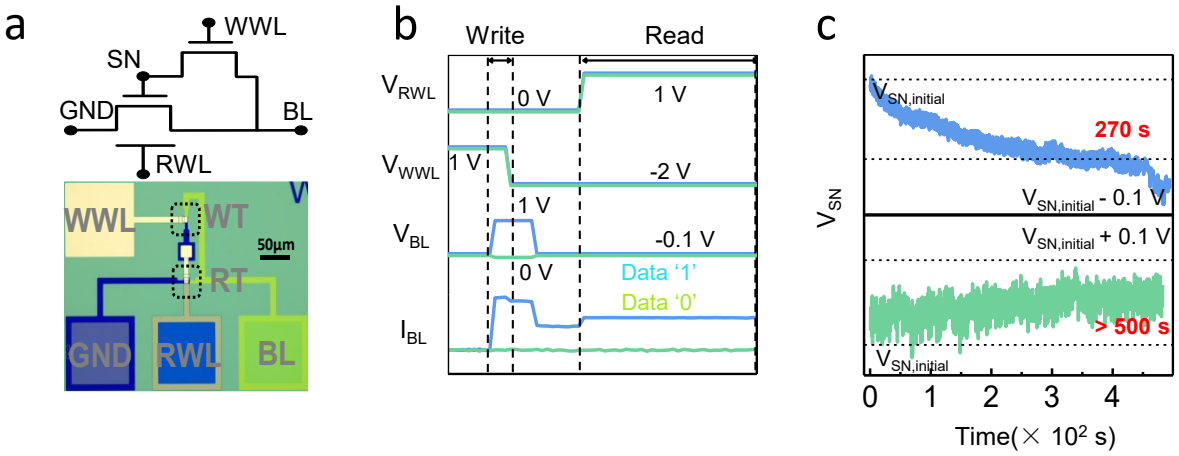
Supplementary Figure 12. Process time in in-situ self-oxidation process. TEM image in the channel region of Ta layer under different oxidation time of **a,** 1h **b,** 1.5h and **c,** 2h. Scale bar, 10nm.



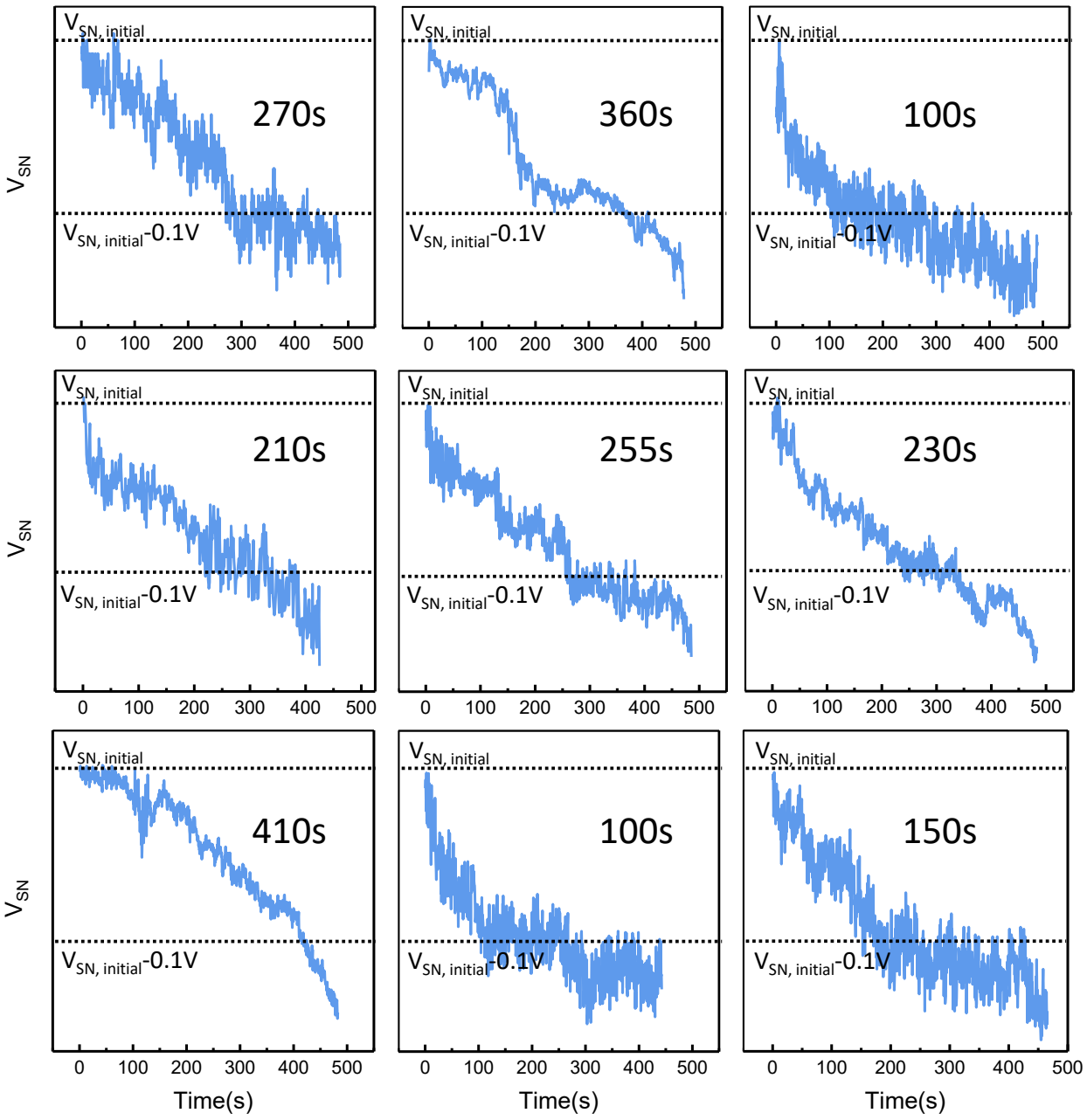
Supplementary Figure 13. V_{TH} modulation function of vertical DG device. a,b transfer curves in dual gate sweep(red line) and single gate sweep(blue line). **a,** OG sweep with V_{IG} varies from -1V to 2V in 1V step. **b,** IG sweep with V_{OG} varies from -1V to 2V in 1V step. **c**, Corresponding threshold voltage shift (ΔV_{TH}) vs. ΔV_{IG} or ΔV_{OG} extracted from **a,b**



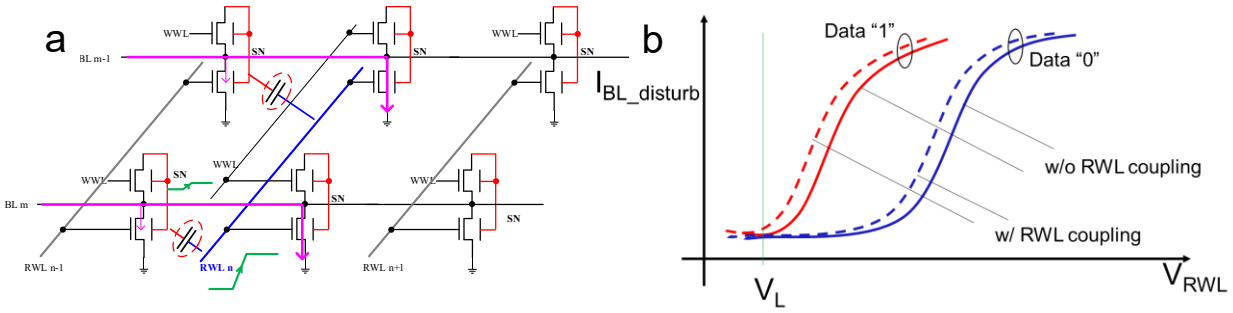
Supplementary Figure 14. Thermal stability of IGZO DG VCTs. a, PBS characteristics after 2V DG stress for 1 hour at 25℃ achieving 65 mV V_{TH} shift. **b,** ΔV_{TH} comparison at 25℃ and 85℃ after 2V DG stress for 1 hour. **c,** Benchmark comparison of PBTS with similar reported IGZO VTFTs. **d,** NBS characteristics after -2V DG stress for 1 hour at 25℃ achieving -7 mV V_{TH} shift. **e,** ΔV_{TH} comparison at 25℃ and 85℃ after -2V DG stress for 1 hour. **f,** Benchmark comparison of NBTS with similar reported IGZO VTFTs.



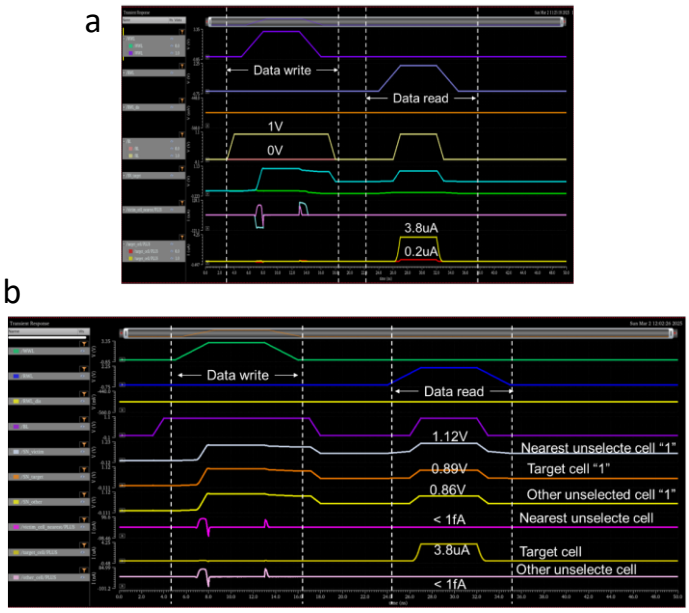
Supplementary Figure 15. Planar interconnect DG 2T0C DRAM bit-cell. **a,** circuit schematic and optical image. **b,** Timing diagram of read/write operation and V_{SN} respond of data '1' and data '0'. **c,** Retention time of data '1' and data '0'. 270s and over 500s retention time for data '1' and data '0' is achieved.



Supplementary Figure 16. Additional retention time characteristic of Vertical DG DRAM cell.



Supplementary Figure 17 Read disturb due to RWL-SN coupling in 2T0C array. a, schematic of the RWL-SN coupling . **b,** dual-gate read strategy to reduce the current disturbance**.**



Supplementary Figure 18 Simulation result of array operation and parasitic analysis for 2T0C array operation. a, Array operation. **b,** Parasitic analysis. The result indicating that our $4F^2$ DG 2T0Ccell can achieve array level read/write operation and showing no obvious current disturbance

Supplementary Table:

Ref.	*Channel*	L_{CH} (nm)	I_{ON}(A/μm)@V_{DS}	*SS*(mV/dec)	*Structure*
[17]	ZnO	500	*0.25	400	Sidewall Gate
[18]	InO	500	*7.5@2.1V	130	Sidewall Gate
			*2.7@2.1V	240	
		1000	*0.54@2.1V	250	
[19]	IGZO	250	*3.3	460	Sidewall Gate
			*0.33	840	
[20]	MoS2	1000	*0.075	151	Horizontal gate
[21]	IGZO	1100	*0.67	200	Horizontal gate
[22]	IAZO	100	*0.39	80	GAA
[23]	IGZO	50	4.07	109	CAA
[24]	IGZO	55	32.8	92	CAA
[25]	IGZO	50	*0.24	230	CAA
[26]	IGZO	170	*0.59	290	Sidewall Gate
			*1.6	380	
			*0.1	430	
[27]	InO/IGZO	500	*5.5@2.1V	120	Sidewall Gate
			*3.0@2.1V	140	
[28]	IGZO	500	*8.0	79.4	CAA
[29]	IGZO	500	*0.06	600	Sidewall Gate
This work	IGZO	120	45.2	68	Dual Gate
			38.1	79.4	

Supplementary Table 1. Comparison of key metrics of state-of-the-art vertical TFTs.

"*" is the extracted data from the figures in Ref.

Supplementary Table 2. Benchmark of representative AOS-based 2T0C DRAM cells.

Ref.	*Channel*	*Retention* (s) (0.1V V_{SN} drop)	*Cell Inter-connection*	*RT&WT Structure*	*Dual-gate Read*	*Cell Deviation*
[23]	IGZO	190	Planar	Vertical CAA	N	N.A.
[25]	IGZO	300	Planar	Vertical CAA	N	N.A.
[30]	IGZO	75	3D stack	Vertical CAA	N	Y
[31]	IGZO	>1500	Planar	Planar DG	Y	N.A.
[32]	IWO	*40(85C) *130(50C) *200(25C)	Planar	Planar DG	N	N.A.
[33]	IGZO	1000 (0.4V V_{SN} drop)	Planar	Planar SG	N	N.A.
[34]	IGZO	77 180 220	Planar	Planar SG	N	N.A.
[35]	IGZO	>400	Planar	Planar SG	N	N.A.
[36]	IGZO	~13	Planar	Planar SG	N	N.A.
[37]	IGZO	>16000	Planar	Planar SG	N	N.A.
[38]	IGZO	>1000	Planar	Planar SG	N	N.A.
[39]	IGZO	>300	Planar	Planar DG	Y	N.A.
[40]	ITO	>200	Planar	Planar SG	N	N.A.
[41]	TiO	400	Planar	Planar SG	N	N.A.
[42]	IGZO/CNT	170	Planar	Planar SG	N	N.A.
[43]	IGZO	>28800 >90000 (50% V_{SN} drop)	Planar	Planar SG	N	N.A.
[44]	ITO	2250	Planar	Planar SG	N	N.A.
[45]	IGZO	10000(RT) 7000(85 C)	Planar	Planar SG	N	N.A.
This work	IGZO	470	3D stack	Vertical DG	Y	N

Supplementary References:

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