Supporting Information

Coupled Ferroelectric-Anisotropic Optoelectronic Synapse for Polarization-Sensitive Neuromorphic Vision

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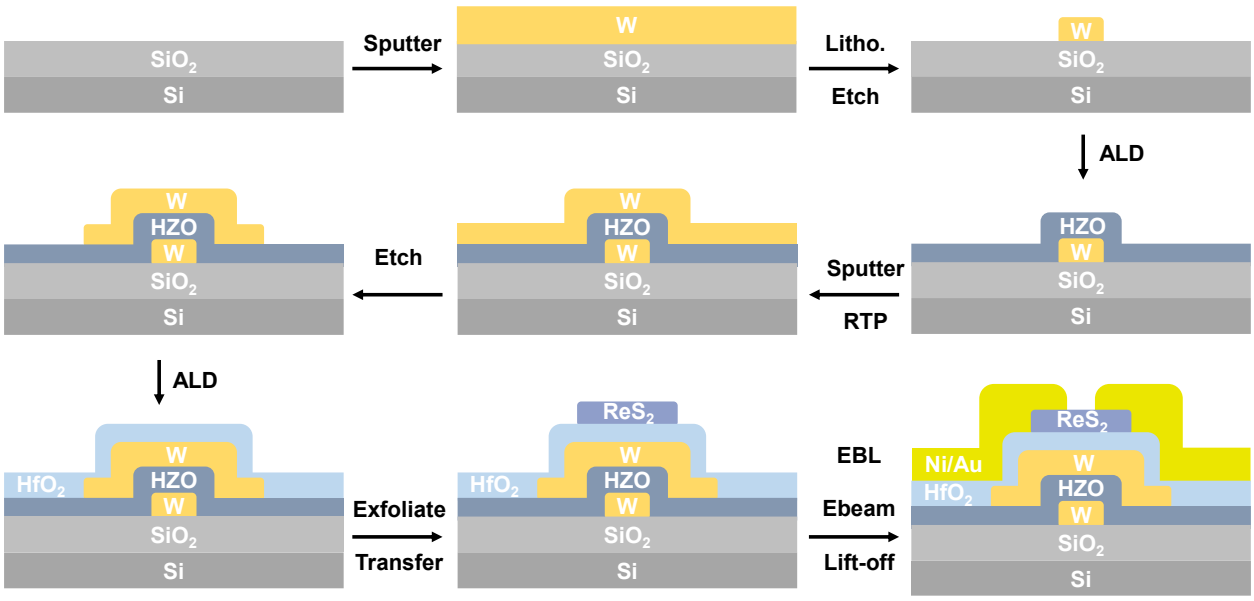
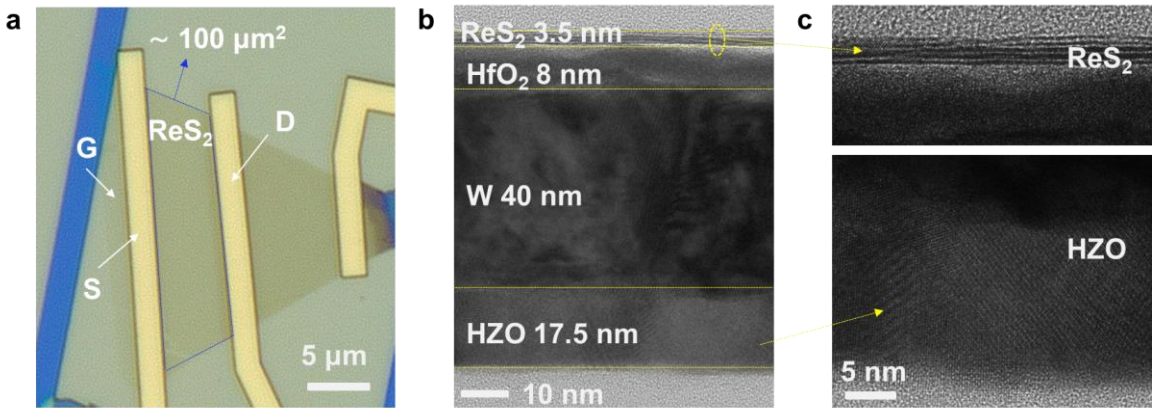
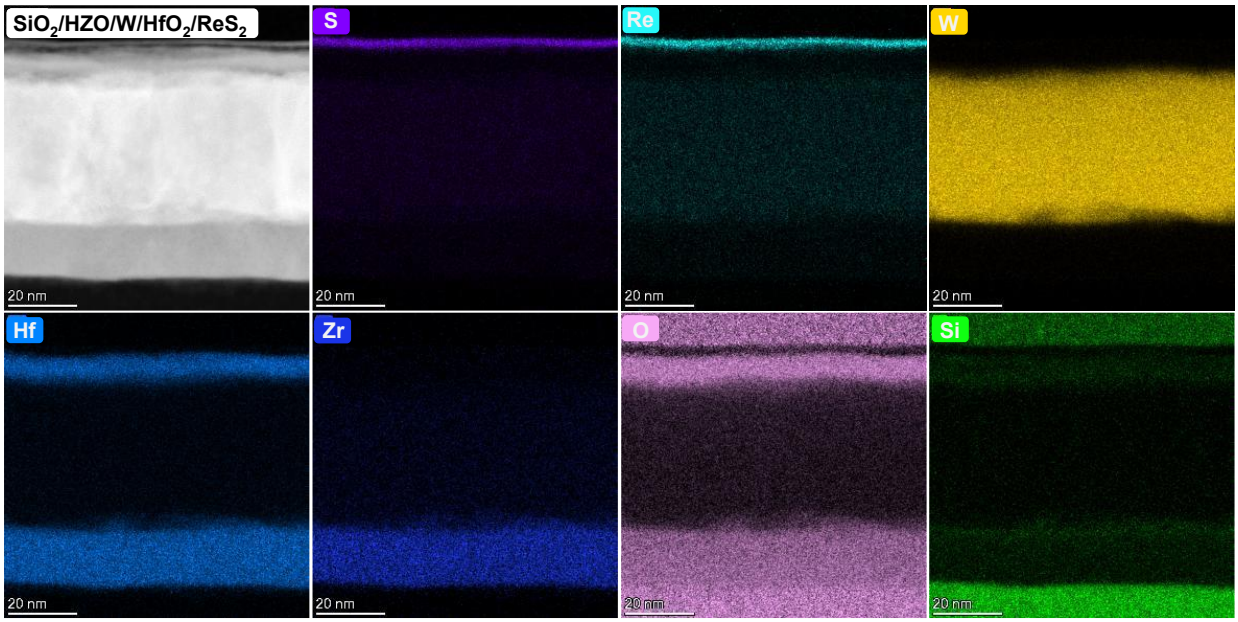


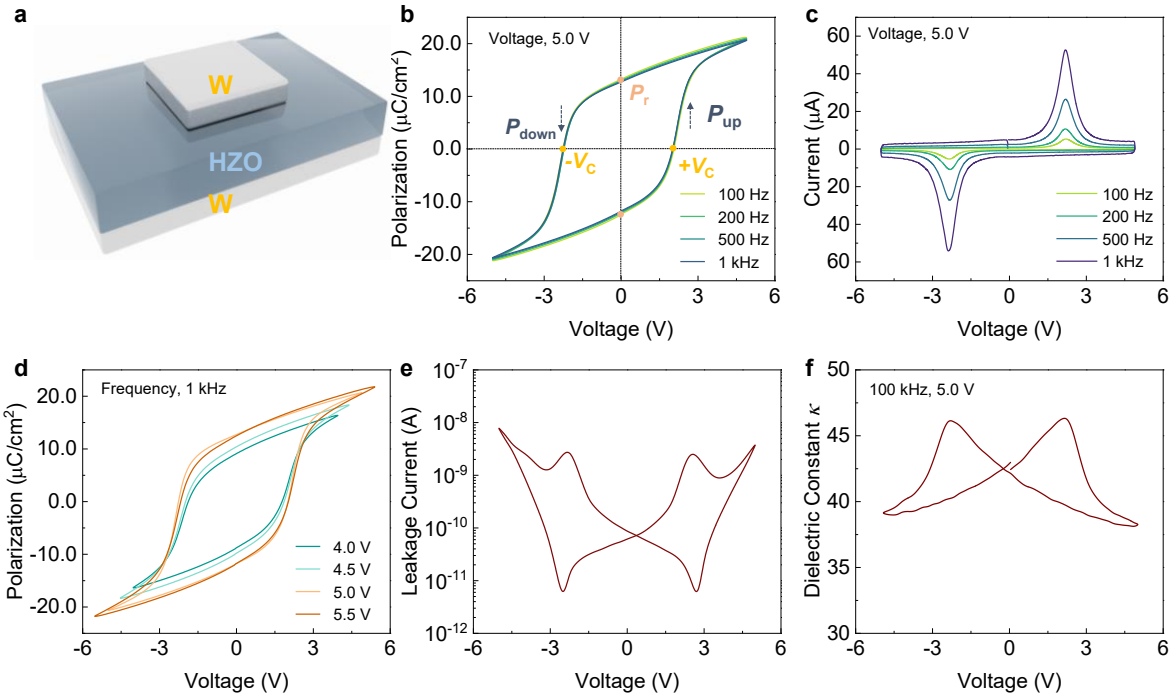
Supplementary Figure 1 | Schematic illustration of the fabrication process for the ReS_2 MFMIS FeFET. The process involves W deposition, gate electrode patterning, ALD growth of the HZO ferroelectric layer, W capping and annealing, FG formation, ALD growth of HfO_2, ReS_2 transfer, and source/drain electrode formation.



Supplementary Figure 2 | Structural characterization of the FeFET. a. The optical micrograph of the fabricated FeFET; scale bar: 5 μm. **b.** TEM image of the MFMIS FeFET structure; scale bar: 10 nm. **c.** High-resolution cross-sectional image showing ~5-layer ReS_2, and the well-defined crystalline HZO layer; scale bar: 5 nm.

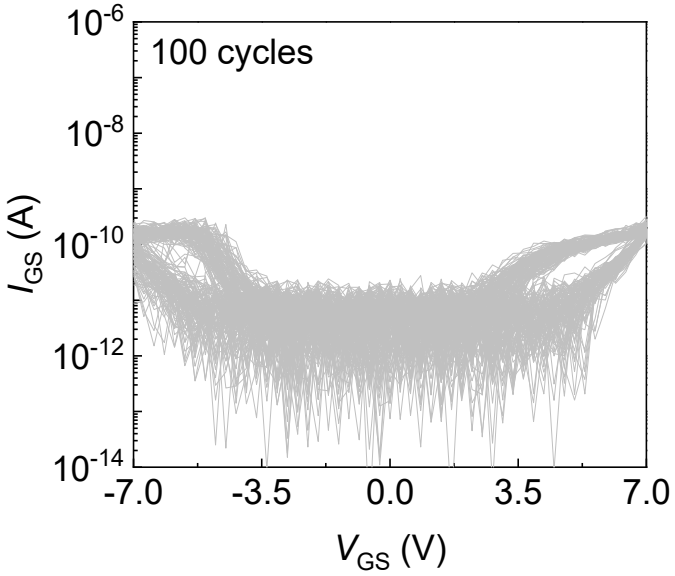


Supplementary Figure 3 | TEM cross-sectional image of the FeFET. The corresponding elemental maps obtained by energy-dispersive X-ray spectroscopy (EDS), illustrating the spatial distribution of key elements and confirming material composition and interface integrity; scale bar: 20 nm.

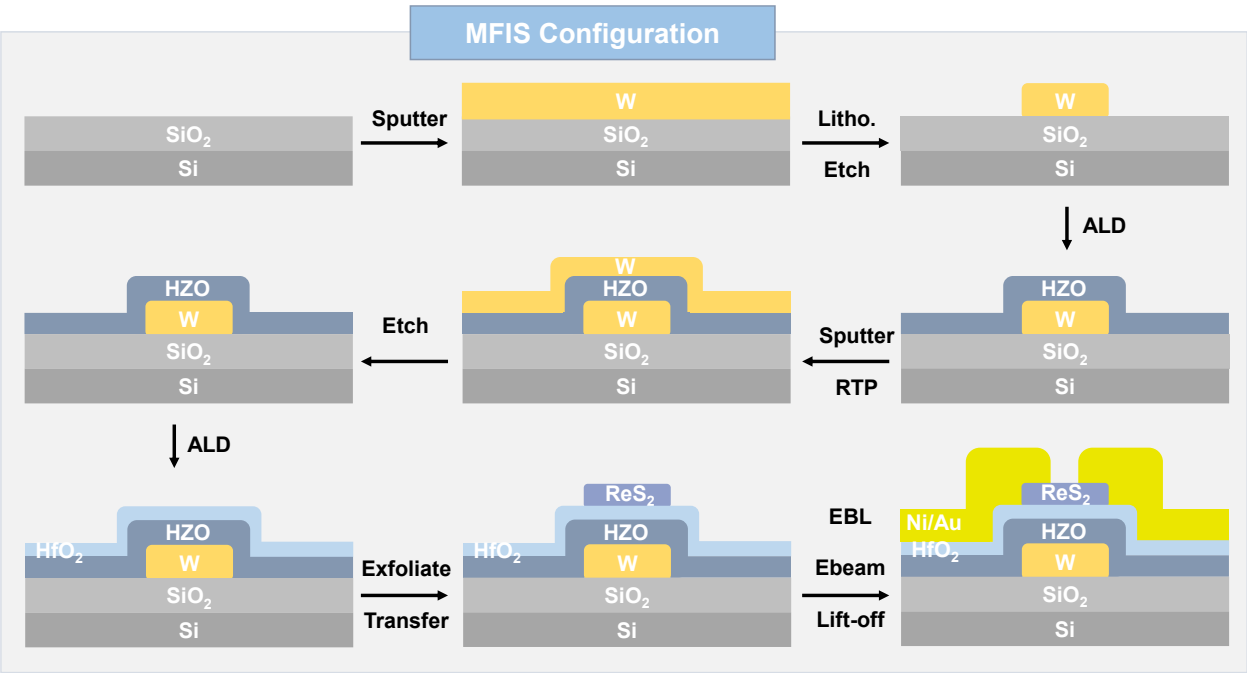


Supplementary Figure 4 | Ferroelectric properties of the HZO layer. a. Schematic of the W/HZO/W metal-ferroelectric-metal (MFM) capacitor structure used to evaluate the ferroelectric properties of the 18

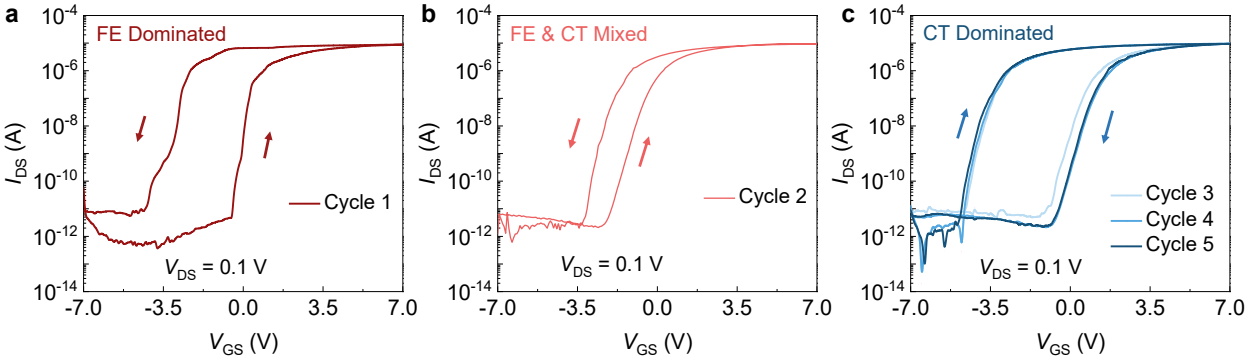
nm HZO layer. **b.** Typical *P*-*V* characteristics of the HZO layer at various frequencies under a 5.0 V applied voltage. P_r represents the remnant polarization, while $+V_C$ and $-V_C$ denote the coercive voltages. **c.** Corresponding current response associated with b. **d.** Typical *P*-*V* loops under different voltages at a frequency of 1 kHz. **e.** DC leakage current measured on an HZO-based MFM capacitor with a 100 μm × 100 μm active area. **f.** Dielectric constant (*k*) of the HZO layer.



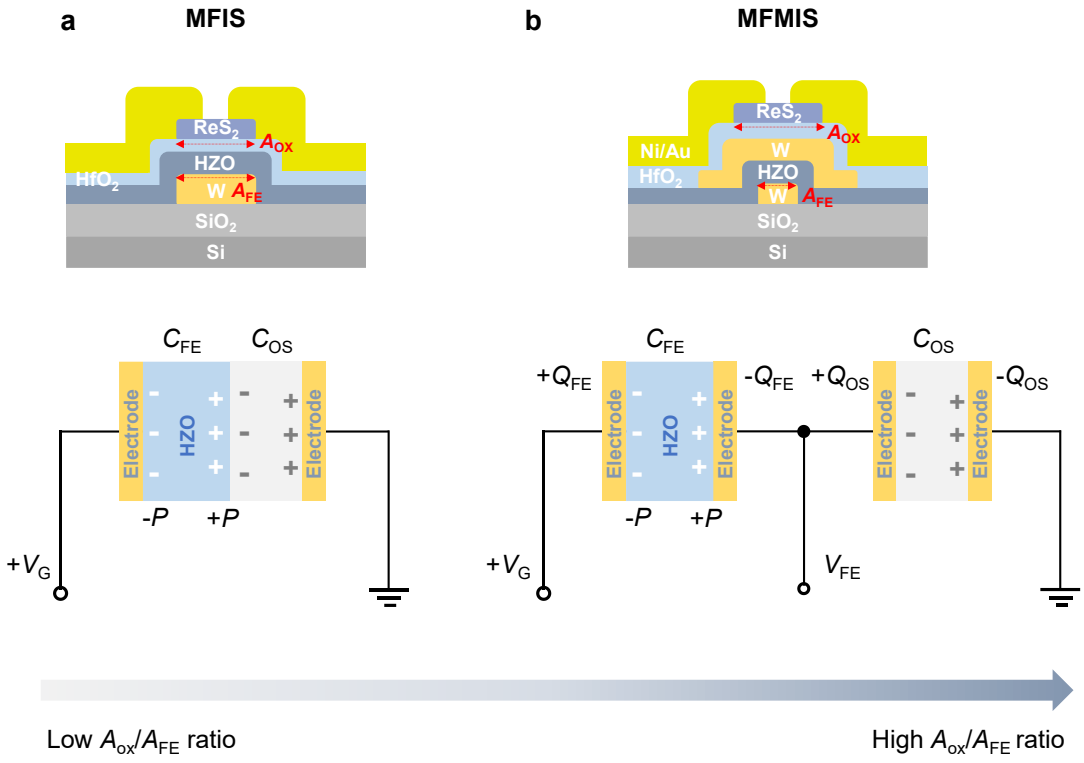
Supplementary Figure 5 | Gate leakage (I_{GS}–V_{GS}) characteristics. Measured over 100 consecutive cycles under bidirectional gate voltage sweeps from –7 V to 7 V. The consistently low leakage current confirms the excellent gate insulation and stability of the device during repeated electrical operation.



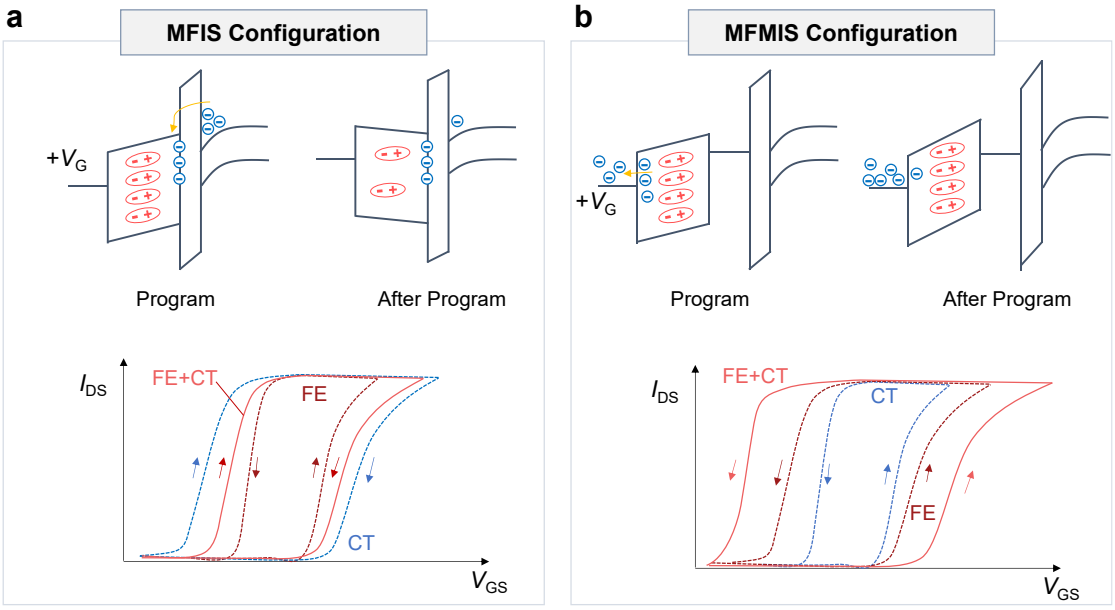
Supplementary Figure 6 | Fabrication process of the ReS_2 MFIS FeFET. The device is built by first depositing a tungsten (W) layer and patterning it into the control-gate electrode. A ferroelectric HZO layer is then deposited uniformly by atomic-layer deposition (ALD), followed by W capping and an annealing step to crystallize the HZO. The cap is subsequently removed, and a high-k HfO_2 dielectric interfacial layer is deposited via ALD. The ReS_2 channel is then transferred onto the dielectric stack, and the source/drain electrodes are formed to complete the MFIS FeFET architecture.



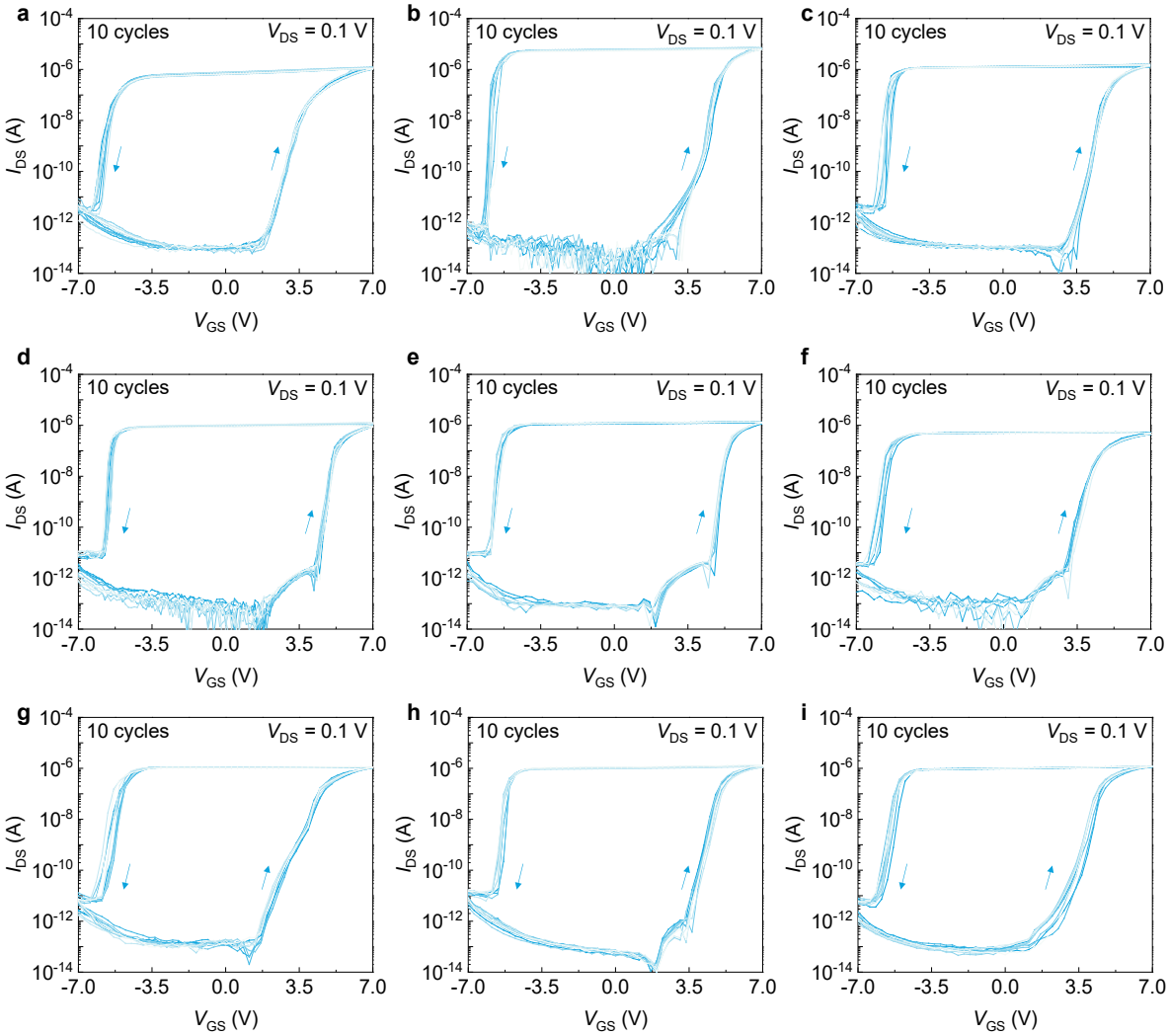
Supplementary Figure 7 | I_{DS}–V_{GS} characteristics of the ReS_2 MFIS FeFET over successive cycles. a. The device initially exhibits a ferroelectric (FE)-dominated hysteresis. **b.** It then transitions to a mixed FE and charge trapping (CT) state. **c.** Finally, it becomes CT-dominated, indicating the progressive suppression of ferroelectric switching due to competing interface charge trapping.



Supplementary Figure 8 | Voltage and charge distribution in MFIS and MFMIS FeFETs. a. Cross-sectional schematic and corresponding voltage and charge distribution of the MFIS FeFET, illustrating a fixed A_{OX}/A_{FE} ratio and incomplete charge compensation. **b.** Cross-sectional schematic and voltage/charge distribution of the MFMIS FeFET, demonstrating a tunable A_{OX}/A_{FE} ratio and enhanced charge compensation enabled by the inserted floating gate.

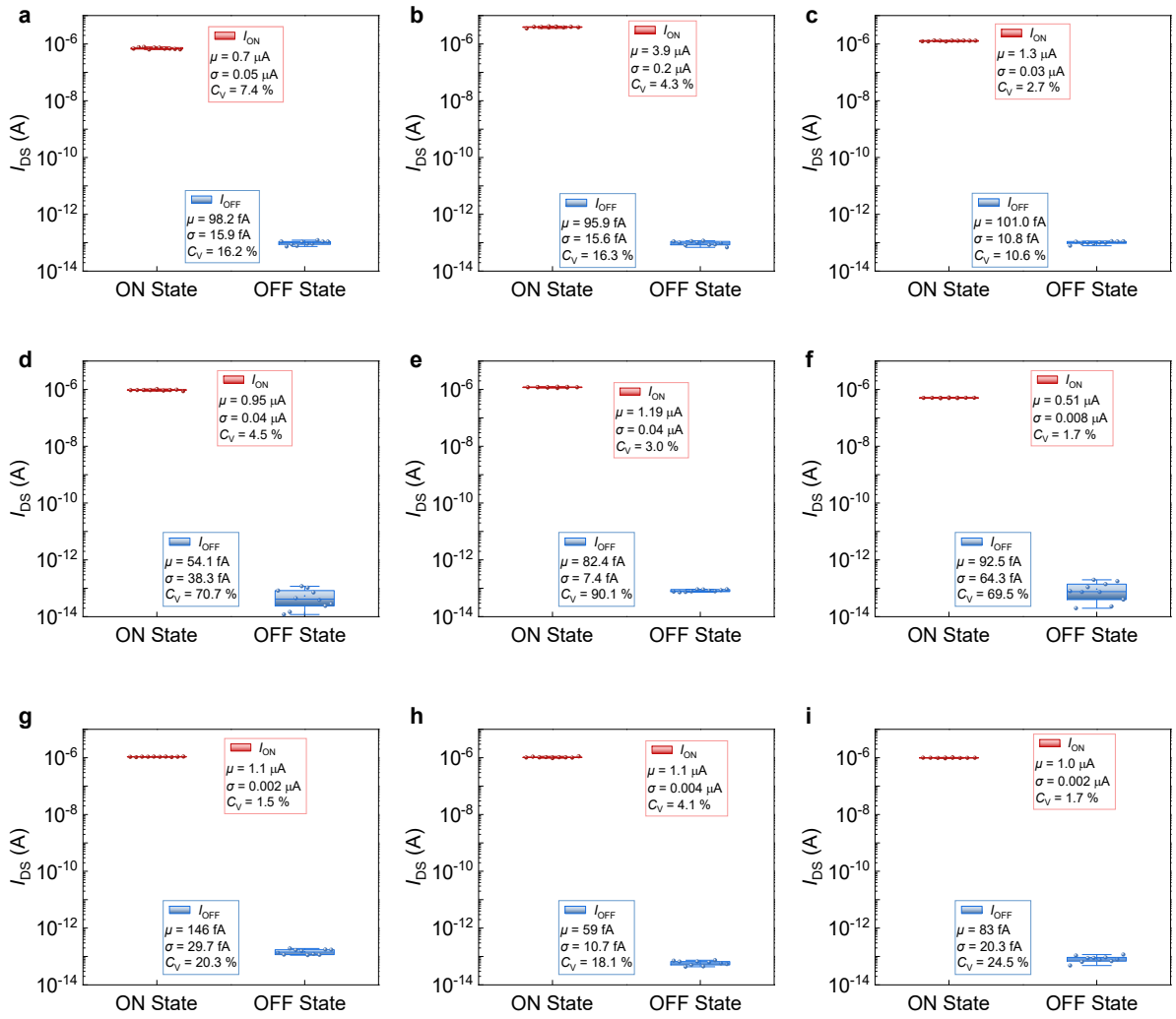


Supplementary Figure 9 | Ferroelectric–charge trapping interplay in MFIS and MFMIS structures. **a.** In the MFIS configuration, charge trapping occurs at the oxide/semiconductor interface, generating an internal electric field that opposes the ferroelectric polarization. This competition reduces the effective V_{FE} and gradually suppresses domain switching, resulting in clockwise hysteresis dominated by charge trapping (CT>FE). **b.** In the MFMIS configuration, the inserted metal layer spatially separates the ferroelectric from interface traps and shifts charge trapping to the ferroelectric/metal interface. The trapped charges align with ferroelectric dipoles, reinforcing polarization switching. This cooperative effect enhances V_{FE} and leads to a stable counterclockwise hysteresis dominated by ferroelectric switching, with CT acting as a supporting mechanism.

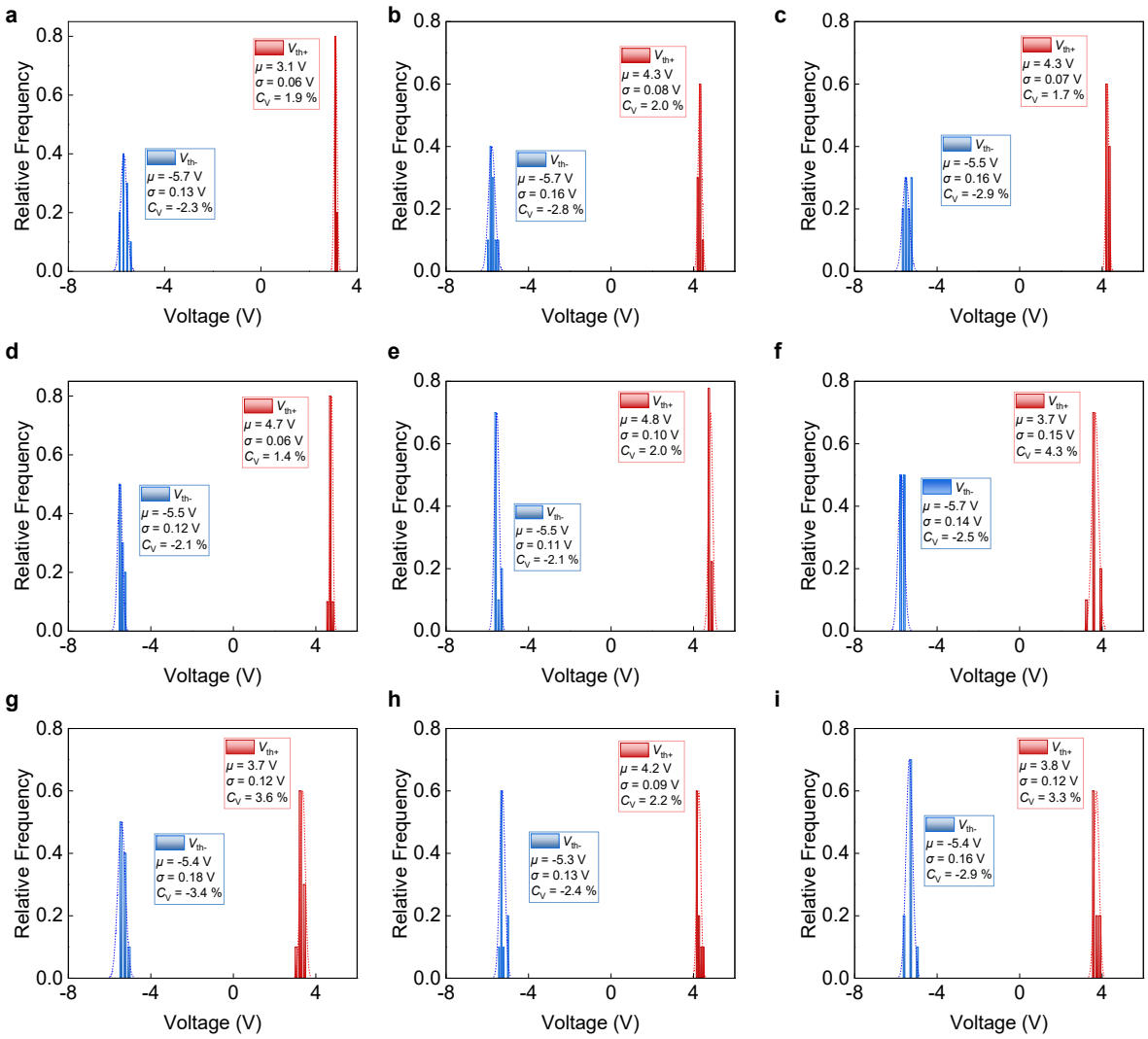


Supplementary Figure 10 | I_{DS}-V_{GS} characteristics of nine individual FeFETs. Each device (D1–D9, labeled **a**-**i**) was measured over ten consecutive cycles with V_{GS} swept from -7.0 V to 7.0 V at V_{DS}=0.1 V.

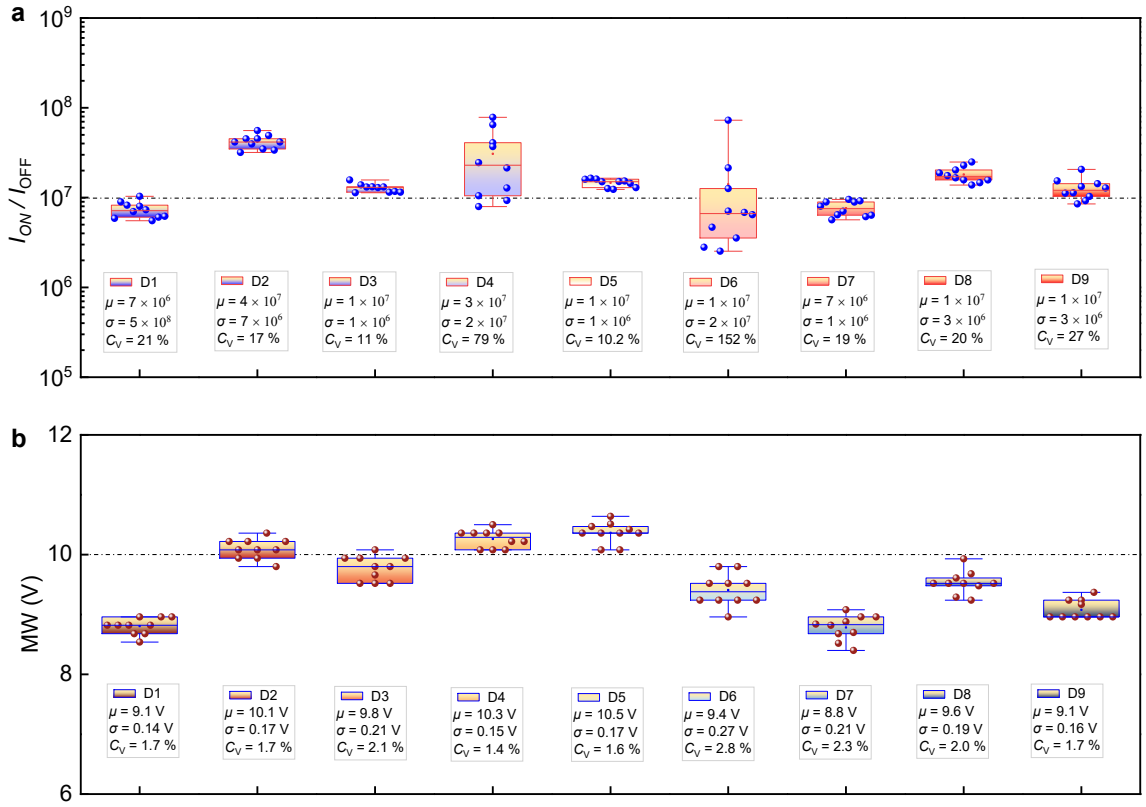
The data enable evaluation of device-to-device (D2D) and cycle-to-cycle (C2C) variations in transfer characteristics.



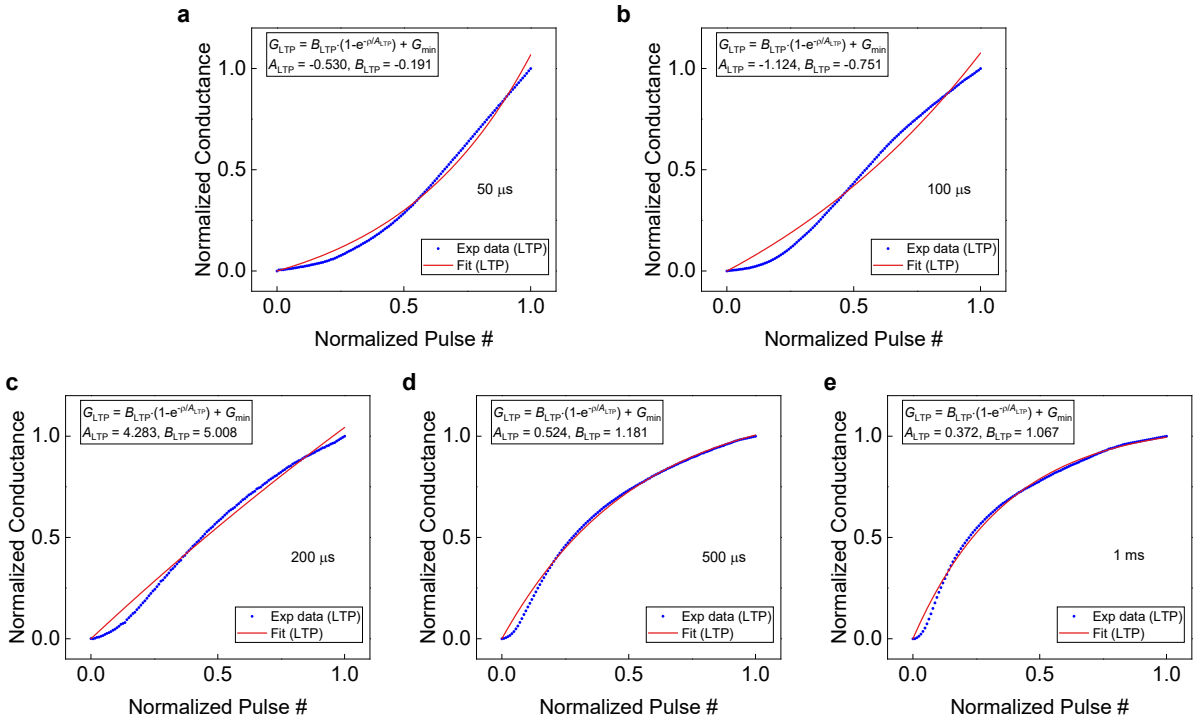
Supplementary Figure 11 | Statistical distribution of I_{ON} and I_{OFF}. These values extracted at V_{GS}=0 V over ten consecutive cycles for nine FeFET devices (D1–D9, labeled **a-i**). For each device, the average (μ), standard deviation (σ), and coefficient of variation (C_V) are calculated to quantify C2C stability and D2D variability. Box plots show the median (center line), interquartile range (box), and 1.5×IQR whiskers. All individual data points (n=10 for each group) are displayed.



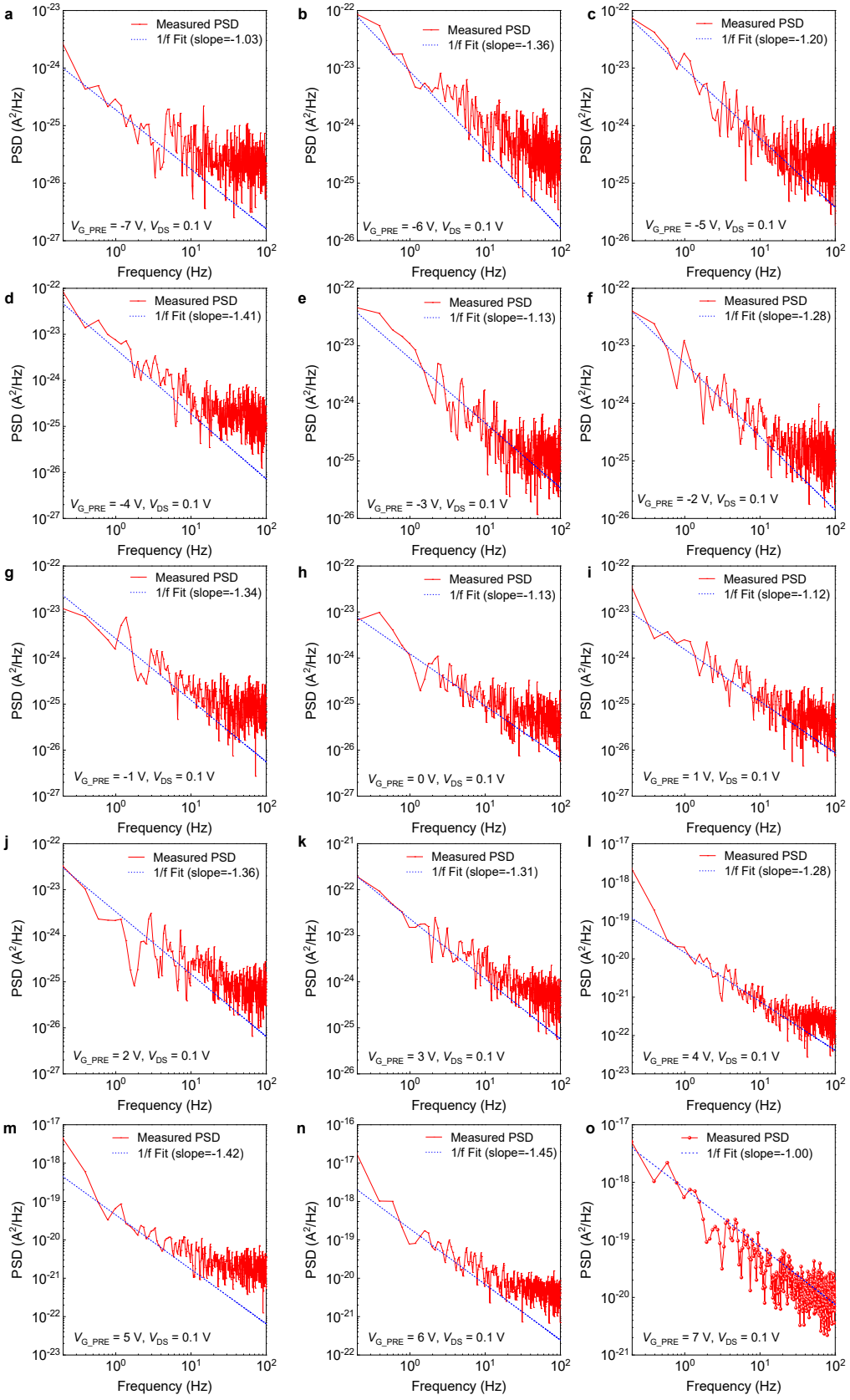
Supplementary Figure 12 | Statistical distribution of threshold voltage (V_{th}). The V_{th} were extracted at I_{DS}=1 nA over ten cycles for nine FeFET devices (D1–D9, labeled **a-i**). Mean (μ), standard deviation (σ), and coefficient of variation (C_V) are used to assess C2C and D2D variability.



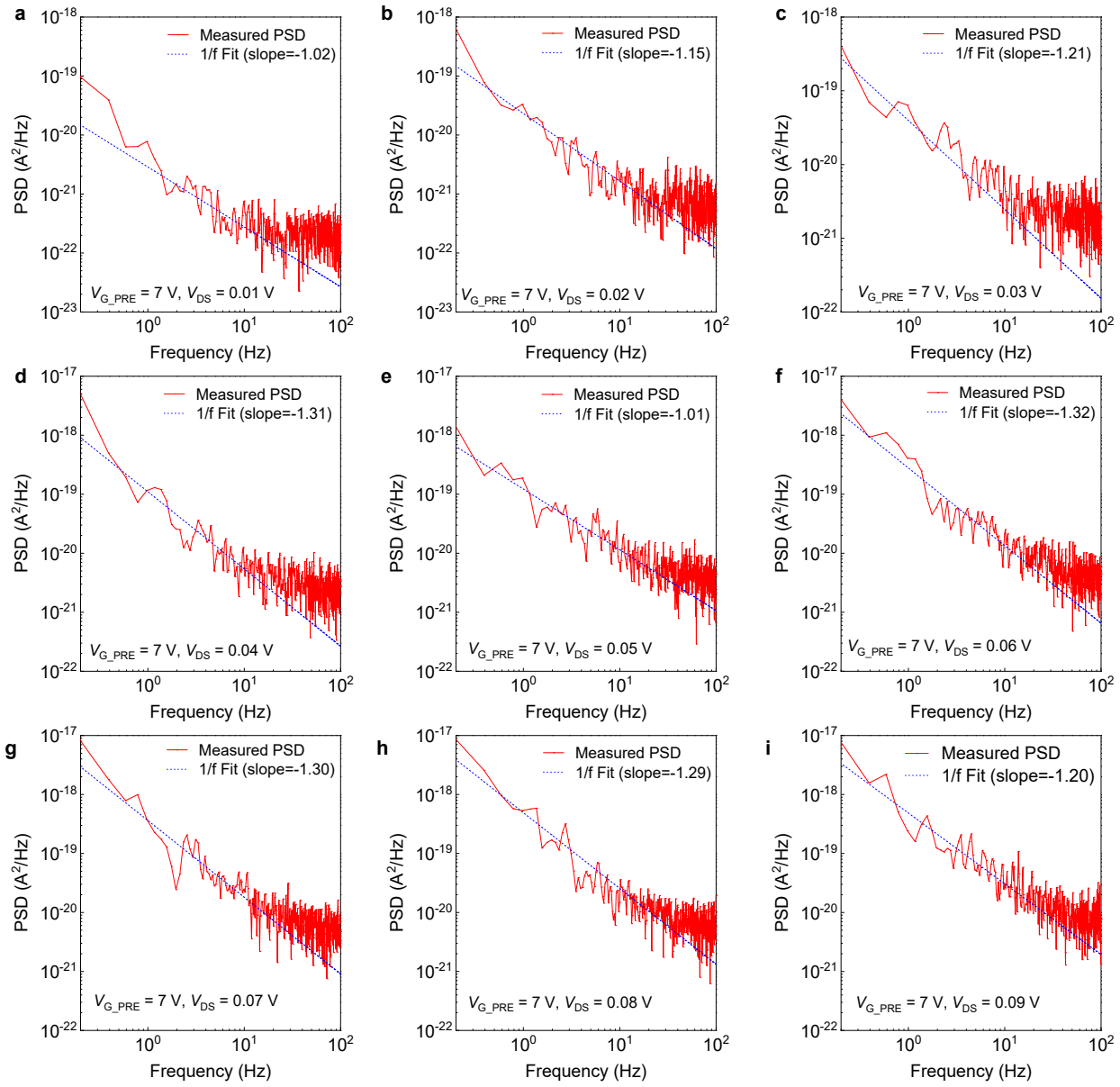
Supplementary Figure 13 | Statistical variability of I_{ON}/I_{OFF} ratio and memory window. a. Statistical distribution of I_{ON}/I_{OFF} ratio and **b.** memory window (MW) over ten cycles for nine FeFET devices (D1–D9), with mean (μ), standard deviation (σ), and coefficient of variation (C_V) reflecting both C2C and D2D variability. Box plots show the median (center line), interquartile range (box), and 1.5×IQR whiskers. All individual data points (n=10 for each group) are displayed.



Supplementary Figure 14 | Experimental and fitted results of LTP behavior. Conductance evolution is measured under gate pulses with a fixed amplitude of 5 V and varying pulse widths. **a**–**e** correspond to pulse widths of 50 µs, 100 µs, 200 µs, 500 µs, and 1 ms, respectively. The conductance evolution is fitted using the empirical model: $G_{LTP}=B_{LTP}\left(1-e^{-p/A_{LTP}}\right)+G_{min}$, where p is the pulse number, and A_{LTP}, B_{LTP}, and G_{min} are fitting parameters. The fitted curves (red) show good agreement with the experimental data (blue).

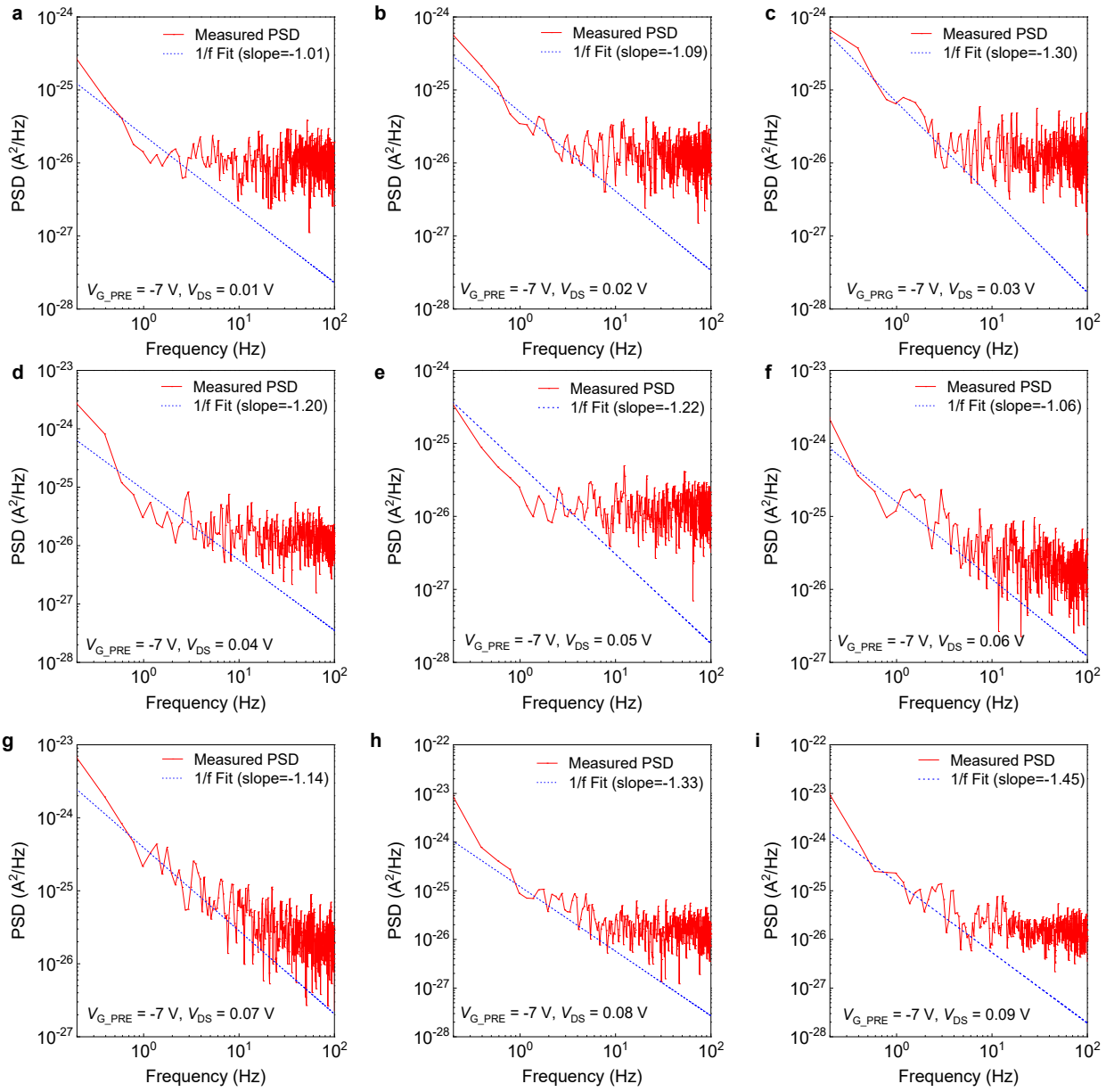

a
Measured PSD
1/f Fit (slope=-1.03)
V_{G_PRE} = -7 V, V_{DS} = 0.1 V
b
Measured PSD
1/f Fit (slope=-1.36)
V_{G_PRE} = -6 V, V_{DS} = 0.1 V
c
Measured PSD
1/f Fit (slope=-1.20)
V_{G_PRE} = -5 V, V_{DS} = 0.1 V
d
Measured PSD
1/f Fit (slope=-1.41)
V_{G_PRE} = -4 V, V_{DS} = 0.1 V
e
Measured PSD
1/f Fit (slope=-1.13)
V_{G_PRE} = -3 V, V_{DS} = 0.1 V
f
Measured PSD
1/f Fit (slope=-1.28)
V_{G_PRE} = -2 V, V_{DS} = 0.1 V
g
Measured PSD
1/f Fit (slope=-1.34)
V_{G_PRE} = -1 V, V_{DS} = 0.1 V
h
Measured PSD
1/f Fit (slope=-1.13)
V_{G_PRE} = 0 V, V_{DS} = 0.1 V
i
Measured PSD
1/f Fit (slope=-1.12)
V_{G_PRE} = 1 V, V_{DS} = 0.1 V
j
Measured PSD
1/f Fit (slope=-1.36)
V_{G_PRE} = 2 V, V_{DS} = 0.1 V
k
Measured PSD
1/f Fit (slope=-1.31)
V_{G_PRE} = 3 V, V_{DS} = 0.1 V
l
Measured PSD
1/f Fit (slope=-1.28)
V_{G_PRE} = 4 V, V_{DS} = 0.1 V
m
Measured PSD
1/f Fit (slope=-1.42)
V_{G_PRE} = 5 V, V_{DS} = 0.1 V
n
Measured PSD
1/f Fit (slope=-1.45)
V_{G_PRE} = 6 V, V_{DS} = 0.1 V
o
Measured PSD
1/f Fit (slope=-1.00)
V_{G_PRE} = 7 V, V_{DS} = 0.1 V
PSD (A^2/Hz)
Frequency (Hz)

Supplementary Figure 15 | 1/*f* noise PSD of the dark current. The PSD was measured under a fixed drain bias of V_{DS}=0.1 V after presetting the device with different gate voltages (V_{G_PRE}) ranging from -7 V to 7 V in 1 V steps. During the noise measurement, V_{GS} was held at 0 V. **a-i** correspond to different V_{G_PRE} values, showing the evolution of 1/*f* noise characteristics as a function of programming gate voltage. The PSD was calculated over a frequency range of 0.1 Hz to 100 Hz.

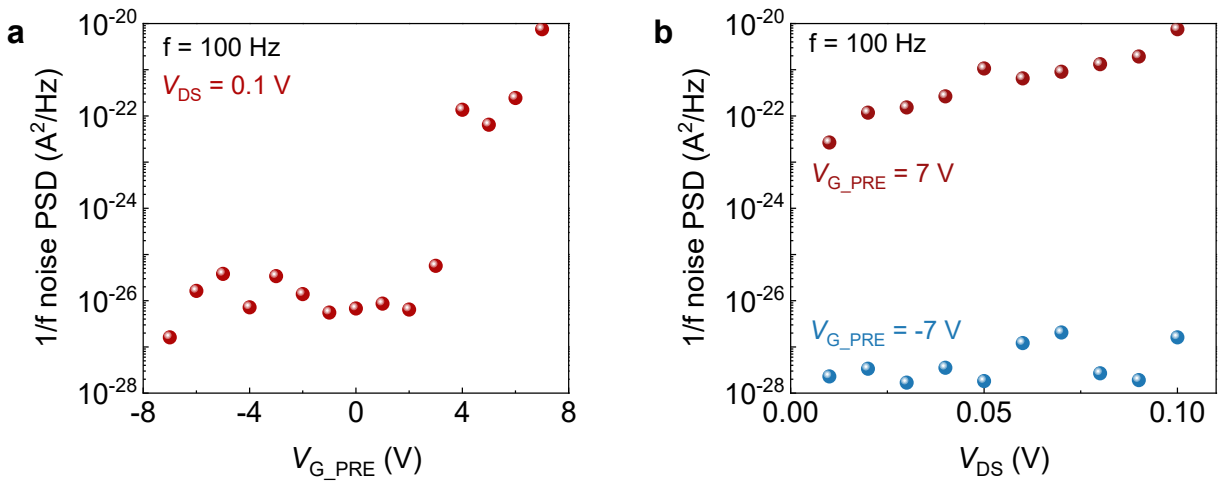


Supplementary Figure 16 | 1/*f* noise PSD in the accumulation regime. The device was first preset with V_{G_PRE}=7 V. After presetting, V_{GS} was held at 0 V while V_{DS} was swept from 0.01 V to 0.09 V in 0.01 V

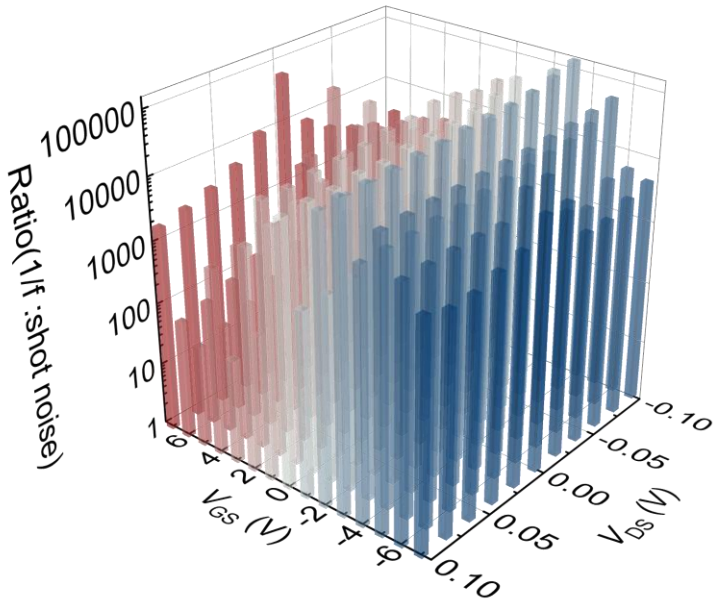
increments. **a-i** correspond to different V_{DS} values, showing the influence of drain voltage on 1/*f* noise behavior. The PSD was calculated over a frequency range of 0.1 Hz to 100 Hz.



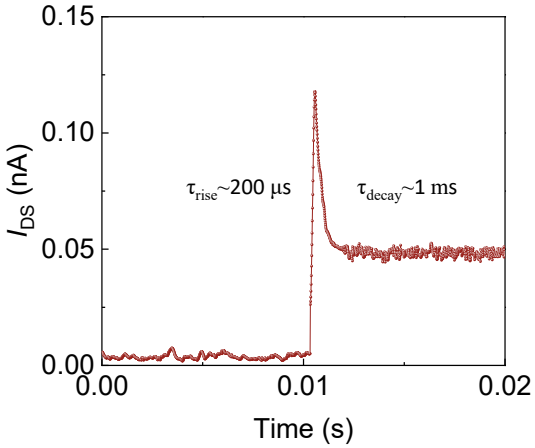
Supplementary Figure 17 | 1/*f* noise PSD in the depletion regime. The devicewas first prest with V_{G_PRE}=-7 V. After presetting, V_{GS} was held at 0 V while V_{DS} was swept from 0.01 V to 0.09 V in 0.01 V increments. **a-i** correspond to different V_{DS} values, showing the influence of drain voltage on 1/*f* noise behavior. The PSD was calculated over a frequency range of 0.1 Hz to 100 Hz.



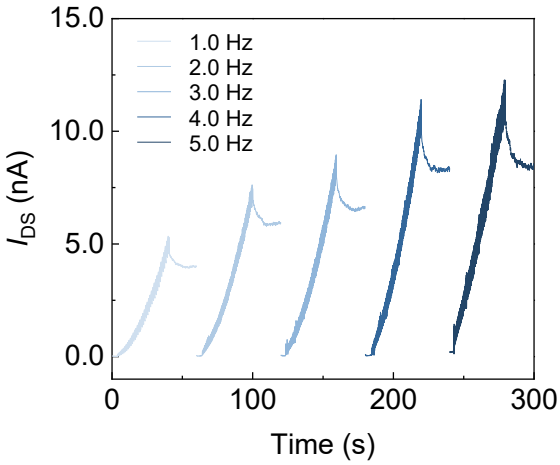
Supplementary Figure 18 | Bias-dependent 1/*f* noise characteristics. a. Drain current noise PSD at 100 Hz as a function of V_{G_PRG}, measured at a fixed drain bias of V_{DS}=0.1 V. **b.** Noise PSD versus V_{DS} under two representative gate biases: V_{G_PRE}=7 V (accumulation) and V_{G_PRE}=-7 V (depletion), highlighting the dependence of noise on channel conductance.



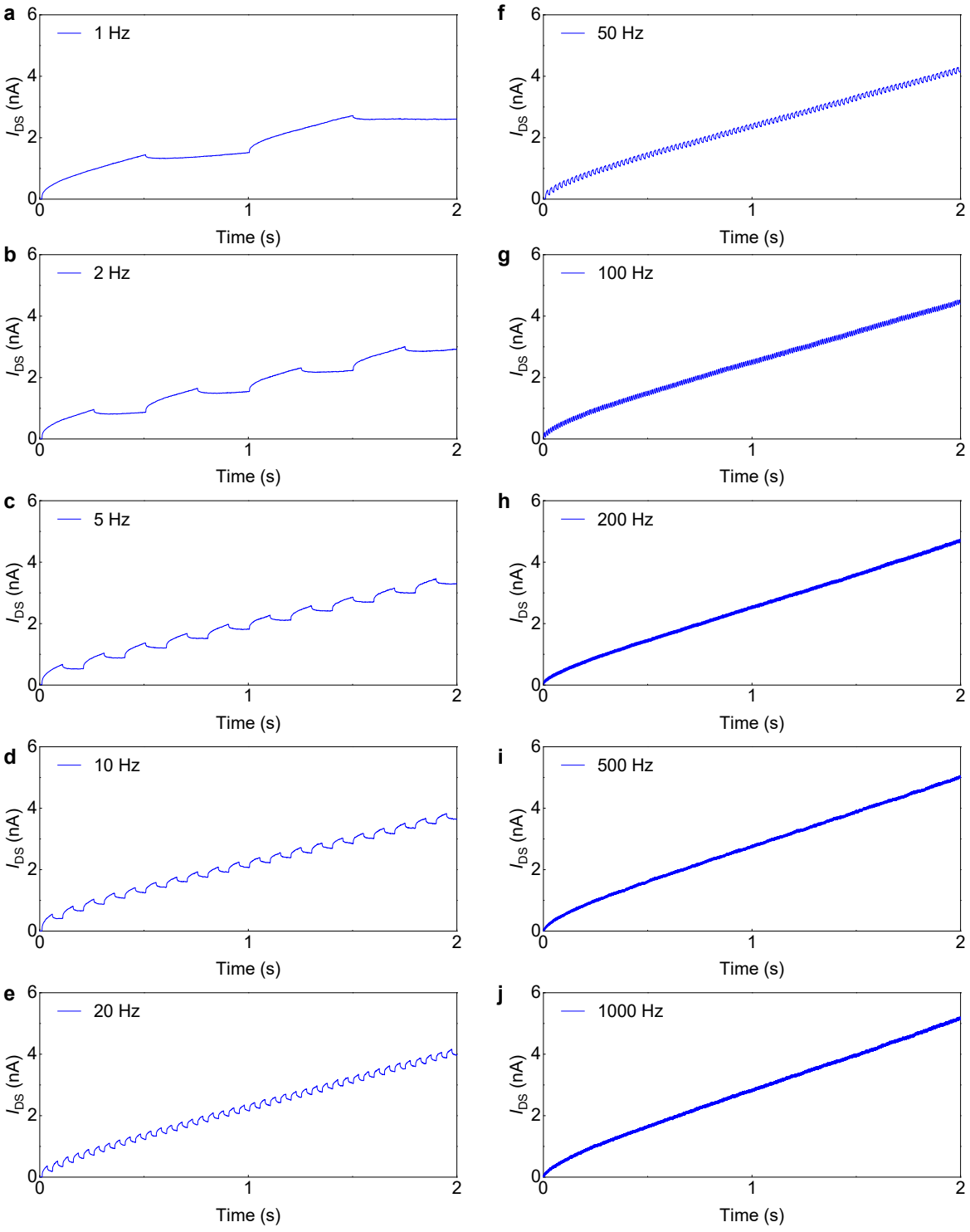
Supplementary Figure 19 | Map of the ratio of 1/*f* noise to shot noise as a function of V_{GS} and V_{DS}. This ratio quantitatively represents the relative strength of the two noise components. The consistently large values across all biasing conditions indicate that 1/*f* noise dominates the total noise behavior of the device.



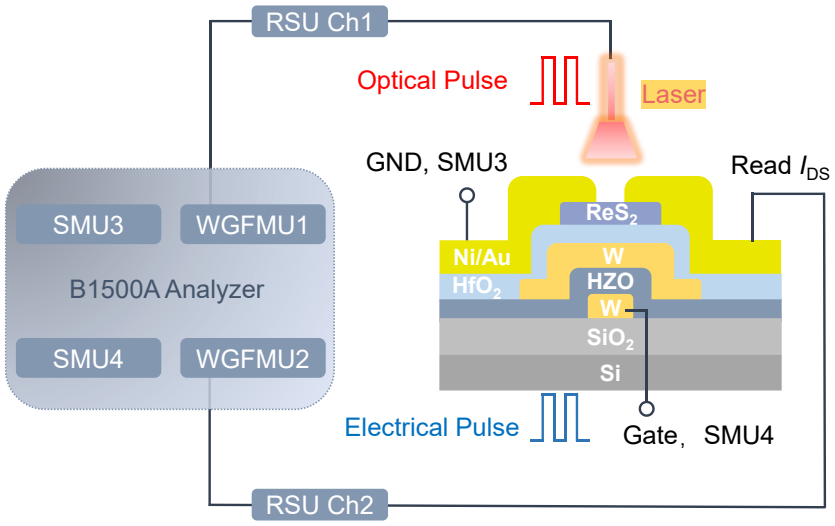
Supplementary Figure 20 | Optical response speed of the FeFET. This includes a rise time of 200 µs and a fall time of 1 ms, demonstrating its fast photoresponse characteristics.



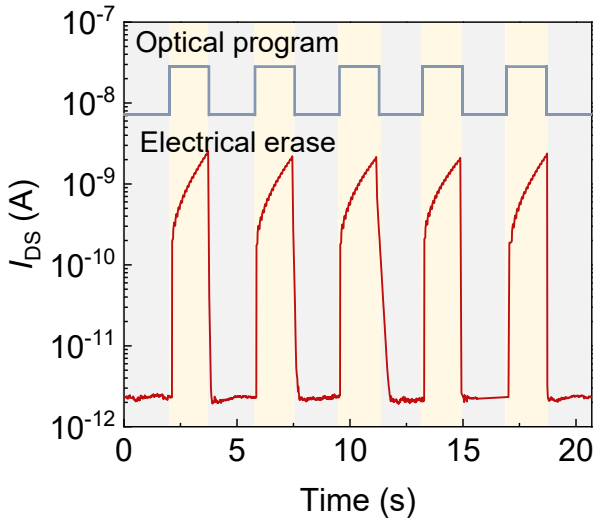
Supplementary Figure 21 | Frequency-dependent optical response of the FeFET. Photocurrent was recorded under continuous illumination with modulation frequencies ranging from 1 Hz to 5 Hz. At higher frequencies, shorter intervals between pulses reduce carrier recombination time, resulting in cumulative charge accumulation and enhanced EPSC.



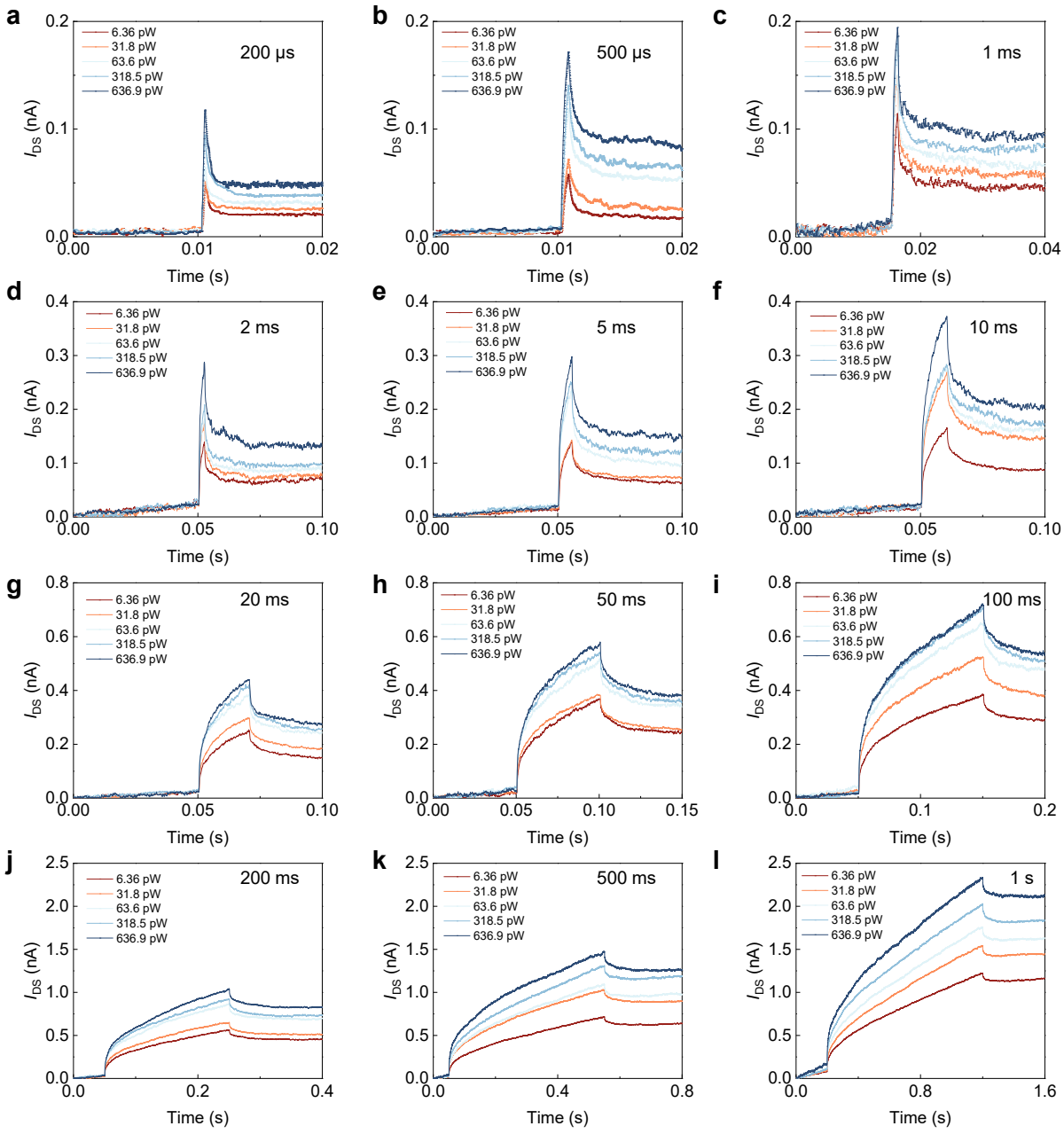
Supplementary Figure 22 | High-frequency optical response of the FeFET. a–j Photocurrent under continuous illumination with modulation frequencies from 1 Hz to 1 kHz. Higher frequencies shorten pulse intervals, enhancing temporal summation and EPSC strength, demonstrating dynamic adaptability for high-speed optical processing and neuromorphic computing.



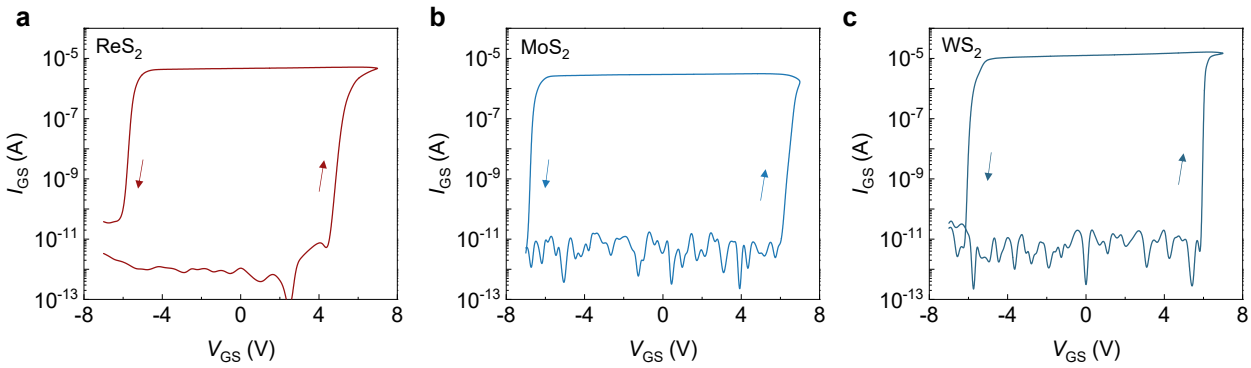
Supplementary Figure 23 | Schematic of the optoelectronic co-modulation setup. During optical programming, WGFMU1 controls the laser pulses, WGFMU2 measures the current, and SMU3 is grounded. For electrical measurements, SMU4 applies the gate voltage, WGFMU2 reads the current, and SMU3 remains grounded.



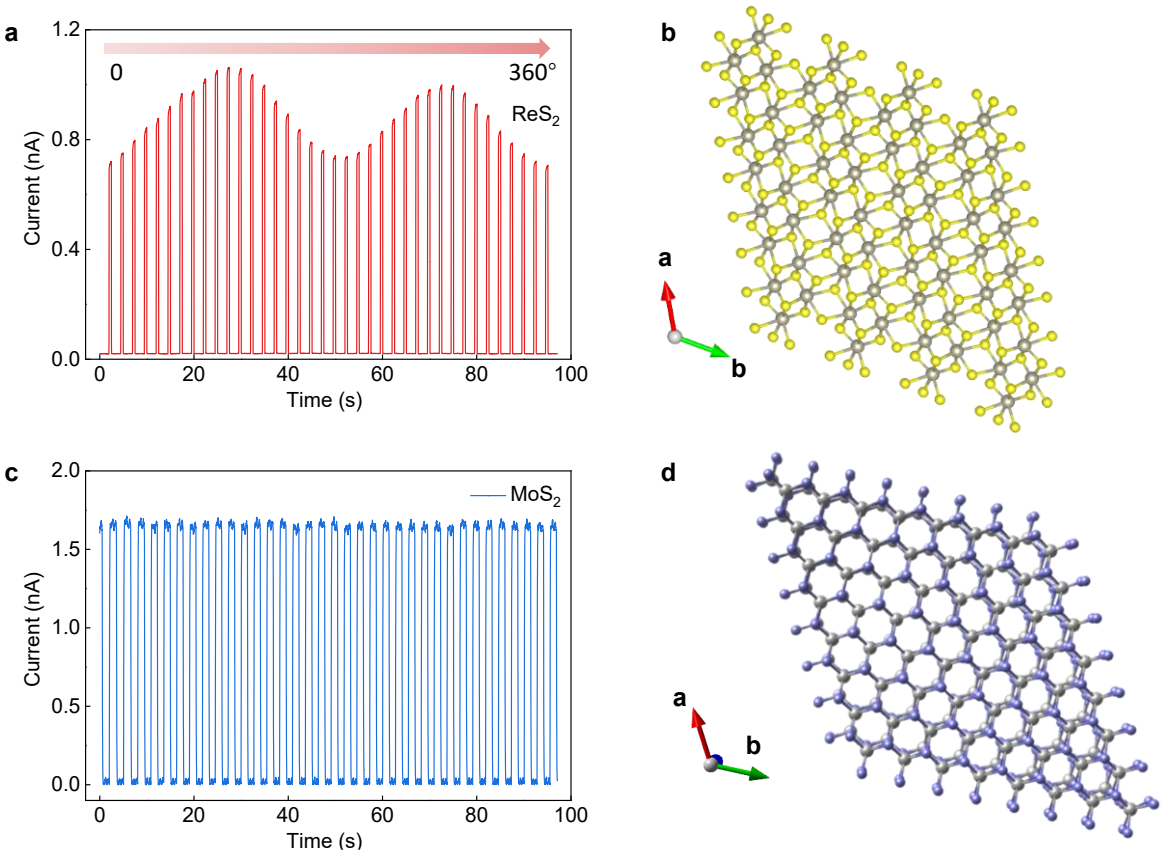
Supplementary Figure 24 | Optical programming and electrical erasing process in the FeFET. The figure demonstrates the dynamic process of optoelectronic co-modulation, wherein the device is first programmed optically, followed by electrical erasing via a gate voltage of V_{GS}=-7 V. This program–erase cycle is repeated to showcase the device's ability to achieve optoelectronic control, enabling a robust system for information writing and erasure.



Supplementary Figure 25 | Photoresponse current under varying light intensities and pulse widths. **a-l**. Optical response measured at pulse widths ranging from 200 µs to 1 s, each subplot corresponding to a specific duration. For each condition, the device was exposed to light powers of 6.36 pW, 31.8 pW, 63.69 pW, 318.45 pW, and 636.9 pW. The results reveal that both light intensity and exposure time modulate the photocurrent, enabling comprehensive evaluation of the device's photoresponse characteristics.

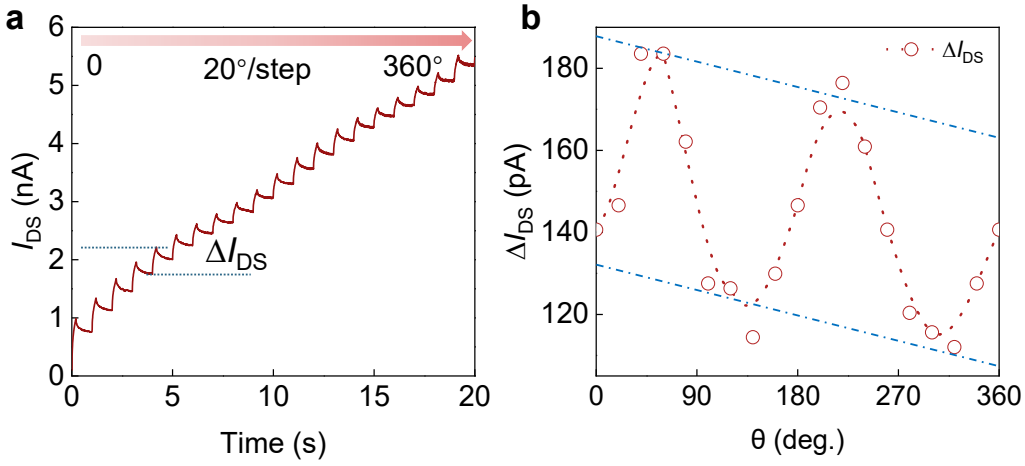


Supplementary Figure 26 | I_{DS}–V_{GS} characteristics of MFMIS FeFETs with different 2D channel materials. a. ReS_2-channel FeFET. **b.** MoS_2-channel FeFET. **c.** WS_2-channel FeFET. All devices were measured at V_{DS}=0.1 V. Each device exhibits a counterclockwise hysteresis loop, confirming reliable ferroelectric switching.

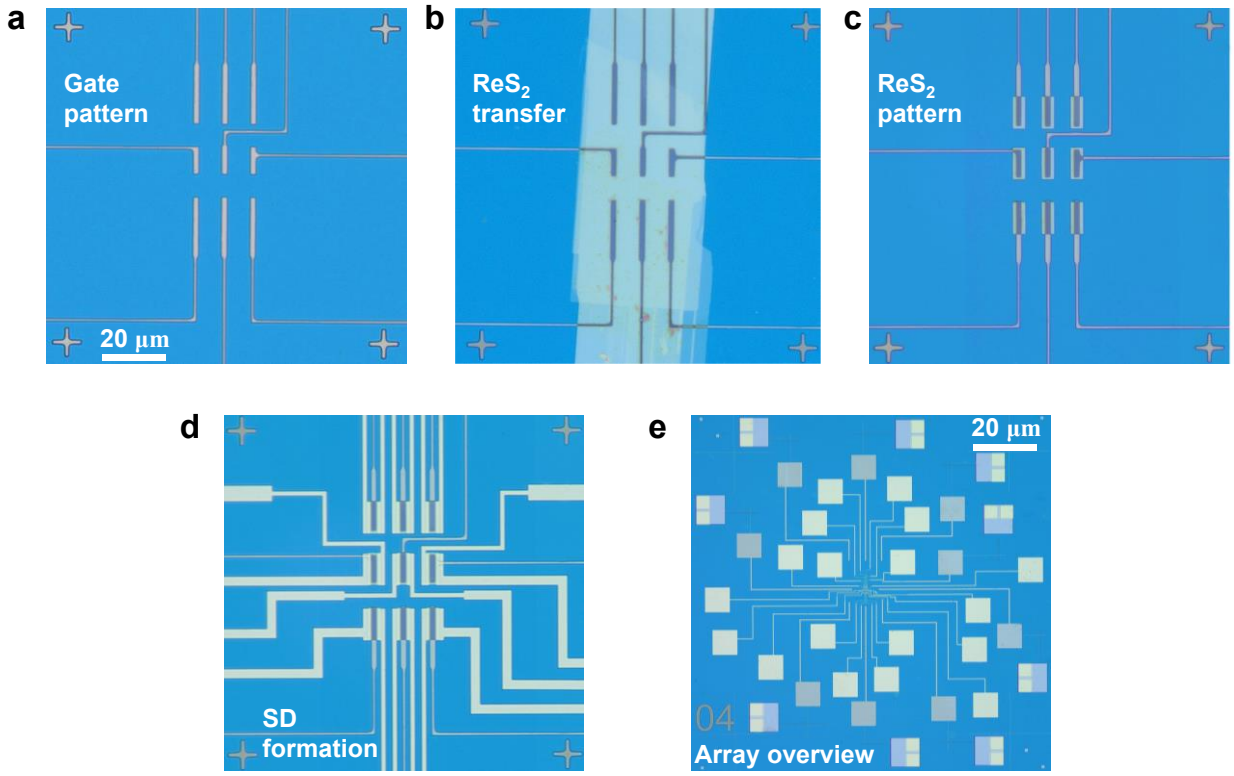


Supplementary Figure 27 | Comparison of polarization-dependent photoresponse between anisotropic ReS_2 and isotropic MoS_2. a. Polarization-resolved photocurrent of ReS_2 measured under linearly polarized light with 20° step increments, exhibiting significant oscillation with maxima along the *b*-axis and minima along the orthogonal *a*-axis, indicating strong angular dependence. **b.** Crystal structure

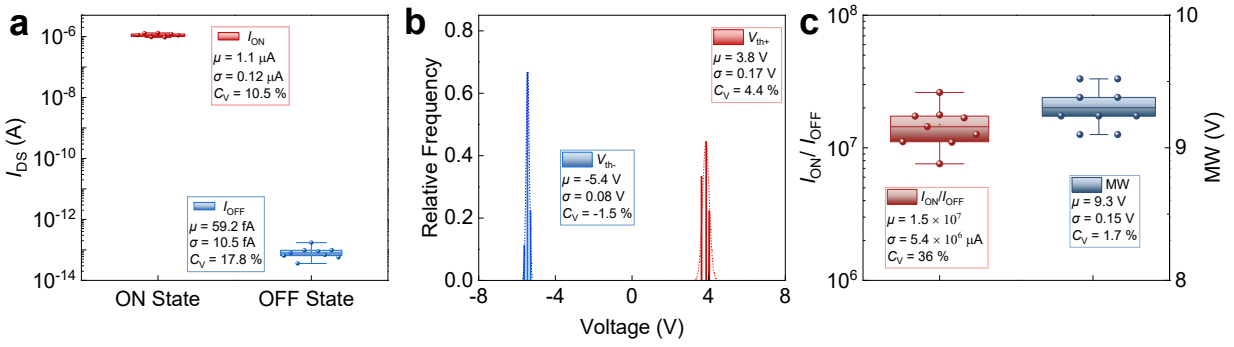
of ReS_2 with a distorted 1T' lattice and zigzag Re chains, which break in-plane symmetry and result in polarization-sensitive optical behavior. **c.** Photocurrent response of MoS_2 under identical polarization modulation conditions, exhibiting minimal angular variation, consistent with its isotropic optical response. **d.** Symmetric hexagonal lattice of MoS_2, lacking in-plane anisotropy, which accounts for its polarization-insensitive optical characteristics. These results highlight the intrinsic structural origin of angular sensitivity in ReS_2, in contrast to the isotropic behavior observed in conventional TMDCs such as MoS_2.



Supplementary Figure 28 | Polarization-dependent modulation of photocurrent in the FeFET. a. Angular-resolved measurement of photo-induced current enhancement ($\Delta I_{DS}=I_{DS2}-I_{DS1}$) as a function of incident light polarization angle, scanned from 0° to 360° in 20° steps. The observed variation reflects the anisotropic optical response of ReS_2. **b.** Polar plot of ΔI_{DS} values extracted at each polarization angle, revealing the symmetry and magnitude of photocurrent amplification with respect to crystal orientation. This anisotropic enhancement underscores the polarization-sensitive nature of the device's optoelectronic behavior.



Supplementary Figure 29 | Fabrication process of the 3×3 ReS_2 MFMIS FeFET array. a. Gate electrode patterning on the substrate. **b.** Transfer of a relatively large-area ReS_2 flake onto the predefined gate region. **c.** Lithographic definition and etching of the ReS_2 channel patterns. **d.** Formation of source/drain (S/D) electrodes to complete the device structure. **e.** Optical micrograph of the fabricated 3×3 ReS_2 FeFET array, showing the overall layout.



Supplementary Figure 30 | Statistical evaluation of the FeFET array. a. ON-state and OFF-state I_{DS} distributions, showing clearly separated current levels with low variation among devices. **b.** Distributions of the positive and negative threshold voltages (V_{th+} and V_{th-}), illustrating narrow spreads and consistent switching characteristics across the array. **c.** Summary of the I_{ON}/I_{OFF} ratios and MW, both exhibiting high

uniformity and small coefficients of variation, confirming reliable ferroelectric memory behavior for all nine devices. Box plots show the median (center line), 25th–75th percentiles (box edges), and 1.5×IQR whiskers. Individual data points (n=9) are shown.

Supplementary Table 1 | Key differences between MFIS and MFMIS FeFET architectures

Features	MFIS (without FG)	MFMIS (with FG)
A_{ox} / A_{FE}	≈ 1(fixed)	>1 (tunable)
V_{FE}	Small	Large
E_{dep}	Strong E_{dep} due to incomplete charge compensation	Suppressed by FG
Charge trapping	Oxide/channel interface Channel-side injection Opposes FE Reduces MW	FE/metal interface Gate-side injection Assist FE Enbances MW
Hysteresis loop	Clockwise (trap-dominated)	Counterclockwise (FE-dominated)

Supplementary Table 2 | Comparison of Si-based FeFETs and ReS_2-based optoelectronic synapses

Feature		Ref. 1	Ref. 2	Ref. 3	Ref. 4	**This work**
Structure		MFS FeFET	MFIS FeFET	ReS_2/h-BN/Gr	Back gate	**MFMIS FeFET**
Channel		Si	Si	ReS_2	ReS_2	**ReS_2**
Mechanism		Ferroelectric HZO	Ferroelectric HZO	Graphene FG	Charge trapping	**Hybrid ferroelectric HZO-FG**
Electrical performance	I_{OFF}	10 pA	10 nA	10 pA	1 pA	**100 fA**
	I_{ON}/I_{OFF}	10^6	10^2	10^5	10^6	**10^7**
	MW	0.8 V	4.79 V	80 V	80 V	**10.5 V**
	SR	0.3_1.5V	-2_4 V	-50_50 V	-80_80 V	**-7_7 V**
	Ratio	44%	79%	80%	50%	**75%**
Optical performance	***R***	-	-	-	-	**4×10^5 A/W**
	D*	-	-	-	-	**1.9×10^{14} Jones**
Functionality		Electrical memory	Electrical memory	Electro-optical synapse	Electro-optical synapse	**Integrated electro-optical memory & synapse**
Applications		-	-	Image recognition; optoelectronic CNN	Digit classification; optoelectronic ANN	**Optoelectronic ANN; Polarization-resolved CNN;**

Supplementary Table 3 | Optoelectronic performance of 2D ferroelectric phototransistors

Parameter	This work	Ref. 5	Ref. 6	Ref. 7	Ref. 8	Ref. 9	Ref. 10	Ref. 11	Ref. 12	Ref. 13	Ref. 14
Channel	**ReS_2**	ReS_2	MoS_2	MoS_2	$MoTe_2$	MoS_2/GeSe	InSb	MoS_2	MoS_2	MoS_2	WS_2
FE gate	**HZO**	P(VDF-TrFE)	P(VDF-TrFE)	P(VDF-TrFE)	P(VDF-TrFE)	P(VDF-TrFE)	P(VDF-TrFE)	HZO	HAO	CIPS	CIPS
Structure	**MFMIS**	MFS	MFS	MFS	MFS	MFS	MFS	MFIS	MFS	MFS	MFS
I_{ON}/I_{OFF}	**10^7**	10^7	10^5	-	10^5	-	-	-	-	10^3	-
I_{dark}	**100 fA**	1 pA	10 pA	10 pA	10 pA	1.5 pA	3 nA	-	49.15 pA	10 pA	10 pA
Voltage	**±7 V**	±40 V	±40 V	-	±30 V	±40 V	±30 V	-	±7 V	±7 V	-
MW	**12 V**	28 V	25 V	-	30 V	30 V	-	-	-	-	-
Retention	**10^4**	-	-	-	-	-	-	-	-	10^4	-
Endurance	**10^5**	-	90000	-	-	-	-	-	-	2567	-
R	**4×10^5 A/W**	11.3 A/W	2570 A/W	3260 A/W	5 A/W	0.7 A/W	311.5 A/W	96.8 A/W	12.35 A/W	321 A/W	88 A/W
D*	**1.9×10^{14} Jones**	1.7×10^{10} Jones	2.2×10^{12} Jones	9×10^{14} Jones	3×10^{12} Jones	4.7×10^{12} Jones	9.8×10^{9} Jones	4.7×10^{14} Jones	3.4×10^{13} Jones	4.6×10^{10} Jones	3.4×10^{13} Jones
wavelength	**658 nm**	visible to near-infrared	0.85 nm-1.55 μm	637 nm	520 nm	520 nm	637 nm-4.3 μm	637 nm	530 nm	405-1200 nm	405-635 nm
Response speed	**200 μs 1 ms**	-	-	480 μs 320 μs	30 μs	14 μs 400 μs	2 ms 2 ms	400 μs 200 ms	199 ms 346 ms	-	37 μs 371 μs

Supplementary Table 4 | Energy consumption of 2D materials-based ferroelectric synapses

Ferroelectric and optoelectronic synaptic material	Synapse operation mode	Energy consumption	Ref.
CIPS/WSe_2	Electrical and optical co-stimulation	20 pJ	Ref. 15
PZT/WS_2	Electrical and optical co-stimulation	2.2 pJ	Ref. 16
Al_2O_3/In_2Se_3	Electrical and optical co-stimulation	1 pJ	Ref. 17
SiO_2/CIPS	Electrical and optical co-stimulation	0.36 pJ	Ref. 18
P(VDF-TrFE)/ReS_2	Electrical and optical co-stimulation	66.7 fJ	Ref. 19
P(VDF-TrFE)/WSe_2	Electrical stimulation only	4 pJ	Ref. 20
h-BN/ In_2Se_3	Electrical stimulation only	234 fJ	Ref. 21
P(VDF-TrFE)/MoS_2	Electrical stimulation only	1 fJ	Ref. 22
HZO/ReS_2	**Electrical and optical co-stimulation**	**2 fJ**	**This work**

Supplementary Note 1 | Fabrication of the ReS_2 MFMIS FeFET

The ReS_2 FeFET was fabricated on SiO_2/p-type Si (100) substrates following a multistep process (**Supplementary Figure 1)**. A 30 nm tungsten (W) back gate was defined by sputtering and patterning. An 18 nm HZO ferroelectric film was deposited by atomic layer deposition (ALD) at 280°C, followed by a 40 nm W top electrode. After rapid thermal annealing (400°C, 60 s, N_2) to crystallize the HZO and activate its ferroelectric phase, completing the metal–ferroelectric–metal (MFM) capacitor structure for ferroelectric verification, the W layer was patterned into an FG. An 8 nm HfO_2 layer was deposited by ALD at 150°C. Few-layer ReS_2 flakes were mechanically exfoliated and transferred onto the HfO_2 surface inside a glovebox to prevent oxidation. Finally, source and drain electrodes were defined by electron beam lithography and deposited with a 30/20 nm Ni/Au bilayer, completing the MFMIS FeFET fabrication. An optical micrograph of the fabricated device is shown in **Supplementary Figure 2a**. The device consists of a few-layer ReS_2 with Ni/Au contacts, covering an area of approximately 100 μm^2. Cross-sectional transmission electron microscopy (TEM) imaging (**Supplementary Figure 2b**) reveals the MFMIS stack with a ~3.5 nm ReS_2 channel. High-resolution TEM (HR-TEM) image (**Supplementary Figure 2c)** confirms five atomic layers of ReS_2 and well-crystallized HZO. Energy-dispersive X-ray spectroscopy (EDS) mapping (**Supplementary Figure 3**) further demonstrates uniform elemental distribution and clean interfaces, verifying successful integration of all components.

Supplementary Note 2 | Comparative analysis of MFIS and MFMIS FeFET switching mechanisms

To comprehensively understand the underlying mechanisms responsible for the enlarged memory window observed in MFMIS FeFETs, we conducted a comparative study using MFIS- and MFMIS-structure FeFETs that were fabricated via similar process flows. Specifically, MFIS FeFETs were fabricated identically to MFMIS devices but without the floating gate layer (**Supplementary Figure 6**), ensuring comparable material stacks and fabrication conditions. The MFIS FeFET exhibits unstable switching behavior across programming cycles. As demonstrated in **Supplementary Figure 7**, the device initially exhibits ferroelectric (FE)-dominated hysteresis (**Supplementary Figure 7a**), then gradually transitions to a mixed FE and charge trapping (CT) state (**Supplementary Figure 7b**), and ultimately becomes dominated by CT (**Supplementary Figure 7c**). This evolution underscores a competitive interaction between ferroelectric polarization and interface-induced charge trapping, which progressively degrades the ferroelectric response. This progressive degradation motivates a deeper investigation into the voltage distribution across the ferroelectric layer, the influence of depolarization fields, and interfacial charge trapping mechanisms in both MFIS and MFMIS architectures, as detailed in the following sections.

a) Voltage distribution across the ferroelectric layer

In both MFIS and MFMIS FeFETs, the applied gate voltage V_G is distributed across the ferroelectric layer, gate dielectric, and semiconductor channel, and can be expressed as:

$$V_G=V_{FE}+V_{OX}+V_{FB}+\varphi_S \quad (1)$$

Here, V_{FE} is the voltage across the ferroelectric layer, V_{OX} is the voltage across the overall oxide/semiconductor stack, V_{FB} is the flat-band voltage, and φ_S is the surface potential of the semiconductor. The gate stack can be modeled as a series connection of the ferroelectric capacitance C_{FE} and the capacitance of the insulating layer and semiconductor (C_{OS}). In this framework, the effective voltage across the ferroelectric is given by:

$$V_{FE}=\frac{C_{OS}}{C_{OS}+C_{FE}}V_G-\frac{P_r}{C_{OS}+C_{FE}} \quad (2)$$

The first term reflects capacitive voltage division, while the second term accounts for the voltage contribution from the remanent polarization (P_r) of the ferroelectric layer.

To include geometric effects, the total capacitance of each layer is scaled by its physical area. The voltage drop across the ferroelectric can then be expressed as:

$$V_{FE}=\frac{C_{OS}A_{OX}}{C_{OS}A_{OX}+C_{FE}A_{FE}}V_{OX}=\frac{\frac{C_{OS}A_{OX}}{C_{FE}A_{FE}}}{1+\frac{C_{OS}A_{OX}}{C_{FE}A_{FE}}}V_{OX} \quad (3)$$

Where A_{OX} and A_{FE} are the physical areas of the insulating/channel and ferroelectric layers, respectively. This expression indicates that V_{FE} is influenced by both the capacitance values and area ratios of the dielectric layers.

In conventional MFIS structures, where $A_{OX}\approx A_{FE}$ and $C_{FE}\gg C_{OS}$, the ratio $\frac{C_{OS}A_{OX}}{C_{FE}A_{FE}}\ll 1$, resulting in a minimal voltage drop across the ferroelectric layer. Consequently, polarization switching is incomplete, and the device exhibits narrow hysteresis loops and reduced memory performance (**Supplementary Figure 8a**).

In contrast, the MFMIS structure introduces a floating gate between the ferroelectric and the underlying oxide/channel stack. This design electrically decouples the two regions and allows geometric tuning of A_{FE} and A_{OX}. By setting $A_{OX}>A_{FE}$, the voltage division ratio improves, allowing a larger fraction of the gate voltage to be applied across the ferroelectric. Furthermore, the floating gate functions as an equipotential surface that suppresses capacitive cross-talk, ensuring that the ferroelectric layer receives sufficient bias to achieve complete polarization reversal (**Supplementary Figure 8b**). These enhancements enable broader memory windows and more robust nonvolatile performance.

b) The influence of depolarization fields

When the gate bias is removed (i.e., during the retention phase, V_G=0), the FeFET stack must satisfy electrostatic equilibrium and charge neutrality. Under this condition:

$$V_G=V_{FE}+V_{OX}=\frac{Q_{FE}-P_r}{C_{FE}}+\frac{Q_{OS}}{C_{OS}}=0 \tag{4}$$

Solving this yields the charge stored on the ferroelectric interface:

$$Q_{FE}=\frac{P_r C_{OS}}{C_{OS}+C_{FE}} \tag{5}$$

Since this charge does not fully compensate the remanent polarization P_r ($Q_{FE}\neq P_r$), a depolarization field (E_{dep}) is induced within the ferroelectric layer:

$$E_{dep}=\frac{P_r}{\varepsilon_{FE}(\frac{C_{OS}}{C_{FE}}+1)} \tag{6}$$

This internal field opposes the remanent polarization and promotes gradual destabilization of the ferroelectric state. Over time, the depolarization field causes a shrinkage in the hysteresis window and degrades retention performance, particularly in scaled devices.

In MFIS structures, the large ferroelectric-to-oxide capacitance ratio ($C_{FE}\gg C_{OS}$) combined with a fixed area ratio ($A_{OX}\approx A_{FE}$) results in inefficient compensation of the remanent polarization after gate bias removal. This imbalance generates a strong E_{dep}, which counteracts the polarization and leads to gradual hysteresis degradation and retention loss.

By contrast, the MFMIS structure introduces a floating gate that effectively compensates the polarization-induced bound charges and spatially separates the ferroelectric layer from defect-prone oxide or interface regions. This configuration significantly suppresses E_{dep}, thereby stabilizing the polarization state and improving both retention and endurance.

c) Interfacial charge trapping mechanisms

Charge trapping mechanisms differ fundamentally between MFIS and MFMIS structures.

In MFIS FeFETs, trapped charges accumulate at the oxide/semiconductor interface, typically due to carrier injection from the channel. These charges generate an internal electric field that opposes the ferroelectric polarization, resulting in a competitive interaction. Over successive cycles, this antagonism leads to the suppression of ferroelectric switching, manifesting as a clockwise, charge-trapping-dominated (CT-dominated) hysteresis. This behavior is often accompanied by a reduced memory window and poor endurance.

In MFMIS FeFETs, charge trapping primarily occurs at the ferroelectric/metal interface due to gate-side injection. The trapped charges possess the same polarity as the bound ferroelectric dipoles, resulting in a cooperative interaction that reinforces the spontaneous polarization. This effect enhances both P_r and

V_{FE}, leading to a strengthened counterclockwise hysteresis. In this case, charge trapping acts as an assistive mechanism that stabilizes ferroelectric domains and improves long-term retention. This favorable interfacial behavior explains the superior endurance and wider memory window observed in MFMIS devices (see **Supplementary Figure 9** for a visual comparison).

Supplementary Note 3 | Cycle-to-cycle and device-to-device reliability of the MFMIS FeFETs

To assess the electrical reliability and statistical uniformity of the MFMIS FeFETs, we systematically investigated both cycle-to-cycle (C2C) and device-to-device (D2D) variations. I_{DS}-V_{GS} characteristics of nine devices (D1 to D9) were measured over ten consecutive cycles under identical test conditions (**Supplementary Figure 10**). All devices consistently exhibited stable and repeatable counterclockwise hysteresis, indicating robust ferroelectric switching and reliable memory behavior.

To quantitatively evaluate performance variation, we extracted key parameters including on-state current (I_{ON}), off-state current (I_{OFF}), positive and negative threshold voltages (V_{th+} and V_{th-}), the I_{ON}/I_{OFF} ratio, and memory window (MW) for each cycle and each device. The statistical results are summarized in **Supplementary Figure 11–13**. For each parameter, the mean (μ), standard deviation (σ), and coefficient of variation ($C_V=\sigma/\mu$) were calculated. All key parameters, including I_{ON}, I_{OFF}, V_{th}, I_{ON}/I_{OFF}, and MW, exhibit relatively small coefficients of variation, indicating consistent performance across cycles and among different devices. As shown in **Supplementary Figure 13**, the I_{ON}/I_{OFF} ratio reaches ~10^7 and the MW is approximately 10 V, further confirming the devices' strong switching contrast and nonvolatile performance.

These results confirm that the MFMIS FeFETs maintain highly uniform electrical switching characteristics with minimal drift or degradation, even under repeated cycling. Such electrical stability ensures consistent performance in the dark state and provides a reliable baseline for evaluating light-induced modulation, reinforcing the credibility of the observed optoelectronic memory and synaptic functionalities.

Supplementary Note 4 | Dominant noise mechanism analysis

The accurate evaluation of specific detectivity (D^*) in photodetectors critically depends on a thorough understanding of the underlying noise mechanisms. Since D^* is defined as a function of responsivity normalized by the total noise current density, neglecting or misidentifying the dominant noise sources may lead to substantial overestimation or underestimation of device performance. The total noise typically arises from three main contributions: shot noise, thermal noise, and 1/f (flicker) noise. Below, we present a detailed analysis of each noise component and its combined impact on the calculation of D^*.

Shot noise arises due to the discrete nature of charge carriers and follows Poisson statistics. It is primarily governed by the dark current (I_{DS}), and its noise current spectral density is given by:

$$\mathrm{PSD_{shot}}=\sqrt{2qI_{DS}} \tag{7}$$

where I_{DS} is the dark current is the drain current in the dark condition, and q is the electron charge. Shot noise is more pronounced at low illumination levels and high frequencies.

Thermal noise results from the random thermal motion of charge carriers within a conductor. In photodetectors, it is influenced by the channel resistance (R_{ch}) and temperature. The PSD for thermal noise is expressed as:

$$\mathrm{PSD_{thermal}}=\sqrt{\frac{4k_BT}{R_{ch}}} \tag{8}$$

where k_B is the Boltzmann constant (1.381×10^{-23} J/K), T is the ambient temperature (293 K), and R_{ch} corresponds to channel resistance ($R_{ch}=V_{DS}/I_{DS}$). Thermal noise is more prominent at higher temperatures and lower resistances.

1/f noise, or flicker noise, is characterized by a power spectral density that is inversely proportional to frequency ($1/f_{\alpha}$, with α typically between 0.8 and 1.2). It originates from low-frequency fluctuations in charge carrier density or mobility. This noise dominates at low frequencies (typically below 100 Hz–100 kHz, depending on the device) and is highly dependent on the device's material properties and operating conditions.

$$\mathrm{PSD}_{1/f}\propto\frac{1}{f^{\alpha}} \tag{9}$$

The overall noise current density in our device is calculated by combining all three contributions in a root-mean-square manner:

$$\mathrm{PSD_{overall}}=\sqrt{\mathrm{PSD_{shot}^2}+\mathrm{PSD_{thermal}^2}+\mathrm{PSD_{1/f}^2}} \tag{10}$$

Based on the measured $\mathrm{PSD_{overall}}$, the specific detectivity (D^*) of the photodetector is calculated using the following expression:

$$D^*=\frac{R\sqrt{A}}{\mathrm{PSD_{overall}}} \tag{11}$$

where R is the responsivity (A/W), A is the active area of the photodetector (cm^2), and $\mathrm{PSD_{overall}}$ is the total noise current density ($A/Hz^{1/2}$) under actual operating conditions. This formulation enables a direct and reliable evaluation of photodetector sensitivity by incorporating the relevant noise mechanisms under actual operating conditions.

To accurately evaluate the dominant noise mechanism in our device, we performed a systematic characterization of 1/f noise behavior under various electrical bias conditions. As shown in **Supplementary Figure 15**, we investigated the effect of gate voltage by presetting the device with different values of V_{G_PRE} ranging from -7 V to 7 V (step=1 V), followed by noise measurements conducted at V_{DS}=0.1 V with V_{GS}

held at 0 V. The extracted PSD spectra, obtained from 5 ms sampled time-domain signals using the Welch method, reveal that the 1/*f* noise magnitude increases with more positive V_{G_PRE}, indicating enhanced carrier accumulation and stronger trap-related fluctuations in the accumulation regime. To assess the influence of drain bias, we conducted further PSD measurements at two representative gate presetting conditions. **Supplementary Figure 16** shows the noise behavior after presetting with V_{G_PRE}=7 V (accumulation regime), where V_{DS} was swept from 0.01 V to 0.09 V. A monotonic increase in PSD amplitude with rising drain voltage was observed, suggesting that carrier injection and increased electric field strength enhance trap-assisted noise. In contrast, **Supplementary Figure 17** presents measurements performed after presetting the device with V_{G_PRE}=-7 V (depletion regime). Under the same V_{DS} sweep, the PSD exhibits substantially lower amplitudes, consistent with suppressed carrier density and weaker trap interaction. Across all conditions, the PSD follows a characteristic $1/f^{\alpha}$ dependence (with $\alpha \approx 1$), confirming the dominance of flicker noise in the low-frequency regime.

Given that the thermal noise is significantly smaller than both the 1/*f* and shot noise under our operating conditions, it was excluded from the detectivity (*D**) recalculation. For example, under a representative bias condition of V_{GS}=7 V and V_{DS}=0.1 V, the drain current is approximately 1 μA, corresponding to a channel resistance of $R_{ch} \approx 100$ kΩ. The corresponding thermal noise power spectral density is calculated as:

$$\mathrm{PSD}_{\mathrm{thermal}}^{2} = \frac{4k_{\mathrm{B}}T}{R_{\mathrm{ch}}} = 1.62 \times 10^{-23}\ \mathrm{A^2/Hz} \tag{12}$$

This value is approximately three orders of magnitude lower than the measured 1/*f* noise (~10^{-20} A^2/Hz; **Supplementary Figure 18**) under the same bias, confirming that thermal noise is negligible in our device. This confirms that thermal noise can be safely neglected relative to the dominant 1/*f* and shot noise. To further clarify which noise component dominates under different bias conditions, we quantitatively analyzed the ratio of 1/*f* noise to shot noise as a function of both gate and drain voltages. As shown in **Supplementary Figure 19**, this ratio remains consistently greater than one across the entire bias range, often exceeding several orders of magnitude. These results indicate that 1/*f* noise dominates the overall noise behavior of the device. Therefore, only 1/*f* and shot noise were considered in the subsequent evaluation of photodetection performance under realistic operating conditions.

Supplementary Note 5 | Energy consumption calculation for the synaptic device

The estimation of energy consumption for the synaptic device is based on the following equations[23]:

$$E_{\mathrm{programming}} = P_{\mathrm{spike}} \times A_{\mathrm{active}} \times T_{\mathrm{duration}} \tag{13}$$

$$E_{\mathrm{erasing}} = V_{\mathrm{GS}} \times I_{\mathrm{GS}} \times T_{\mathrm{duration}} \tag{14}$$

Here, $E_{\mathrm{programming}}$ and E_{erasing} denote the energy consumption in a single photonic programming process and electric erasing process, respectively. P_{spike}, $A_{\mathrm{active,}}$ and T_{duration} are the optical spike power (6.36 mW/cm^2,

10^{-6} cm^2, 200 μs), the active channel area, and the spike duration, respectively[23]. V_{GS} and I_{GS} represent gate voltage and gate leakage current (-7 V, 1 pA, 100 μs).

$$E_{programming} = 6.36\times10^{-3}\times10^{-6}\times200\times10^{-6} = 1.272\times10^{-15}\ J = 1.272\ fJ$$

$$E_{erasing} = 7\times10^{-12}\times100\times10^{-6} = 0.7\times10^{-15}\ J = 0.7\ fJ$$

Thus, the total energy consumption of a single synaptic spike is approximately 2.0 fJ, confirming the energy-efficient operation of the device and demonstrating its suitability for integration into future low-power neuromorphic computing architectures.

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