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Peer Review File

Coupled Ferroelectric-Anisotropic Optoelectronic Synapse for Polarization-Sensitive Neuromorphic Vision

Corresponding Author: Professor Kah-Wee Ang

Parts of this Peer Review File have been redacted as indicated to remove third-party material.

This file contains all reviewer reports in order by version, followed by all author rebuttals in order by version.

Version 0:

Reviewer comments:

Reviewer #1

(Remarks to the Author)
The author reports on an optoelectronic synapse based on a ReS2 channel and a ferroelectric HfZrO2 (HZO) gate dielectric in a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) ferroelectric field-effect transistor (FeFET) architecture. A floating gate (FG) design is introduced to decouple the ferroelectric polarization from direct doping effects on the 2D channel, thereby reducing charge scattering and preserving carrier mobility. This architecture enables an ultra-low dark current (<1 pA) and high photoresponsivity up to 4×105 A/W even at zero gate bias, due to the polarization-enhanced electric field modulation. Moreover, capacitive matching within the gate stack suppresses depolarization, improving the retention of both electrical and optical states. The device further supports tunable synaptic weights through dual-mode modulation via gate voltage and optical illumination, with energy consumption as low as 3.18 pJ per event.

This manuscript presents a well-structured and compelling study that makes a valuable contribution to the field of neuromorphic vision systems. The research question is clearly articulated, the methodology is rigorous, and the results are presented with appropriate analysis and discussion. I suggest to accept this manuscript. However, some issues need to be addressed before the manuscript can be published.

1. In the manuscript, on page 11, line 240, “These photoexcited carriers…by the built-in electric field,”. The built-in electric field refers to the electric field generated within a semiconductor or insulator as a result of internal phenomena, rather than from an external source. However, the photoexcited carriers in the FeFET ReS2 channel should be driven by the bias applied from the source and drain electrodes, rather than by the built-in electric field.

2. It is a scientific standard for photodetector papers to present actual measurements of noise to evaluate specific detectivity. This is because of the ubiquitous presence of 1/f noise that can be dominant, especially when bias is present. The expression of D* on page 11 has often been misused, without considering which noise mechanism is dominant in the device. As such, the noise analysis and value of D* are likely incorrect.

3. The voltage conditions for the EPSC response illustrated in Fig. 2d should be specified.

4. In the manuscript, on page 8, line 191, “Long-term potentiation…varying pulse widths (10 μs, 50 μs, 100 μs, 500 μs and 1 ms)”. The description of the pulse widths is inconsistent with that presented in Fig. 2e.

5. In the manuscript, on page 15, line 327, “In Fig. 4g, light pulses (0.5 s duration, 636.9 pW power, and 658 nm wavelength) …”. Fig. 4g should be Fig. 4d.

6. Fig. 4g should add auxiliary lines to assist in identifying the current corresponding to the start of the pulse. The related works in neuromorphic vision systems are not cited [e.g., Nature Electronics, 2024, 7, 705-713; Nature Nanotechnology, 2024, 19, 919-930]

Reviewer #2

(Remarks to the Author)
This research article presents a conceptual optoelectronic synaptic device based on an MFMIS FeFET architecture, incorporating a ReS_2 channel and an HZO gate dielectric, aimed at applications in neuromorphic vision systems. The demonstrated device shows good photodetection sensitivity and stable non-volatile memory performance, attributed to built-in ferroelectric polarization. Moreover, dual-mode modulation enables linear and tunable synaptic behavior.
However, the article lacks a clear explanation of the functional advantages conferred by the use of ReS_2 as the channel material, especially in comparison to alternative options. While the integration of HZO as the gate dielectric within an MFMIS structure is acknowledged, its novelty—beyond its pairing with ReS_2—requires further elaboration and contextualization with respect to existing literature. The manuscript does not adequately address the rationale for selecting ReS_2, nor does it convincingly articulate the resulting improvements in device performance or the underlying mechanisms that contribute to any scientific advancement. Without a more comprehensive discussion of the unique role and contributions of the ReS_2 channel, as well as a clearer distinction from prior work, the significance and broader impact of this research remain insufficiently justified. Therefore, it is difficult to recommend the publication.

Please note the following comments intended to help improve the quality of the manuscript.

1. The actual image of the fabricated device should be included in the main text. If all the device characteristics were measured from the single device shown in Figure 1, the reliability of the data is significantly compromised. It is necessary to present statistical data to support the findings.
2. While the authors utilize ReS_2 as the channel material in the FeFET, the manuscript does not provide a compelling justification for this choice over more extensively studied 2D semiconductors such as MoS_2 or WS_2, which often demonstrate superior optoelectronic performance.
3. The optical micrograph shown in Figure 1C lacks a scale bar, making it difficult to assess the physical dimensions of the device and limiting its utility for replication or comparative analysis.
4. In Figure S4e, a leakage current of approximately 10 nA is reported, which is relatively high and does not support the classification of the device as exhibiting “low leakage” for FeFET applications. Additionally, the actual area of the MIM capacitor used for leakage testing is not specified, preventing accurate calculation of current density and hindering meaningful comparison with existing literature.
5. Although Figure 2i demonstrates excellent electrical endurance over 10^5 cycles, the manuscript does not include endurance data for repeated optical programming. Such data are crucial for evaluating the long-term reliability of optically induced nonvolatile states in neuromorphic applications.
6. In Figure 2e, the LTP curves corresponding to 500 μs and 1 ms pulse widths display significant nonlinearity, which appears inconsistent with the manuscript's claim of linear conductance modulation.
7. The reported energy consumption per synaptic event (3.18 pJ) seems low; however, it is calculated using a 0.5 s light pulse—substantially longer than the typical spike durations (<1 ms) used in neuromorphic systems. Given the device’s fast optical response time (<100 μs), it is reasonable to expect that a shorter pulse would result in even lower energy consumption, which should be discussed.

Reviewer #3

(Remarks to the Author)
The main contents of this work can be summarized as following: (1) constructing the HZO floating gate based FeFET for non-volatile memory and suppressing dark currents of the ReS2 photodetector (DOI: 10.1109/TED.2024.3386508; DOI: 10.1109/TED.2024.3371945; https://onlinelibrary.wiley.com/doi/full/10.1002/smll.202311630); (2) using synergetic photoelectric/electric modulation to generate synaptic plasticity to provide weight values for ANN computation （https://pubs.acs.org/doi/full/10.1021/acsnano.4c11898; https://onlinelibrary.wiley.com/doi/full/10.1002/smll.202311630）. There is a great deal of this kind of work. Therefore, the referee considered that this work has not shown sufficient differences from others and be lack of novelty.

The MFMIS device structure is shown in Fig 1c. Is the HZO point (left) on the same layer of the HZO layer under the channel (right)? What would be the difference between the MFMIS and MFIS devices with the same materials?

Version 1:

Reviewer comments:

Reviewer #1

(Remarks to the Author)
The authors have made satisfactory revisions. I would recommend the acceptance.

Reviewer #2

(Remarks to the Author)
The authors have made considerable efforts to address the previous reviewers' comments. Nevertheless, they have not provided a clear or satisfactory resolution to the most critical weakness of this work — the lack of sufficient novelty. Furthermore, for many of the previously raised concerns, their responses remain unconvincing or insufficiently clear.

Therefore, consistent with my earlier assessment, it is difficult to recommend this work for publication.

Reviewer #4

(Remarks to the Author)
The author reports an optoelectronic synapse based on a 2D ReS2 channel and a ferroelectric HfZrO2 (HZO) gate dielectric in a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) ferroelectric field-effect transistor (FeFET). Moreover, linear and tunable synaptic behavior is achieved via optical-electrical dual-mode modulation, with energy consumption as low as 2.0 fJ per synaptic event. I believe the author chose ReS_2 as the channel material because of its polarization properties. However, the research on polarization properties in this paper is quite limited, and the advantages of using ferroelectric gate dielectrics and the MFMIS structure for polarization properties have not been demonstrated. Therefore, the article lacks a clear novelty and is not recommended for publication in NC.

Please note that the following comments can be used to further improve the quality of the manuscript.

(1)Has the polarization property of ReS2 been improved by using ferroelectric gate dielectric and MFMIS? In what aspects is this manifested? For example, maximum polarized responsivity? dichroic ratio?

(2)Please explain in detail what the symbol “T” represents in Figure 4j and how it is related to the device. Is the application of this scenario only possible with devices that have ferroelectric long-time plasticity? If not, what are the advantages of the ferroelectric device proposed by the author in such scenarios?

(3)Similarly, what is the connection between the algorithm shown in Figure 5 and ferroelectric polarization and polarization characteristics, and why is it employed here?

Reviewer #5

(Remarks to the Author)
Optical performance of ReS2 FeFET is very impressive. I would suggest following clarifications to make what is based on real experiment or not.

1)Even Figure 1c shows device using very small ReS2 crystal piece, but the next figure is a schematic of large array. Is this array actually fabricated?
2) Fig.4. Fig.5 assumes large array operation, but it doesn't look like the authors made actual array. 3) The authors should include the time scale discussion on the operation mechanism whether the current speed of sensing and programming is suitable for the operation/ image sensing claimed by the authors.

Version 2:

Reviewer comments:

Reviewer #2

(Remarks to the Author)
Although the authors have made efforts to address prior reviewer feedback, their revisions remain inadequate. The most critical weakness—the lack of sufficient novelty—has not been resolved. In addition, many of their responses are vague, unconvincing, or insufficiently detailed, leaving key concerns unaddressed. This lack of clarity undermines confidence in the robustness of the study and reinforces the earlier conclusion that the manuscript does not meet the standards required for publication.
Moreover, the study relies solely on a single unit device for computing, rather than demonstrating an array configuration as indicated in Figure 5b. Devices fabricated with small flakes inherently suffer from non-uniformity, instability, and poor reliability. Without presenting an array of ReS_2 devices with consistent and reproducible characteristics, the work fails to convincingly demonstrate realistic functionality or scalability. This omission substantially weakens the practical relevance and impact of the reported results.

Reviewer #4

(Remarks to the Author)
It has been well revised, and can be accepted.

Reviewer #5

(Remarks to the Author)
The authors clarified many concerns and revised manuscript to restrict the application to neuromorphic vision applications. I am not fully convinced what is the role of neuromorphic vision processing whose speed is limited to ~ KHz operation. Yet, I think this manuscript has enough novelty for the publication.

Dear Editor,

We really appreciate your help, the reviewers' comments and valuable suggestions. According to all the comments and suggestions, the manuscript has been revised carefully and extensively. We hope that the additional experiments and clarifications have fully addressed the reviewers' concerns. The responses to the reviewers' comments are listed as follows:

========== Authors' responses to the reviewer's comments ==========

Reviewer #1

The author reports on an optoelectronic synapse based on a ReS_2 channel and a ferroelectric $HfZrO_2$ (HZO) gate dielectric in a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) ferroelectric field-effect transistor (FeFET) architecture. A floating gate (FG) design is introduced to decouple the ferroelectric polarization from direct doping effects on the 2D channel, thereby reducing charge scattering and preserving carrier mobility. This architecture enables an ultra-low dark current (<1 pA) and high photoresponsivity up to 4×10^5 A/W even at zero gate bias, due to the polarization-enhanced electric field modulation. Moreover, capacitive matching within the gate stack suppresses depolarization, improving the retention of both electrical and optical states. The device further supports tunable synaptic weights through dual-mode modulation via gate voltage and optical illumination, with energy consumption as low as 3.18 pJ per event.

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Comment #1

1. In the manuscript, on page 11, line 240, "These photoexcited carriers…by the built-in electric field,". The built-in electric field refers to the electric field generated within a semiconductor or insulator as a result of internal phenomena, rather than from an external source. However, the photoexcited carriers in the FeFET ReS_2 channel should be driven by the bias applied from the source and drain electrodes, rather than by the built-in electric field.

Our response:

We thank the reviewer for the insightful comment. We agree that the previous use of the term "built-in electric field" may have led to confusion. In our device, the photoexcited carriers are

separated primarily by the external electric field applied between the source and drain electrodes, rather than by a built-in field arising from internal junctions or polarization effects.

To clarify this mechanism, we have revised the sentence on page 11 (line 240) as follows:

Original:

"These photoexcited carriers are efficiently separated by the built-in electric field, resulting in a measurable photocurrent."

Revised:

"These photoexcited carriers are efficiently separated by the external electric field applied between the source and drain, resulting in a measurable photocurrent."

Corresponding change:

Page: 10

Comment #2

2. It is a scientific standard for photodetector papers to present actual measurements of noise to evaluate specific detectivity. This is because of the ubiquitous presence of 1/f noise that can be dominant, especially when bias is present. The expression of D* on page 11 has often been misused, without considering which noise mechanism is dominant in the device. As such, the noise analysis and value of D* are likely incorrect.

Our response:

We thank the reviewer for highlighting the importance of presenting accurate noise measurements when evaluating specific detectivity (D^*), particularly given the ubiquitous presence of 1/f noise under bias conditions. We acknowledge that our earlier analysis did not provide a comprehensive breakdown of the dominant noise mechanisms, which may have led to an incomplete assessment of D^*.

To address this concern, we now present a detailed analysis of the key noise sources that influence photodetector performance and ultimately determine the detectivity. The total noise typically arises from three main contributions: shot noise, thermal noise, and 1/f (flicker) noise. Below, we present a detailed analysis of each noise component and its combined impact on the calculation of D^*.

Shot noise arises due to the discrete nature of charge carriers and follows Poisson statistics. It is primarily governed by the dark current (I_{DS}), and its noise current spectral density is given by:

$$PSD_{shot} = \sqrt{2qI_{DS}}$$

where I_{DS} is the dark current is the drain current in the dark condition, and q is the electron charge. Shot noise is more pronounced at low illumination levels and high frequencies.

Thermal noise results from the random thermal motion of charge carriers within a conductor. In photodetectors, it is influenced by the channel resistance (R_{ch}) and temperature. The PSD for thermal noise is expressed as:

$$PSD_{thermal} = \sqrt{\frac{4k_BT}{R_{ch}}}$$

where k_B is the Boltzmann constant (1.381×10^{-23} J/K), T is the ambient temperature (293 K), and R_{ch} corresponds to channel resistance ($R_{ch}=V_{DS}/I_{DS}$). Thermal noise is more prominent at higher temperatures and lower resistances.

1/f noise, or flicker noise, is characterized by a power spectral density that is inversely proportional to frequency ($1/f_{\alpha}$, with α typically between 0.8 and 1.2). It originates from low-frequency fluctuations in charge carrier density or mobility. This noise dominates at low frequencies (typically below 100 Hz–100 kHz, depending on the device) and is highly dependent on the device's material properties and operating conditions.

$$PSD_{1/f} \propto \frac{1}{f^{\alpha}}$$

The overall noise current density in our device is calculated by combining all three contributions in a root-mean-square manner:

$$PSD_{overall} = \sqrt{PSD_{shot}^2 + PSD_{thermal}^2 + PSD_{1/f}^2}$$

Based on the measured $PSD_{overall}$, the specific detectivity (D^*) of the photodetector is calculated using the following expression:

$$D^* = \frac{R\sqrt{A}}{PSD_{overall}}$$

where R is the responsivity (A/W), A is the active area of the photodetector (cm^2), and $PSD_{overall}$ is the total noise current density ($A/Hz^{1/2}$) under actual operating conditions. This formulation enables a direct and reliable evaluation of photodetector sensitivity by incorporating the relevant noise mechanisms under actual operating conditions.

To accurately evaluate the dominant noise mechanism in our device, we performed a systematic characterization of 1/f noise behavior under various electrical bias conditions. As shown in **Fig. S15**, we investigated the effect of gate voltage by presetting the device with different values of V_{G_PRE} ranging from -7 V to 7 V (step = 1 V), followed by noise measurements conducted at V_{DS} = 0.1 V

with V_{GS} held at 0 V. The extracted PSD spectra, obtained from 5 ms sampled time-domain signals using the Welch method, reveal that the 1/f noise magnitude increases with more positive V_{G_PRE}, indicating enhanced carrier accumulation and stronger trap-related fluctuations in the accumulation regime. To assess the influence of drain bias, we conducted further PSD measurements at two representative gate programming conditions. **Fig. S16** shows the noise behavior after programming with V_{G_PRE} = 7 V (accumulation regime), where V_{DS} was swept from 0.01 V to 0.09 V. A monotonic increase in PSD amplitude with rising drain voltage was observed, suggesting that carrier injection and increased electric field strength enhance trap-assisted noise. In contrast, **Fig. S17** presents measurements performed after erasing the device with V_{G_PRE} = -7 V (depletion regime). Under the same V_{DS} sweep, the PSD exhibits substantially lower amplitudes, consistent with suppressed carrier density and weaker trap interaction. Across all conditions, the PSD follows a characteristic 1/f^α dependence (with α ≈ 1), confirming the dominance of flicker noise in the low-frequency regime.

Given that the thermal noise is significantly smaller than both the 1/f and shot noise under our operating conditions, it was excluded from the detectivity (D^*) recalculation. For example, under a representative bias condition of V_{GS} = 7 V and V_{DS} = 0.1 V, the drain current is approximately 1 μA, corresponding to a channel resistance of R_{ch} ≈100 kΩ. The corresponding thermal noise power spectral density is calculated as:

$$PSD_{thermal}^2 = \frac{4k_BT}{R_{ch}} = 1.62 \times 10^{-23}\ A^2/Hz$$

This value is approximately three orders of magnitude lower than the measured 1/f noise (~10^{-20} A^2/Hz; **Fig.S18**) under the same bias, confirming that thermal noise is negligible in our device. This confirms that thermal noise can be safely neglected relative to the dominant 1/f and shot noise. Accordingly, D^* was recalculated based solely on these two contributions under realistic bias conditions, providing a more reliable assessment of the device's photodetection capability.

To further clarify which noise component dominates under different bias conditions, we quantitatively analyzed the ratio of 1/f noise to shot noise as a function of both gate and drain voltages. As shown in **Fig. S19**, this ratio remains consistently greater than one across the entire bias range, often exceeding several orders of magnitude. These results indicate that 1/f noise dominates the overall noise behavior of the device. This finding further underscores the necessity of including 1/f noise in the D^* recalculation to ensure accurate and meaningful performance evaluation.

The updated D^* values presented in **Fig. 3f** and **3g** incorporate both shot noise and 1/f noise, capturing the bias-dependent noise characteristics of the system. Compared to the initial calculation that neglected 1/f noise, the revised D^* values are reduced by approximately one order of magnitude, as illustrated in **Fig. R1**. Detailed discussions on noise sources and calculation methodology have

been added to the main text and **Supplementary Note S3**. This approach enables a more accurate and meaningful comparison with other state-of-the-art photodetectors, thereby enhancing the reliability of our performance evaluation under realistic operating conditions.

Corresponding change:

Page: 13

Figure: Fig.3f, Fig.3g, Fig.S15-S19, Supplementary Note S3

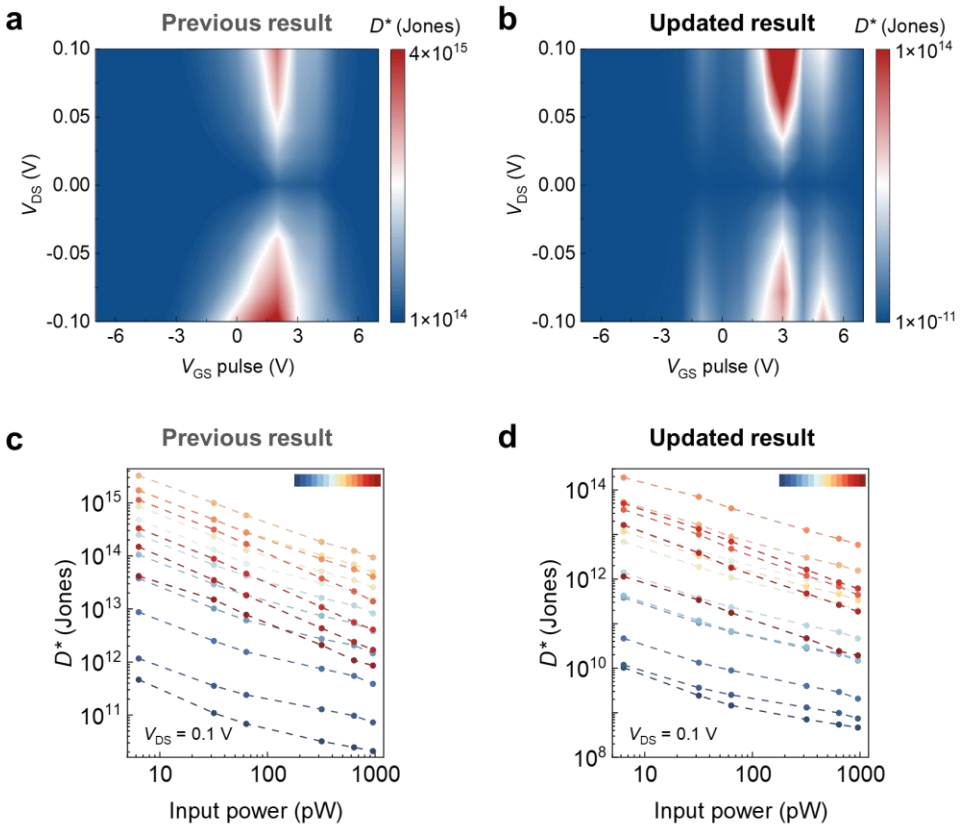


Fig. R1 Comparison of detectivity before and after correction. After incorporating actual noise spectral density, the calculated D* decreases by approximately one order of magnitude.

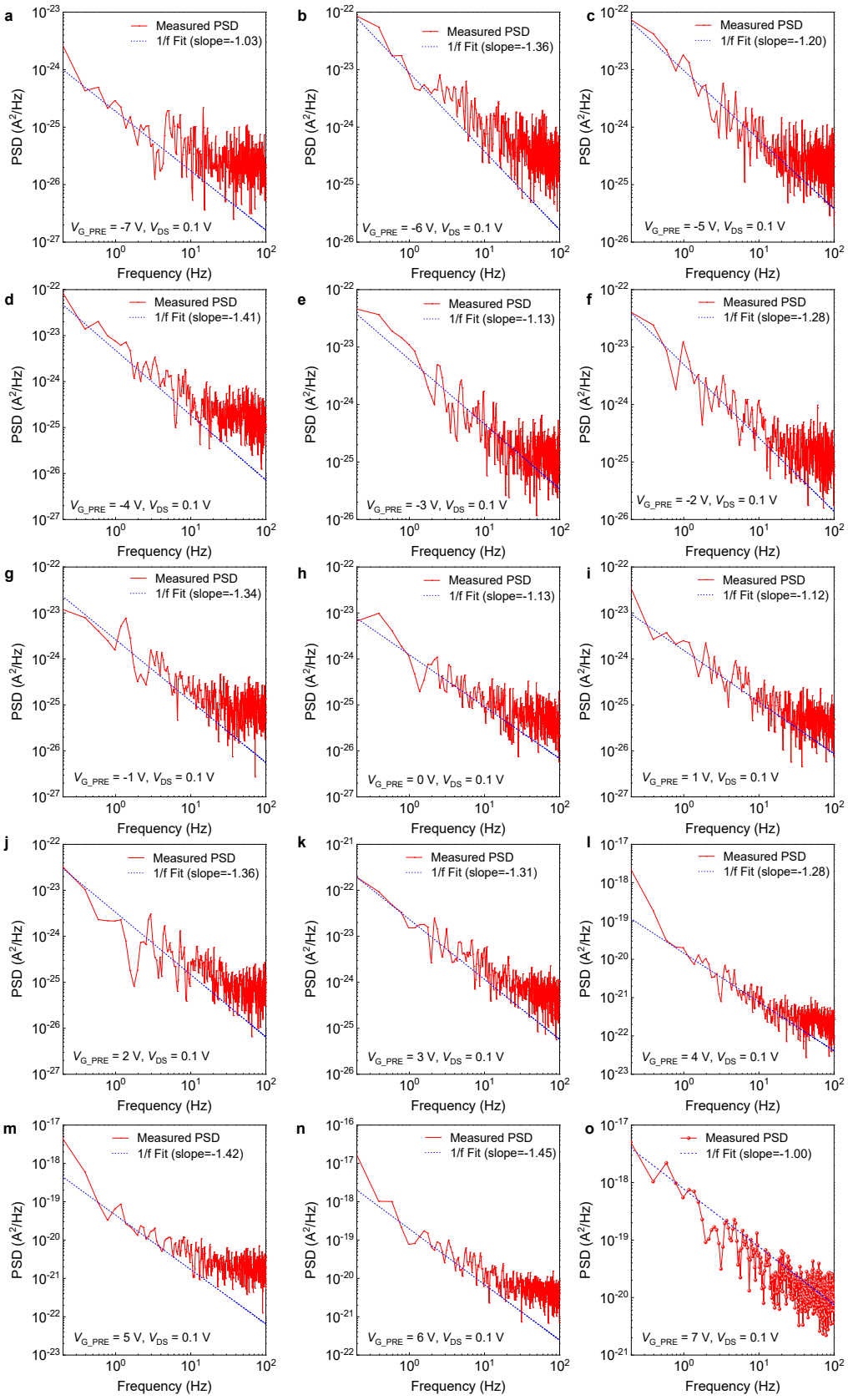

a
Measured PSD
1/f Fit (slope=-1.03)
V_{G_PRE} = -7 V, V_{DS} = 0.1 V
b
Measured PSD
1/f Fit (slope=-1.36)
V_{G_PRE} = -6 V, V_{DS} = 0.1 V
c
Measured PSD
1/f Fit (slope=-1.20)
V_{G_PRE} = -5 V, V_{DS} = 0.1 V
d
Measured PSD
1/f Fit (slope=-1.41)
V_{G_PRE} = -4 V, V_{DS} = 0.1 V
e
Measured PSD
1/f Fit (slope=-1.13)
V_{G_PRE} = -3 V, V_{DS} = 0.1 V
f
Measured PSD
1/f Fit (slope=-1.28)
V_{G_PRE} = -2 V, V_{DS} = 0.1 V
g
Measured PSD
1/f Fit (slope=-1.34)
V_{G_PRE} = -1 V, V_{DS} = 0.1 V
h
Measured PSD
1/f Fit (slope=-1.13)
V_{G_PRE} = 0 V, V_{DS} = 0.1 V
i
Measured PSD
1/f Fit (slope=-1.12)
V_{G_PRE} = 1 V, V_{DS} = 0.1 V
j
Measured PSD
1/f Fit (slope=-1.36)
V_{G_PRE} = 2 V, V_{DS} = 0.1 V
k
Measured PSD
1/f Fit (slope=-1.31)
V_{G_PRE} = 3 V, V_{DS} = 0.1 V
l
Measured PSD
1/f Fit (slope=-1.28)
V_{G_PRE} = 4 V, V_{DS} = 0.1 V
m
Measured PSD
1/f Fit (slope=-1.42)
V_{G_PRE} = 5 V, V_{DS} = 0.1 V
n
Measured PSD
1/f Fit (slope=-1.45)
V_{G_PRE} = 6 V, V_{DS} = 0.1 V
o
Measured PSD
1/f Fit (slope=-1.00)
V_{G_PRE} = 7 V, V_{DS} = 0.1 V
PSD (A^2/Hz)
Frequency (Hz)

Fig. S15 1/f noise power spectral density (PSD) of the dark current measured under a fixed drain bias of V_{DS} = 0.1 V after presetting the device with different gate voltages (V_{G_PRE}) ranging from -7 V to 7 V in 1 V steps. During the noise measurement, V_{GS} was held at 0 V. **a-i** correspond to different V_{G_PRE} values, showing the evolution of 1/f noise characteristics as a function of programming gate voltage. The PSD was calculated over a frequency range of 0.1 Hz to 100 Hz.

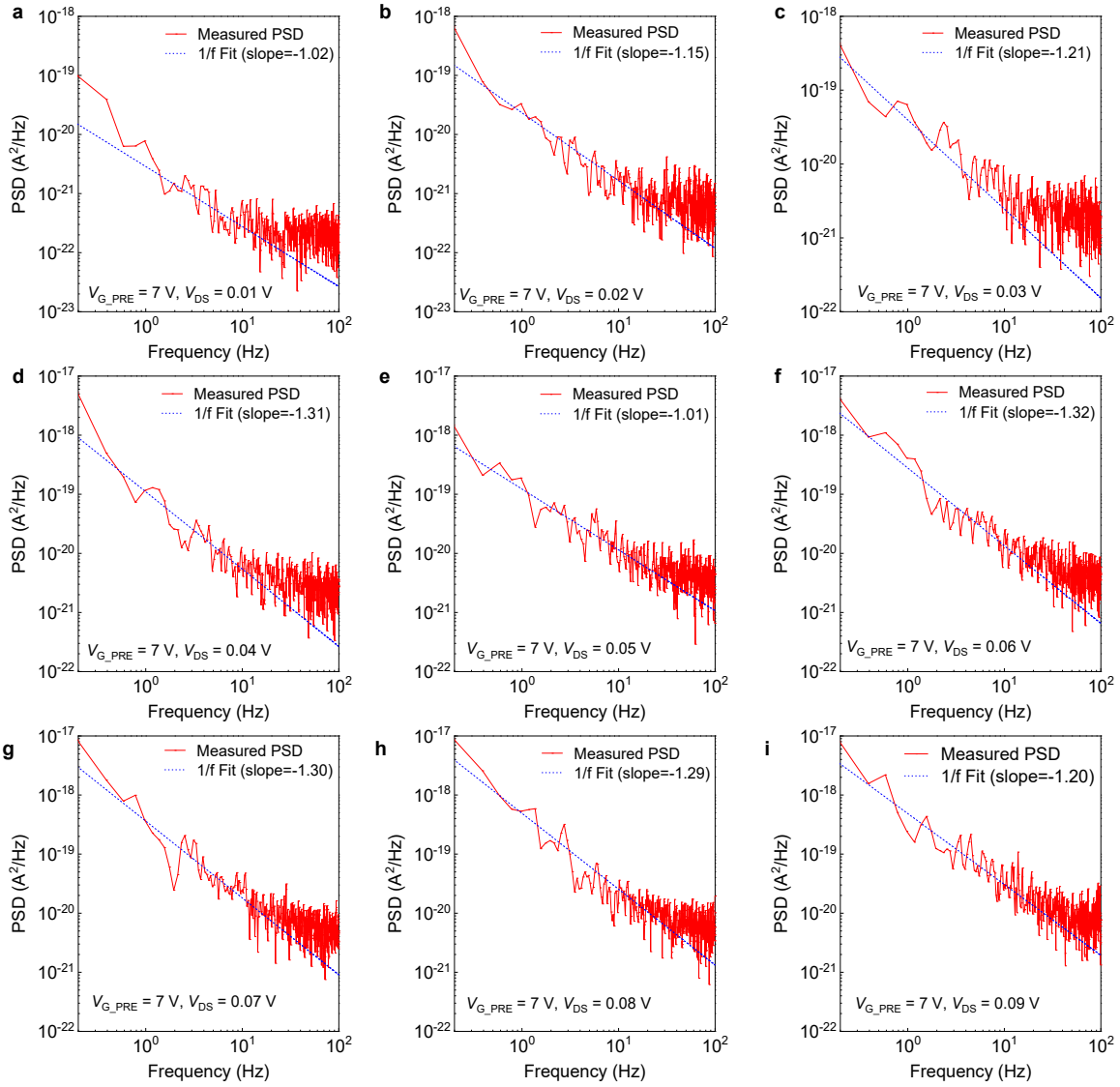


Fig. S16 1/f noise PSD of the dark current measured in the accumulation regime after presetting the device with V_{G_PRE} = 7 V. During the noise measurement, V_{GS} was held at 0 V while V_{DS} was swept from 0.01 V to 0.09 V in 0.01 V increments. **a-i** correspond to different V_{DS} values, showing the influence of drain voltage on 1/f noise behavior. The PSD was calculated over a frequency range of 0.1 Hz to 100 Hz.

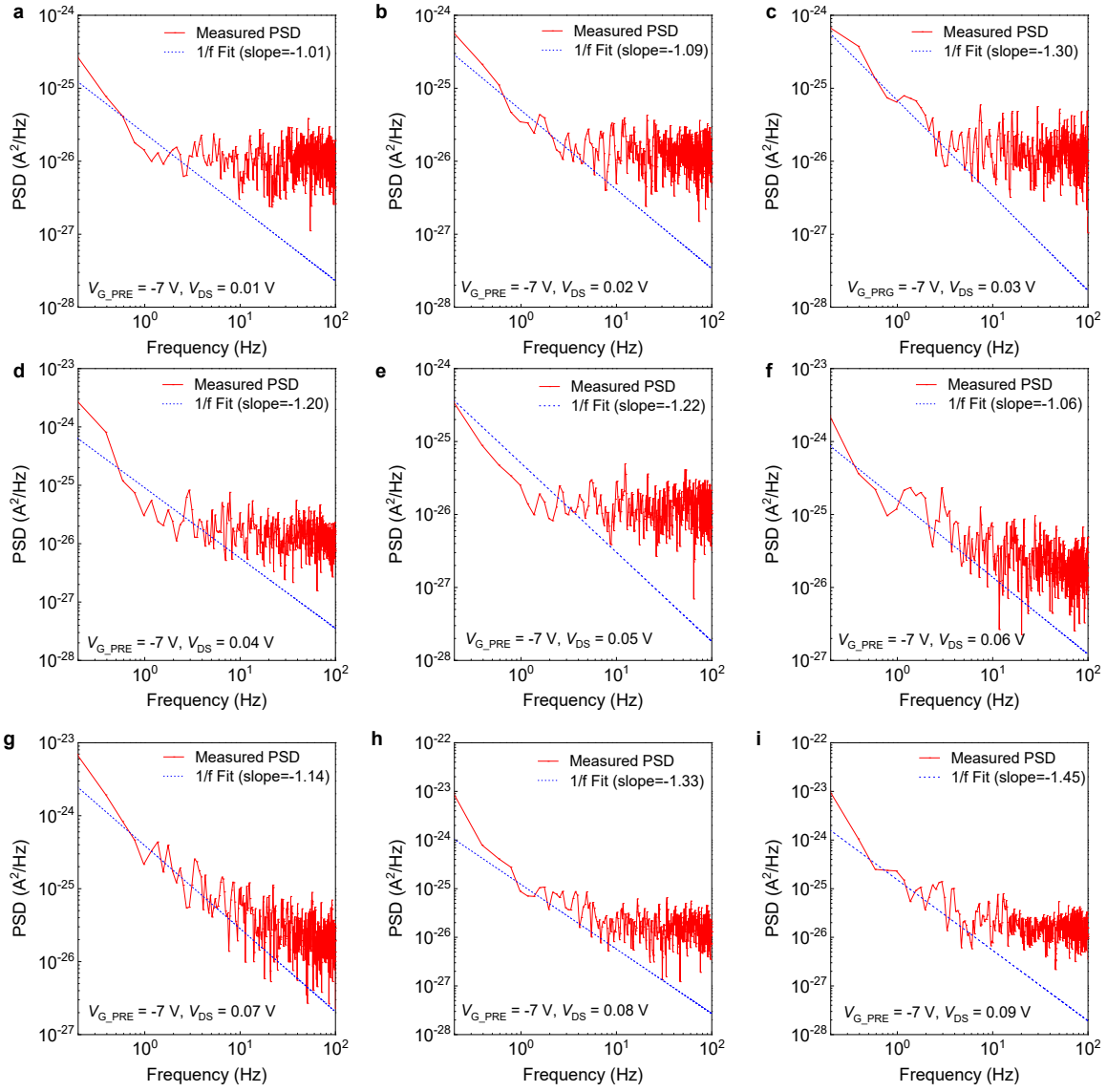


Fig. S17 1/f PSD of the dark current measured in the depletion regime after presetting the device with V_{G_PRE} = -7 V. During the noise measurement, V_{GS} was held at 0 V while V_{DS} was swept from 0.01 V to 0.09 V in 0.01 V increments. **a-i** correspond to different V_{DS} values, showing the influence of drain voltage on 1/f noise behavior. The PSD was calculated over a frequency range of 0.1 Hz to 100 Hz.

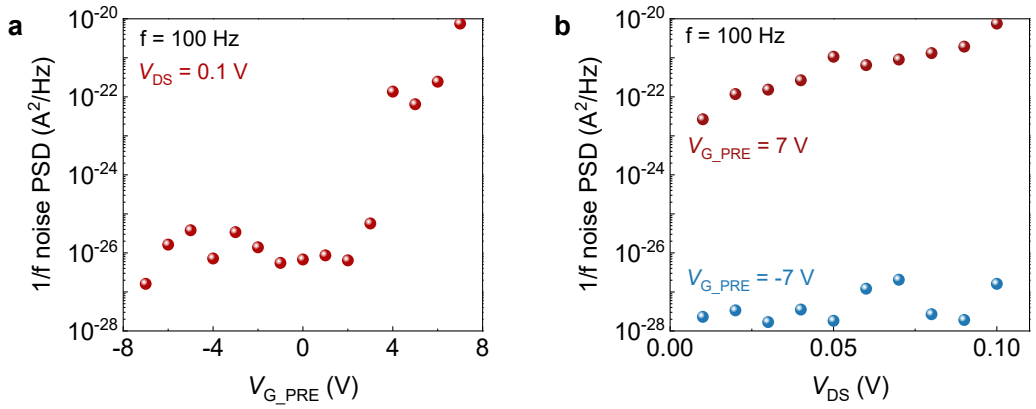


Fig. S18 Bias-dependent 1/f noise characteristics. **a.** Drain current noise PSD at 100 Hz as a function of V_{G_PRE}, measured at a fixed drain bias of V_{DS} = 0.1V. **b.** Noise PSD versus V_{DS} under two representative gate biases: V_{G_PRE} = 7 V (accumulation) and V_{G_PRE} = -7 V (depletion), highlighting the dependence of noise on channel conductance.

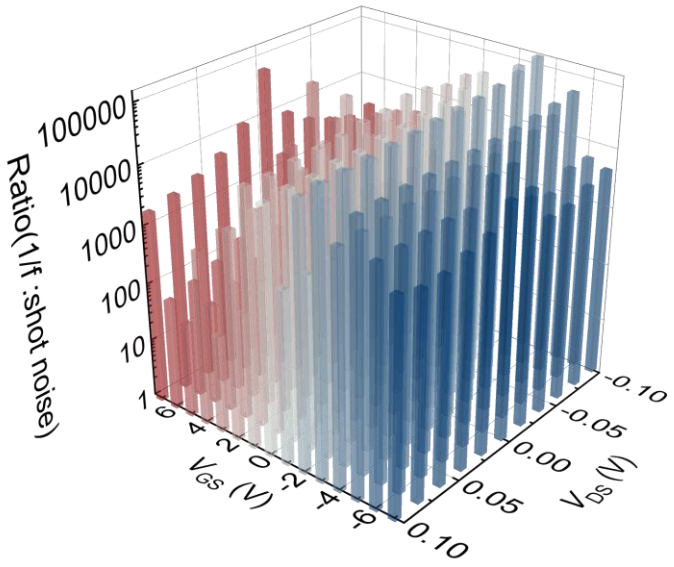


Fig. S19 Three-dimensional bar plot presenting the ratio of 1/f noise to shot noise as a function of V_{GS} and V_{DS}. This ratio quantitatively represents the relative strength of the two noise components. The consistently large values across all biasing conditions indicate that 1/f noise dominates the total noise behavior of the device.

Comment #3

3. The voltage conditions for the EPSC response illustrated in Fig. 2d should be specified.

Our response:

We thank the reviewer for pointing out the need to clarify the voltage conditions for the EPSC measurement originally presented in Fig. 2d. In our experiments, the EPSC responses were measured under a fixed V_{GS} of 7 V, with varying input pulse widths ranging from 100 μs to 100 ms. As part of our manuscript revision and reorganization of figures, this panel has now been relocated to **Fig. 2f**. To address the reviewer's concern, we have updated the main text as follows:

Original:

*"The excitatory postsynaptic current (EPSC) responses (**Fig. 2d**) show persistent output across input pulse widths ranging from 100 μs to 100 ms, evidencing extended temporal retention."*

Revised:

*"The excitatory postsynaptic current (EPSC) responses (**Fig. 2f**) show persistent output across a range of input pulse widths from 100 μs to 100 ms at a constant gate voltage V_{GS} of 7.0 V, demonstrating extended temporal retention."*

In addition, we have updated the figure caption of **Fig. 2f**:

*"**f.** EPSC response under a single gate pulse (V_{GS} = 7.0 V) with varying pulse widths, showing current retention."*

We have also labeled the voltage condition (V_{GS} = 7.0 V) in the figure itself for clarity. We thank the reviewer for helping us improve the completeness of the data presentation.

Corresponding change:

Page: 9-10

Figure: Fig.2f

Comment #4

4. In the manuscript, on page 8, line 191, "Long-term potentiation…varying pulse widths (10 μs, 50 μs, 100 μs, 500 μs and 1 ms)". The description of the pulse widths is inconsistent with that presented in Fig. 2e.

Our response:

We appreciate the reviewer's careful observation. The pulse widths described in the manuscript for the LTP measurements in Fig. 2e were incorrectly listed. The actual pulse widths used in the experiments were 50 μs, 100 μs, 200 μs, 500 μs, and 1 ms, which were correctly shown in **Fig. 2e**, but inconsistently described in the main text and figure caption.

In our revised manuscript, we have corrected this inconsistency by updating both the main text and the figure caption. Additionally, due to figure reorganization, the original **Fig. 2e** now appears as **Fig. 2g**.

Original:

"Long-term potentiation (LTP) evaluated by applying identical positive gate pulses V_{GS} (5.0 V) with varying pulse widths (10 μs, 50 μs, 100 μs, 500 μs, and 1 ms), reveals gradual and linear conductance modulation (Fig. 2e), a key feature for weight tuning in neuromorphic learning."

Revised:

*"Long-term potentiation (LTP), induced by identical +5 V gate pulses with varying pulse widths (50 μs, 100 μs, 200 μs, 500 μs, and 1 ms), reveals gradual and linear conductance modulation (**Fig. 2g**), a key feature for synaptic weight tuning in neuromorphic learning."*

The figure caption for **Fig. 2g** has been updated:

"LTP behavior under a series of identical V_{GS} pulses (5.0 V) with pulse widths of 50 μs to 1 ms."

In addition, we have verified that the correct pulse widths are accurately reflected in the figure itself. We thank the reviewer again for pointing out this inconsistency, which helped improve the precision of our manuscript.

Corresponding change:

Page: 10

Figure: Fig.2g

Comment #5

5. In the manuscript, on page 15, line 327, "In Fig. 4g, light pulses (0.5 s duration, 636.9 pW power, and 658 nm wavelength)…". Fig. 4g should be Fig. 4d.

Our response:

We thank the reviewer for pointing out the figure labeling error. The reference to "Fig. 4g" in the manuscript was incorrect. The correct figure is Fig. 4d, which illustrates the application of light pulses to simulate the initial learning process.

Original:

"In Fig. 4g, light pulses (0.5 s duration, 636.9 pW power, and 658 nm wavelength) were applied consecutively to the ReS_2 channels over 40 s to mimic the brain's initial learning process."

Revised:

*"To evaluate learning and forgetting behavior, **Fig. 4d** shows that continuous 0.5 s light pulses (636.9 pW) over 40 s elevate EPSC to ~1 nA, which decays to 0.5 nA after stimulus removal, mimicking biological forgetting."*

Corresponding change:

Page: 14

Comment #6

6. Fig. 4g should add auxiliary lines to assist in identifying the current corresponding to the start of the pulse. The related works in neuromorphic vision systems are not cited [e.g., Nature Electronics, 2024, 7, 705-713; Nature Nanotechnology, 2024, 19, 919-930].

Our response:

We sincerely thank the reviewer for the constructive suggestions regarding both the clarity of **Fig. 4g** and the inclusion of relevant recent literature on neuromorphic vision systems.

To improve the readability of **Fig. 4g**, which illustrates the dynamic optoelectronic modulation process involving optical programming followed by electrical erasure under a gate bias of V_{GS} = -7 V, we have updated the figure by adding auxiliary vertical dashed lines that mark the onset of each optical pulse. These lines serve as clear visual indicators that assist in identifying the current response corresponding to each stimulus. This addition enhances the figure by allowing readers to more easily correlate the applied optical inputs with the device's current modulation behavior during the programming and erasing cycles. Due to figure rearrangement, the updated panel is now presented as **Fig. S24** in the revised manuscript.

In addition, we greatly appreciate the reviewer's recommendation of two recent and highly relevant studies on neuromorphic vision systems. These works provide important context for our device's functionality in terms of visual learning and memory behavior. We have now cited the following references in the revised manuscript to better align our work with the latest developments in the field:

[2] Wang, Z., Wan, T., Ma, S. & Chai, Y. Multidimensional vision sensors for information processing. Nat. Nanotechnol. 19, 919-930 (2024).

[10] Ouyang, B. et al. Bioinspired in-sensor spectral adaptation for perceiving spectrally distinctive features. Nat. Electron. 7, 705-713 (2024).

These references have been incorporated into both the main text and the reference list to ensure comprehensive and consistent coverage. We once again thank the reviewer for the valuable suggestions that have improved the clarity and positioning of our work.

Corresponding change:

Page: S-25

Figure: Fig. S24

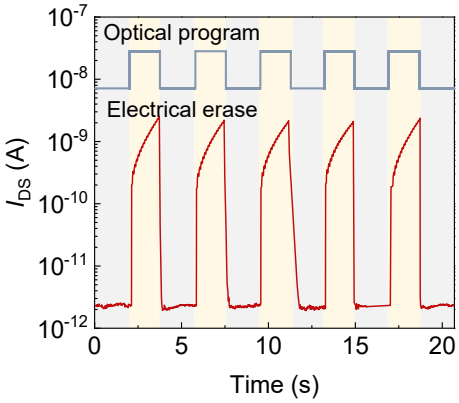


Fig. S24. Optical programming and electrical erasing. The figure demonstrates the dynamic process of optoelectronic co-modulation, wherein the device is first programmed optically, followed by electrical erasing via a gate voltage of V_{GS} = -7 V. This program–erase cycle is repeated to showcase the device's ability to achieve optoelectronic control, enabling a robust system for information writing and erasure.

Reviewer #2

This research article presents a conceptual optoelectronic synaptic device based on an MFMIS FeFET architecture, incorporating a ReS_2 channel and an HZO gate dielectric, aimed at applications in neuromorphic vision systems. The demonstrated device shows good photodetection sensitivity and stable non-volatile memory performance, attributed to built-in ferroelectric polarization. Moreover, dual-mode modulation enables linear and tunable synaptic behavior.

However, the article lacks a clear explanation of the functional advantages conferred by the use of ReS_2 as the channel material, especially in comparison to alternative options. While the integration of HZO as the gate dielectric within an MFMIS structure is acknowledged, its novelty—beyond its pairing with ReS_2—requires further elaboration and contextualization with respect to existing literature. The manuscript does not adequately address the rationale for selecting ReS_2, nor does it convincingly articulate the resulting improvements in device performance or the underlying mechanisms that contribute to any scientific advancement. Without a more comprehensive discussion of the unique role and contributions of the ReS_2 channel, as well as a clearer distinction from prior work, the significance and broader impact of this research remain insufficiently justified. Therefore, it is difficult to recommend the publication.

Please note the following comments intended to help improve the quality of the manuscript.

Comment #1

1. The actual image of the fabricated device should be included in the main text. If all the device characteristics were measured from the single device shown in Figure 1, the reliability of the data is significantly compromised. It is necessary to present statistical data to support the findings.

Our response:

We thank the reviewer for the valuable suggestion. In response to this comment, and following the reviewer's recommendation, we have included an actual optical image of the fabricated device in the main text (**Fig. 1c**), in which the source (S), drain (D), and gate (G) regions are clearly labeled to illustrate the device layout and fabrication quality. Additionally, a cross-sectional TEM image is provided to confirm the layered structure of the ReS_2/HfO_2/HZO stack and the integrity of the interfaces. A corresponding description has also been added to the revised manuscript as follows:

*"The device structure and working principle are illustrated in **Fig. 1c**. The top-left optical image shows the fabricated MFMIS FeFET with clearly defined source (S), drain (D), and gate (G)*

regions, confirming successful patterning and alignment. The cross-sectional TEM image below reveals the layered structure of the ReS_2/HfO_2/HZO stack, verifying high-quality interfaces and uniform film thicknesses."

To further address the concern regarding data reliability, we clarify that the results presented in the main text are representative measurements from multiple independently fabricated MFMIS FeFETs, rather than from a single device. We also performed detailed studies on device-to-device (D2D) and cycle-to-cycle (C2C) variability to evaluate the uniformity and reproducibility of our devices.

As detailed in the Supporting Information (**Fig. S10**–**S13**), we performed I_{DS}-V_{GS} measurements on nine individual devices (D1 to D9), each measured over ten consecutive cycles under identical testing conditions (V_{GS} swept from -7.0 V to 7.0 V at V_{DS} = 0.1 V). All devices consistently exhibited stable and repeatable counterclockwise hysteresis loops, confirming robust ferroelectric switching behavior (**Fig. S10**).

We then conducted a comprehensive statistical analysis by extracting key parameters, including on-state current (I_{ON}), off-state current (I_{OFF}), positive and negative threshold voltages (V_{th+} and V_{th-}), the ratio of I_{ON} / I_{OFF}, and memory window (MW), from each cycle of each device, thereby covering both C2C and D2D variability. The corresponding parameter distributions are summarized in **Fig. S11**–**S13**. The calculated mean (μ), standard deviation (σ), and coefficient of variation (C_V = σ/μ) for each metric reveal minimal variation across cycles and devices, which strongly supports the uniformity and reproducibility of our device performance.

Specifically, the I_{ON} / I_{OFF} ratio reached ~10^7, with I_{OFF} values in the range of 10^{-13}–10^{-12}A, I_{ON} ~10^{-7} A, and MW ~10 V across all devices and cycles. These results demonstrate excellent switching performance and electrical stability of the FeFETs.

Taken together, the structural characterizations and comprehensive D2D and C2C statistical analysis confirm the uniformity, robustness, and reproducibility of our MFMIS FeFET devices, thereby substantiating the reliability of both the electrical and optoelectronic characteristics presented in the main manuscript.

The D2D and C2C analysis described above has also been explicitly included in **Supplementary Note S2**, corresponding to **Fig. S10**–**S13**.

Corresponding change:

Page: 4, 5, 8

Figure: Fig. 1c, Fig. S10-S13, Supplementary Note S2

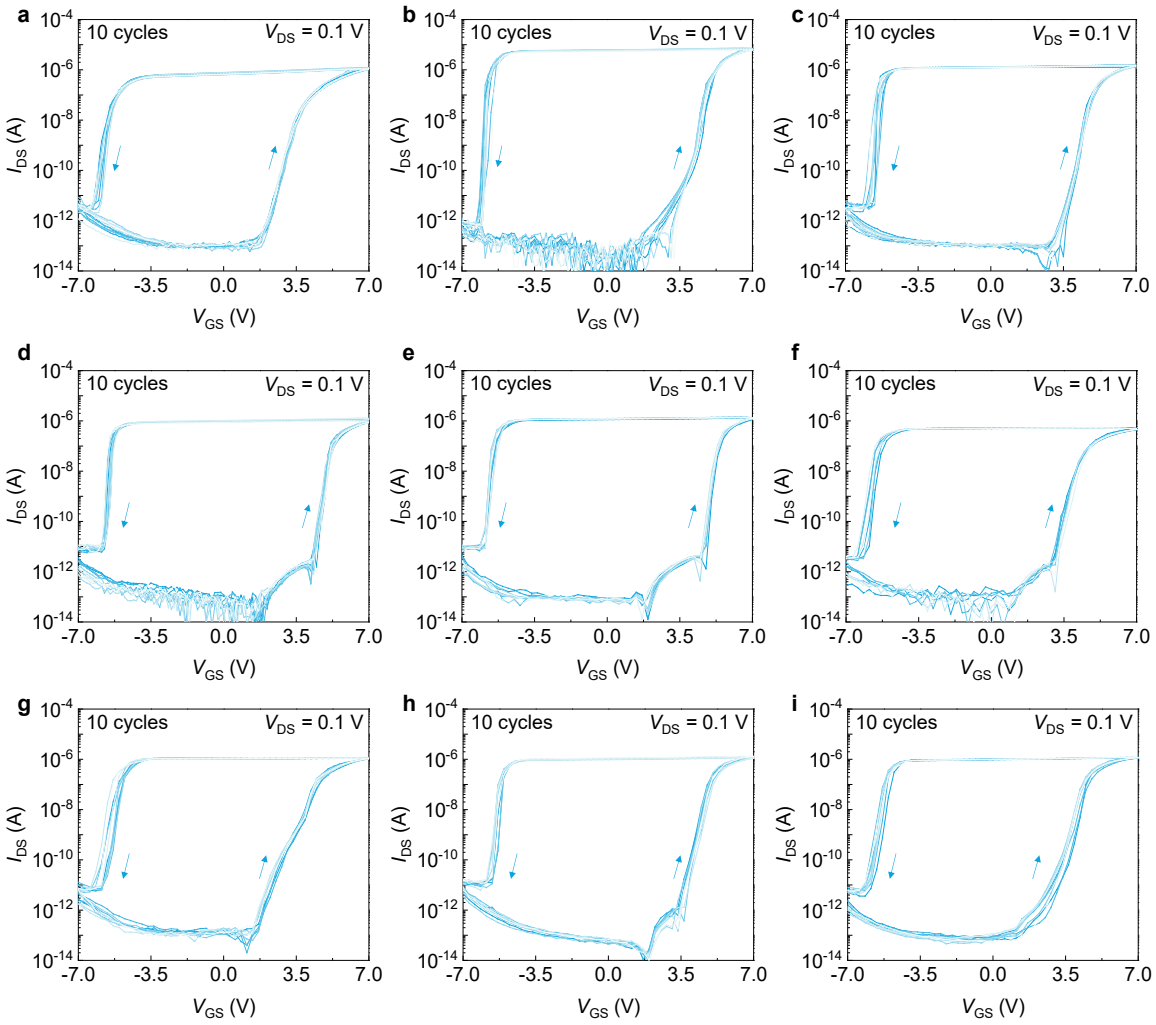


Fig. S10 I_{DS}-V_{GS} characteristics of nine individual FeFET devices (D1-D9, labeled a-i), each measured over ten consecutive cycles with V_{GS} swept from -7.0 V to 7.0 V at V_{DS} = 0.1 V. The data enable evaluation of device-to-device (D2D) and cycle-to-cycle (C2C) variations in transfer characteristics.

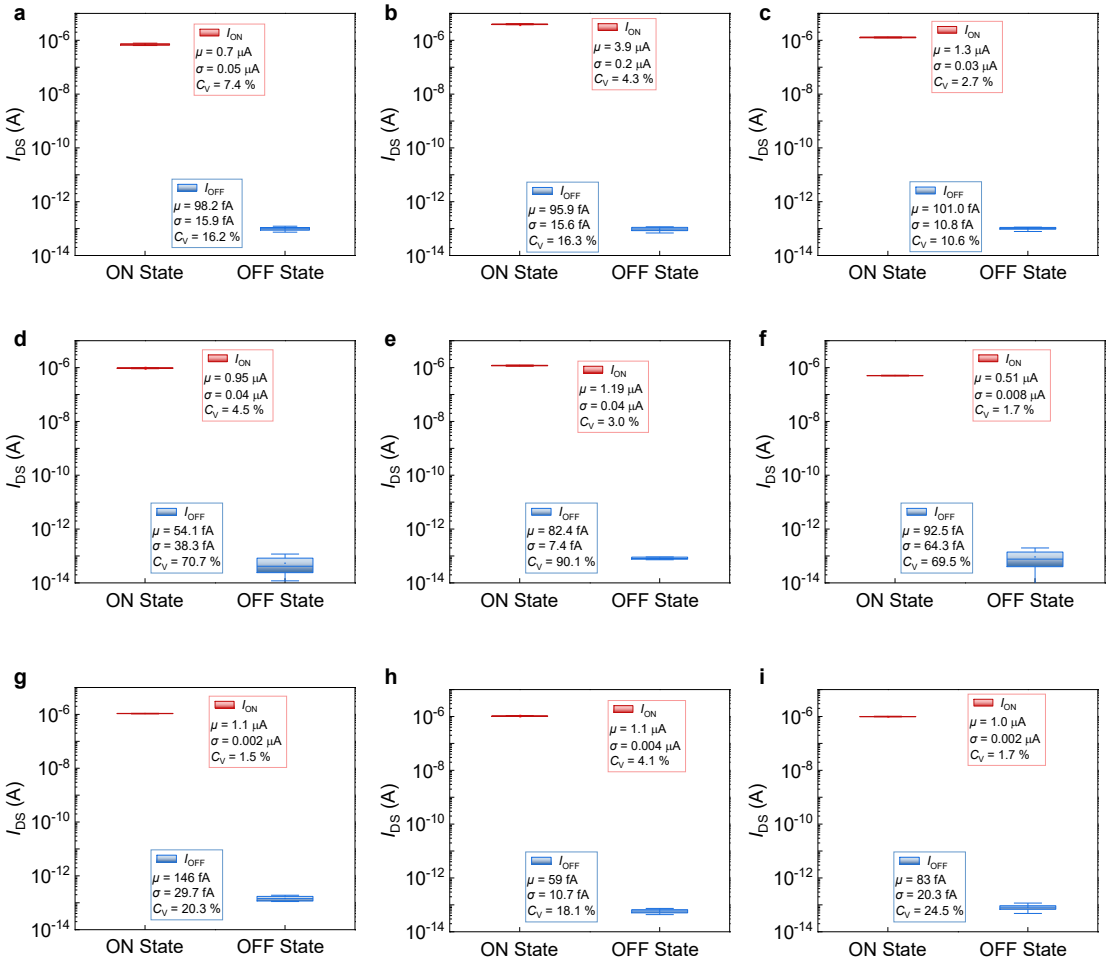


Fig. S11 Statistical distribution of I_{ON} and I_{OFF} extracted at $V_{GS} = 0$ V over ten consecutive cycles for nine FeFET devices (D1–D9). For each device, the average (μ), standard deviation (σ), and coefficient of variation (C_V) quantify C2C stability and D2D variability.

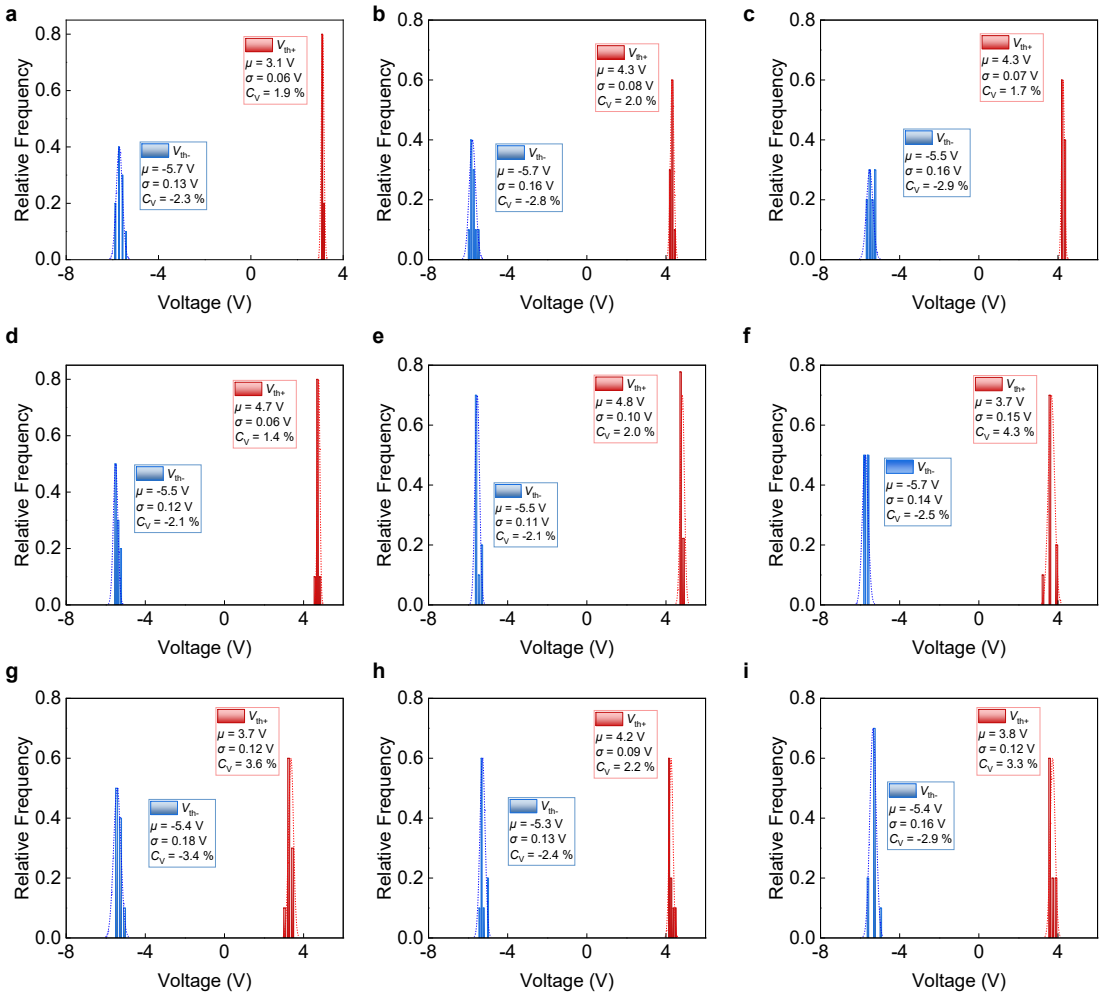


Fig. S12 Statistical distribution of positive (V_{th+}) and negative (V_{th-}) threshold voltages extracted at I_{DS} = 1 nA over ten cycles for nine FeFET devices (D1–D9). Mean (μ), standard deviation (σ), and coefficient of variation (C_V) are used to assess C2C and D2D variability.

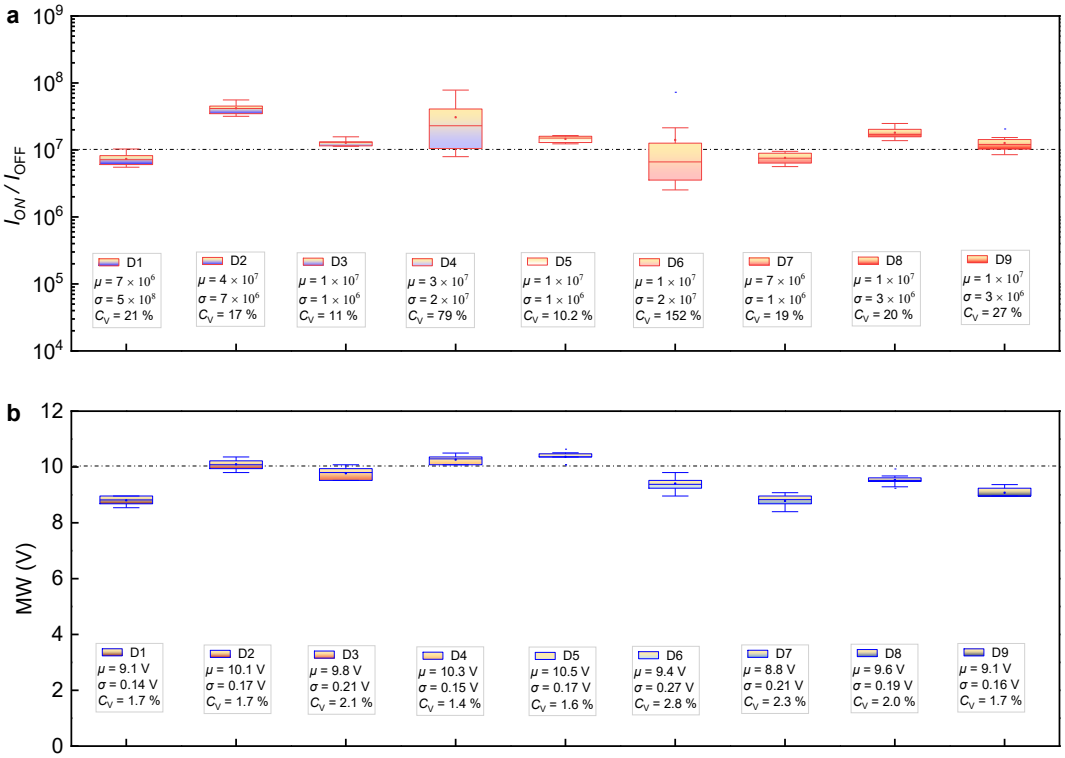


Fig. S13 a. Statistical distribution of I_{ON} / I_{OFF} ratio and **b.** memory window (MW) over ten cycles for nine FeFET devices (D1–D9), with mean (μ), standard deviation (σ), and coefficient of variation (C_V) reflecting both C2C and D2D variability.

Comment #2

2. While the authors utilize ReS_2 as the channel material in the FeFET, the manuscript does not provide a compelling justification for this choice over more extensively studied 2D semiconductors such as MoS_2 or WS_2, which often demonstrate superior optoelectronic performance.

Our response:

We thank the reviewer for the insightful suggestion regarding the rationale for selecting ReS_2 as the channel material. Following the reviewer's recommendation, we conducted a comparative study using MoS_2- and WS_2-based FeFETs fabricated with the same MFMIS structure as the ReS_2 device. As shown in **Fig. S26**, all devices exhibit similar transfer characteristics and large memory

windows, confirming that the MFMIS architecture is broadly compatible with different 2D semiconductors and reliably supports non-volatile memory operation.

However, it is in the optical domain that ReS_2 reveals a distinct advantage. Unlike MoS_2 or WS_2, which possess symmetric hexagonal lattices and exhibit isotropic optical behavior, ReS_2 has a distorted 1T' crystal structure that introduces strong in-plane anisotropy. This structural feature gives rise to a pronounced polarization-sensitive photoresponse, which is a central requirement for the development of directionally selective neuromorphic vision systems targeted in this work.

ReS_2 possesses a distorted 1T' crystal structure featuring zigzag rhenium chains aligned along the *b*-axis. This structural arrangement breaks the in-plane symmetry, resulting in pronounced anisotropy in both optical absorption and electrical transport. In contrast, MoS_2 has a symmetric hexagonal lattice, which yields largely isotropic behavior. This fundamental structural difference underlies the contrasting polarization-dependent photoresponses of the two materials.

As shown in **Fig. S27**, the photocurrent response of ReS_2 under linearly polarized light exhibits a strong angular dependence, with the signal oscillating significantly as the polarization angle is varied in 20° increments. Maxima are observed when the polarization is aligned along the *b*-axis, and minima appear along the orthogonal *a*-axis. This demonstrates the intrinsic polarization sensitivity of ReS_2. **Fig. S27b** further illustrates the crystal structure of ReS_2, where the distorted lattice and zigzag Re chains are the structural origin of this optical anisotropy.

By comparison, MoS_2 displays negligible variation in photocurrent under identical polarization modulation conditions (**Fig. S27c**), confirming its isotropic optical response. The symmetric hexagonal lattice of MoS_2 (**Fig. S27d**) lacks the in-plane anisotropy necessary for polarization sensitivity. These results directly highlight the structural origins of ReS_2's angular photoresponse, distinguishing it from conventional TMDCs such as MoS_2.

Layered ReS_2 exhibits strong in-plane anisotropy due to its distorted 1T' Re-chain structure, enabling anisotropic nonvolatile memory behavior. As illustrated in **Fig. 4g**, this polarization-sensitive response mimics polarization vision in insects like bees, which use polarized light for navigation. Such biomimetic capability highlights the potential of ReS_2-based synaptic devices in energy-efficient, directionally selective neuromorphic vision systems. The full angular dependence of the photocurrent response under linearly polarized light is shown in **Fig. S28**, which demonstrates a periodic modulation of current amplitude with polarization angle. As illustrated in **Fig. 4h**, photocurrent evolution under pulsed light excitation along the crystallographic *a*- and *b*-axes reveals a much stronger response along the *b*-axis, clearly reflecting the in-plane anisotropy. This enables encoding of direction-specific optical stimuli into synaptic weights, offering a neuromorphic mechanism for polarization-resolved learning.

To further evaluate the joint influence of polarization angle and pulse duration on the optoelectronic synaptic behavior, a 3D surface map was constructed (**Fig. 4i**), showing the channel current enhancement as a function of both parameters. The data reveal that both the polarization direction and the optical pulse width contribute to the overall photocurrent amplitude. Specifically, longer pulse durations lead to increased current enhancement, while the polarization angle governs the periodic angular dependence, with maximum response aligned along the crystal's *b*-axis. This demonstrates a coupled modulation mechanism, where excitation intensity and directionality collectively shape the synaptic output.

Inspired by this property, we simulated a polarization-resolved optical sensing task in a realistic environment. When light transitions between two media, such as air and water, partial reflection and refraction occur. At a specific angle known as the Brewster angle, the reflected light becomes fully polarized, containing only the polarization component parallel to the incident plane. In **Fig. 4j**, we apply this principle to demonstrate polarization-selective imaging using our ReS_2-based FeFET. Electrical output patterns were simulated under linear polarization aligned at 0° and 90° relative to the ReS_2 *b*-axis. The 90° frame highlights underwater contours by filtering out surface reflections, while the 0° frame captures reflected sky patterns and glare. The contrast between these polarization-resolved images enables superior feature discrimination, mimicking polarization demultiplexing strategies used by certain insects. These results demonstrate the potential of ReS_2 synapses as low-power, directionally selective components in neuromorphic systems and bio-inspired polarization imaging applications.

The above justification for the selection of ReS_2 and its intrinsic advantages is supported by the experimental and simulation results presented in the main manuscript (**Fig. 4g–j**) and supplementary information **(Fig. S26–S28)**, which collectively demonstrates its polarization-sensitive behavior and relevance for neuromorphic optoelectronic applications. To underscore the innovation and motivation for selecting ReS_2, its anisotropic characteristics are additionally emphasized in the Abstract, Introduction, and Discussion.

Corresponding change:

Page: 1, 2, 3, 15-17, S-28, S-29

Figure: Fig. 4g-j, Fig. S26-S28

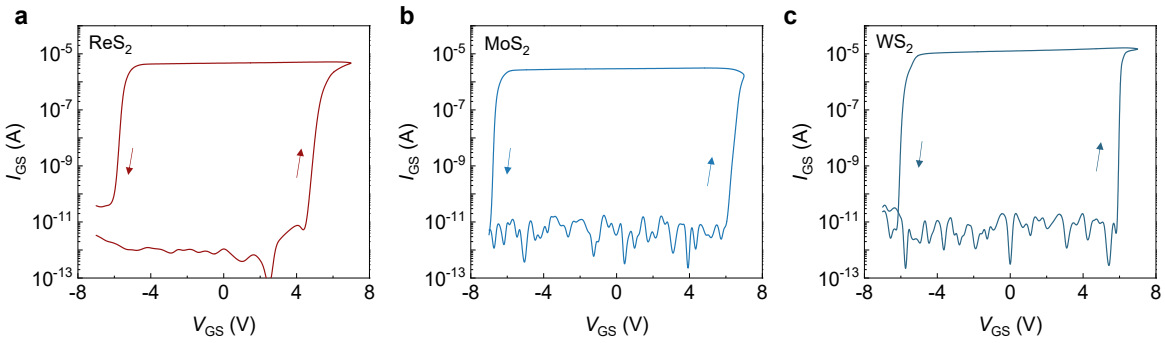


Fig. S26 I_{DS}–V_{GS} characteristics of MFMIS FeFETs based on different 2D channel materials: **a.** ReS_2, **b.** MoS_2, and **c.** WS_2. All devices were measured at V_{DS} = 0.1 V. Each device exhibits a counterclockwise hysteresis loop, confirming reliable ferroelectric switching.

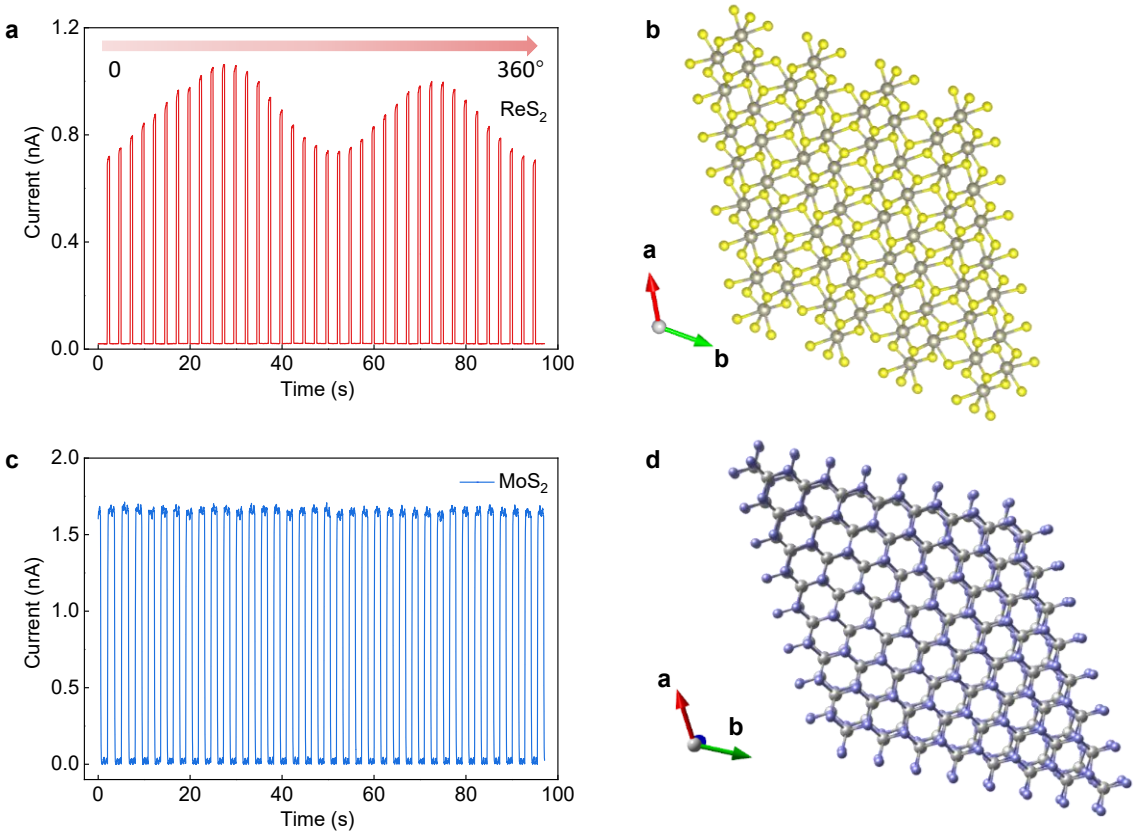


Fig. S27 Comparison of polarization-dependent photoresponse between anisotropic ReS_2 and isotropic MoS_2. a. Polarization-resolved photocurrent of ReS_2 measured under linearly polarized light with 20° step increments, exhibiting significant oscillation with maxima along the *b*-axis and minima along the orthogonal *a*-axis, indicating strong angular dependence. **b.** Crystal structure of ReS_2 with a distorted 1T' lattice and zigzag Re chains, which break in-plane symmetry and result in

polarization-sensitive optical behavior. **c.** Photocurrent response of MoS_2 under identical polarization modulation conditions, exhibiting minimal angular variation, consistent with its isotropic optical response. **d.** Symmetric hexagonal lattice of MoS_2, lacking in-plane anisotropy, which accounts for its polarization-insensitive optical characteristics. These results highlight the intrinsic structural origin of angular sensitivity in ReS_2, in contrast to the isotropic behavior observed in conventional TMDCs such as MoS_2.

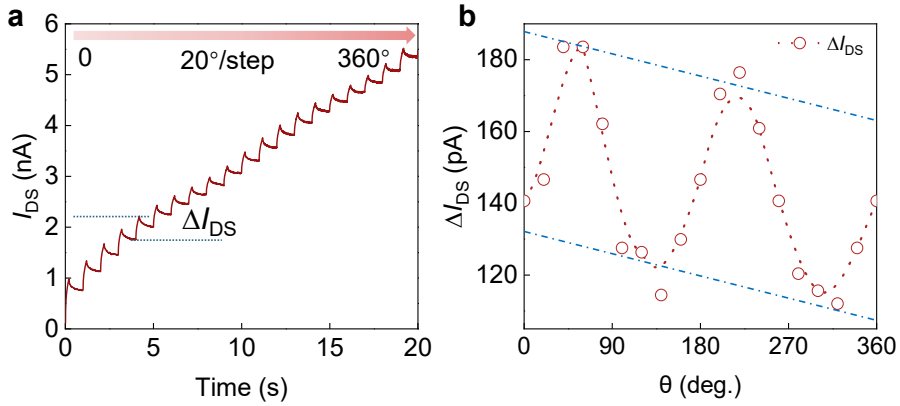


Fig. S28 Polarization-dependent modulation of photocurrent in the FeFET. a. Angular-resolved measurement of photo-induced current enhancement ($\Delta I_{DS} = I_{DS2} - I_{DS1}$) as a function of incident light polarization angle, scanned from 0° to 360° in 20° steps. The observed variation reflects the anisotropic optical response of ReS_2. **b.** Polar plot of ΔI_{DS} values extracted at each polarization angle, revealing the symmetry and magnitude of photocurrent amplification with respect to crystal orientation. This anisotropic enhancement underscores the polarization-sensitive nature of the device's optoelectronic behavior.

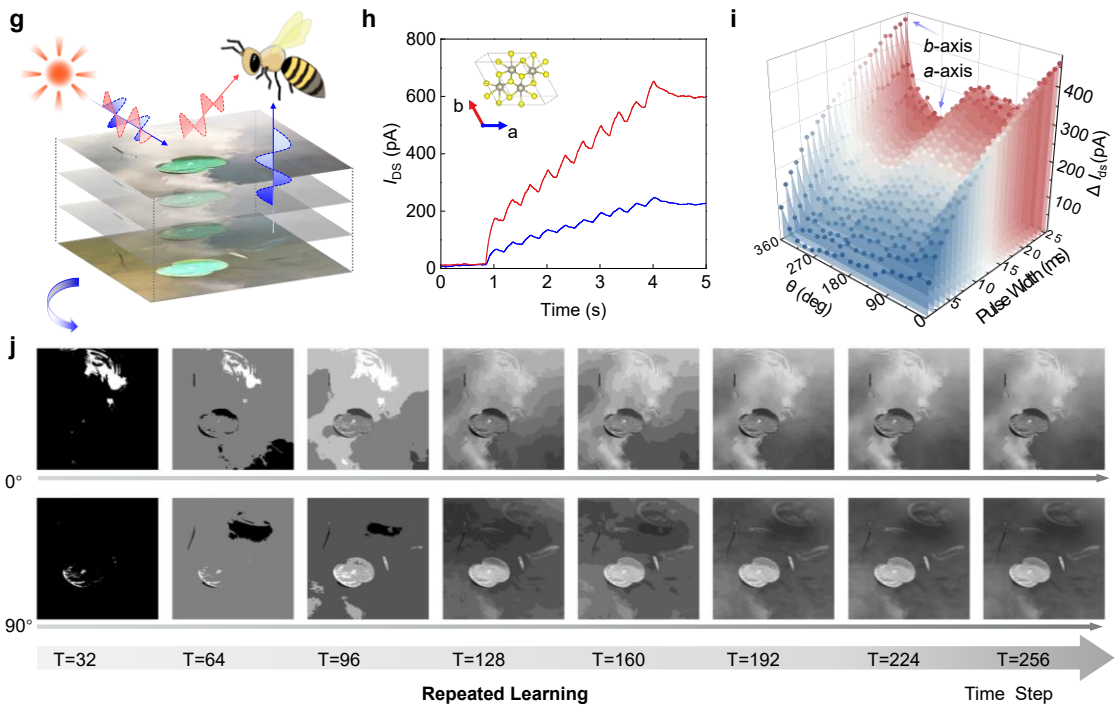


Fig. 4 g. Schematic illustration of polarization-sensitive vision for distinguishing surface reflections and subsurface objects. **h.** Photocurrent evolution under optical programming along the crystallographic *a*- and *b*-axes of ReS_2. A significantly higher response is observed along the *b*-axis, reflecting its intrinsic in-plane anisotropy. Inset: Crystal structure of ReS_2. **i.** 3D surface plot showing the optically induced channel current enhancement as a function of polarization angle and light pulse width. **j.** Time-sequenced images under linear polarization at 0° (top) and 90° (bottom) relative to the ReS_2 *b*-axis reveal the ability to distinctly distinguish surface and underwater features, respectively.

Comment #3

3. The optical micrograph shown in Figure 1C lacks a scale bar, making it difficult to assess the physical dimensions of the device and limiting its utility for replication or comparative analysis.

Our response:

We appreciate the reviewer's helpful comment. You're correct that including a scale bar in the optical micrograph of **Fig. 1c** is essential for clarity, reproducibility, and scientific rigor. Scale bars

provide a crucial reference for estimating feature sizes and enable others to replicate device dimensions with confidence.

Accordingly, we have added a clearly labeled scale bar to **Fig. 1c** in the revised manuscript. This update enhances the figure's utility for accurate dimensional analysis and strengthens its suitability for comparative and replication studies.

Corresponding change:

Page: 5

Figure: Fig. 1c

Comment #4

4. In Figure S4e, a leakage current of approximately 10 nA is reported, which is relatively high and does not support the classification of the device as exhibiting "low leakage" for FeFET applications. Additionally, the actual area of the MIM capacitor used for leakage testing is not specified, preventing accurate calculation of current density and hindering meaningful comparison with existing literature.

Our response:

We thank the reviewer for the thoughtful and constructive comments. We would like to clarify that the ~10 nA leakage current shown in **Fig. S4e** corresponds to a standalone metal–ferroelectric–metal (MFM) capacitor, which is not part of the FeFET structure. This capacitor was deliberately fabricated with a relatively large area (100 μm × 100 μm) to assess the intrinsic ferroelectric properties and leakage behavior of the HZO layer deposited by ALD. Such test structures are used as process control monitors to evaluate material quality before device integration. We have now explicitly stated the capacitor area in the revised supplementary information to avoid potential confusion.

In contrast, the FeFET devices discussed in the main text have a much smaller effective gate area of approximately 1.5 μm × 1.5 μm. As a result, the actual gate leakage current during operation is significantly lower, as clearly shown in **Fig. S5**, where the I_{GS}–V_{GS} characteristics over 100 consecutive cycles demonstrate stable and consistently low gate current, confirming excellent gate insulation and leakage performance under repeated switching.

*To clarify this point, the following sentence has been added to the main text: "The corresponding gate leakage current over 100 cycles (**Fig. S5**) confirms robust gate insulation during repeated switching."*

We hope this clarification resolves the misunderstanding and reinforces the reliability of the low-leakage behavior of our FeFET devices under practical operating conditions.

Corresponding change:

Page: 7, S-4

Figure: Fig. S5

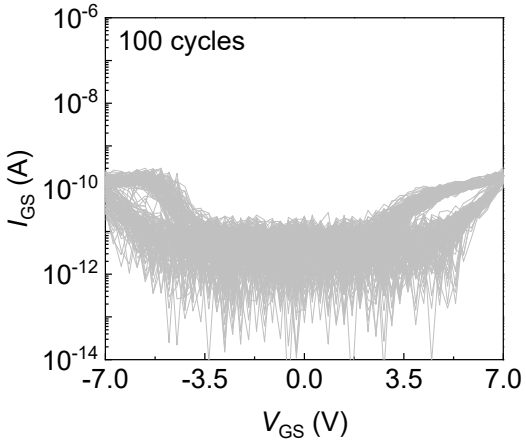


Fig. S5 Gate leakage current (I_{GS}–V_{GS}) characteristics measured over 100 consecutive cycles under bidirectional gate voltage sweeps from –7 V to 7 V. The consistently low leakage current confirms the excellent gate insulation and stability of the device during repeated electrical operation.

Comment #5

5. Although Figure 2i demonstrates excellent electrical endurance over 10^5 cycles, the manuscript does not include endurance data for repeated optical programming. Such data are crucial for evaluating the long-term reliability of optically induced nonvolatile states in neuromorphic applications.

Our response:

We appreciate the reviewer's insightful comment regarding the need for endurance data under repeated optical programming, which is indeed critical for assessing the long-term reliability of

nonvolatile states in neuromorphic applications. To address this, we have performed extended endurance testing that involves 10^5 consecutive cycles of optical programming followed by electrical erasure, as now presented in **Fig. 4f**.

In each cycle, the device is programmed by an optical pulse and then reset using an electrical erase pulse. During this process, the change in drain current was continuously monitored to evaluate the integrity and retention of the memory states. The measured ΔI_{DS} remains consistently stable throughout the entire 10^5-cycle sequence, with clearly distinguishable high and low states and no significant deterioration in signal amplitude or state separation.

These results demonstrate that the memory window remains well-preserved across repeated optical stimuli, with no apparent fatigue or degradation of the ferroelectric switching or channel conduction. Such performance indicates excellent operational robustness of the FeFET under hybrid optical-electrical cycling, which is particularly important for neuromorphic systems that rely on frequent optical input.

*The following sentence has been added to the manuscript: "The device also demonstrates stable endurance, as shown in **Fig. 4f**. Under repeated cycles of optical programming and electrical erasing, a stable memory window and high contrast between conductance states were maintained over 10^5 cycles, confirming the robustness of the optoelectronic synaptic scheme for non-volatile memory applications."*

Together with the electrical endurance data provided in **Fig. 2i**, this optical cycling endurance highlights the dual-mode programmability of our FeFET devices and confirms their long-term stability, reliability, and suitability for advanced photoferroelectric and neuromorphic applications that require high-cycle, low-power, optically addressable memory elements.

Corresponding change:

Page: 15

Figure: Fig. 4f

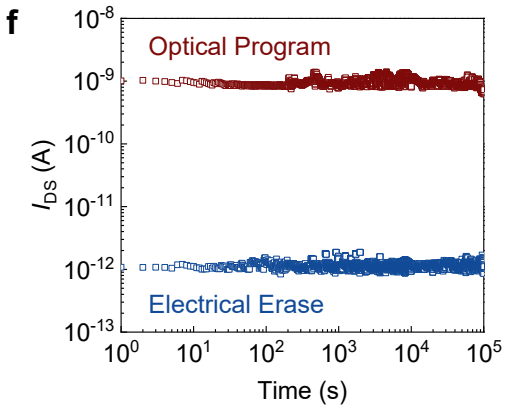


Fig.4 f. Optical programming combined with electrical erasure demonstrates remarkable endurance over 10^5 cycles. Each cycle consists of an optical program pulse followed by electrical erase, and the resulting change of I_{DS} remains consistently distinct between high and low states throughout repeated operations. This stable memory window and reliable current-state separation after 10^5 cycles highlight the device's exceptional robustness and suitability for long-term non-volatile memory applications.

Comment #6

6. In Figure 2e, the LTP curves corresponding to 500 µs and 1 ms pulse widths display significant nonlinearity, which appears inconsistent with the manuscript's claim of linear conductance modulation.

Our response:

We thank the reviewer for this valuable observation. We agree that under longer pulse durations (500 µs and 1 ms), the LTP curves exhibit noticeable nonlinearity, which was not sufficiently acknowledged in the original manuscript. In response, we have revised the relevant sentence in the main text (now **Fig. 2g**) to clarify that linear conductance modulation is primarily observed under shorter pulse widths (50–200 µs), while longer pulses lead to degraded linearity. This degradation is likely caused by accelerated charge accumulation and partial saturation of trap states in the floating gate, which reduces the incremental conductance change per pulse. The corresponding fitting results are provided in **Fig. S14**. This revision ensures a more accurate interpretation of the data and better aligns the discussion with the experimental observations.

To enhance clarity, we have added the following explanatory sentence to the revised manuscript (page 8, line 192):

"Long-term potentiation (LTP), induced by identical +5 V gate pulses with varying pulse widths (50 μs to 1 ms), results in gradual conductance modulation with reasonably linear trends under shorter pulses (50–200 μs), as shown in ***Fig. 2g****. However, under longer pulse widths (500 μs and 1 ms), the linearity of conductance updates diminishes, which may be attributed to accelerated charge accumulation or partial saturation of trap states in the FG, limiting the incremental conductance change per pulse. Nevertheless, the conductance evolution remains monotonic and stable, enabling controllable synaptic weight tuning for neuromorphic learning applications. The corresponding fitting results are provided in* ***Fig. S14****."*

Corresponding change:

Page: 10, S-15

Figure: Fig. 2g, Fig. S14

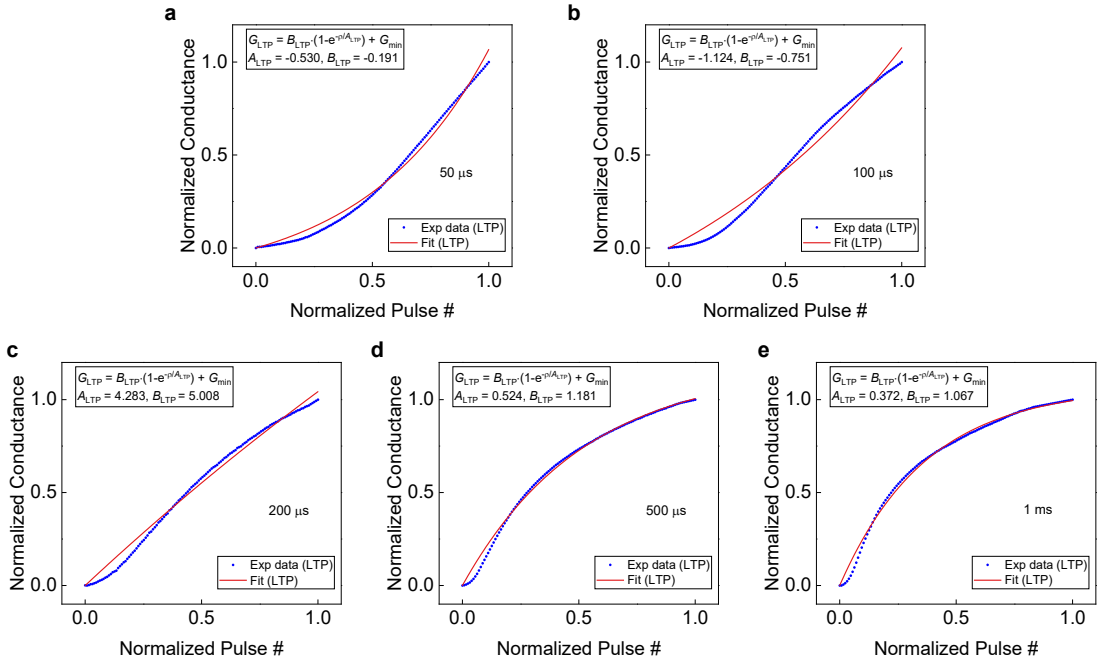


Fig. S14 Experimental and fitted results of long-term potentiation (LTP) behavior under gate pulses with a fixed amplitude of 5 V and varying pulse widths. **a**–**e** correspond to pulse widths of 50 μs, 100 μs, 200 μs, 500 μs, and 1 ms, respectively. The conductance evolution is fitted using the empirical model: $G_{LTP} = B_{LTP}\left(1 - e^{-\rho/A_{LTP}}\right) + G_{min}$, where p is the pulse number, and A_{LTP}, B_{LTP}, and G_{min} are fitting parameters.

Comment #7

7. The reported energy consumption per synaptic event (3.18 pJ) seems low; however, it is calculated using a 0.5 s light pulse-substantially longer than the typical spike durations (<1 ms) used in neuromorphic systems. Given the device's fast optical response time (<100 μs), it is reasonable to expect that a shorter pulse would result in even lower energy consumption, which should be discussed.

Our response:

We sincerely thank the reviewer for this valuable comment regarding the energy consumption calculation. In our initial analysis, the reported energy value of 3.18 pJ was derived from using a 0.5 s light pulse, which significantly overestimates the energy required for a typical synaptic event, especially considering that spike durations in neuromorphic computing are usually below 1 ms.

To address this, we have re-evaluated the energy consumption using data shown in **Fig. S25**, where we systematically measured the photocurrent response under optical pulses with widths ranging from 200 μs to 1 s and incident light powers of 6.36 pW, 31.8 pW, 63.69 pW, 318.45 pW, and 636.9 pW. We found that reliable photocurrent generation begins at a pulse width of 200 μs. Under the most energy-efficient condition, a 200 μs pulse with 6.36 pW incident light power produces a measurable photocurrent of approximately 0.2 μA, leading to a recalculated optical programming energy of:

$$E_{\text{programming}} = P_{\text{spike}} \times A_{\text{active}} \times T_{\text{duration}} = 6.36\ \text{pW} \times 100\ \mu\text{m}^2 \times 200\ \mu\text{s} \approx 1.27\ \text{fJ}$$

In addition, the electrical erase step consumes only about 0.7 fJ, based on a gate leakage current of 1 pA under a gate voltage of -7 V for 100 μs. The total energy per synaptic event, combining both optical programming and electrical erasing, is therefore estimated to be approximately 2.0 fJ.

A clarification on energy consumption has been added to the manuscript: The energy consumption per synaptic event in the MFMIS FeFET is determined by the optical programming and electrical erasing. As shown in ***Fig. S25****, photoresponse measurements were conducted under varying illumination power (6.36□636.9 pW) and pulse widths (200 μs–1 s), revealing the dependence on illumination parameters. Based on the measured photocurrent and input power, the optical programming energy was estimated to be ~1.3 fJ (6.39 pW, 200 μs), while electrical erasing consumed ~0.7 fJ, yielding a total of ~2.0 fJ per synaptic operation. The methodology and calculations are detailed in* ***Supplementary Note S4***[49]*.*

Additionally, **Fig. S22** presents the device's frequency-dependent photoresponse under repeated illumination from 1 Hz to 1 kHz, further confirming its adaptability to rapid optical stimulation and compatibility with high-speed synaptic operations.

This refined calculation confirms that our device operates with ultralow energy consumption, suitable for neuromorphic computing. We have revised the main text accordingly and provided a detailed analysis in **Supplementary Note S4**.

Corresponding change:

Page: 15, S-26, S-27

Figure: Fig. S22, Fig. S25, Supplementary Note S4

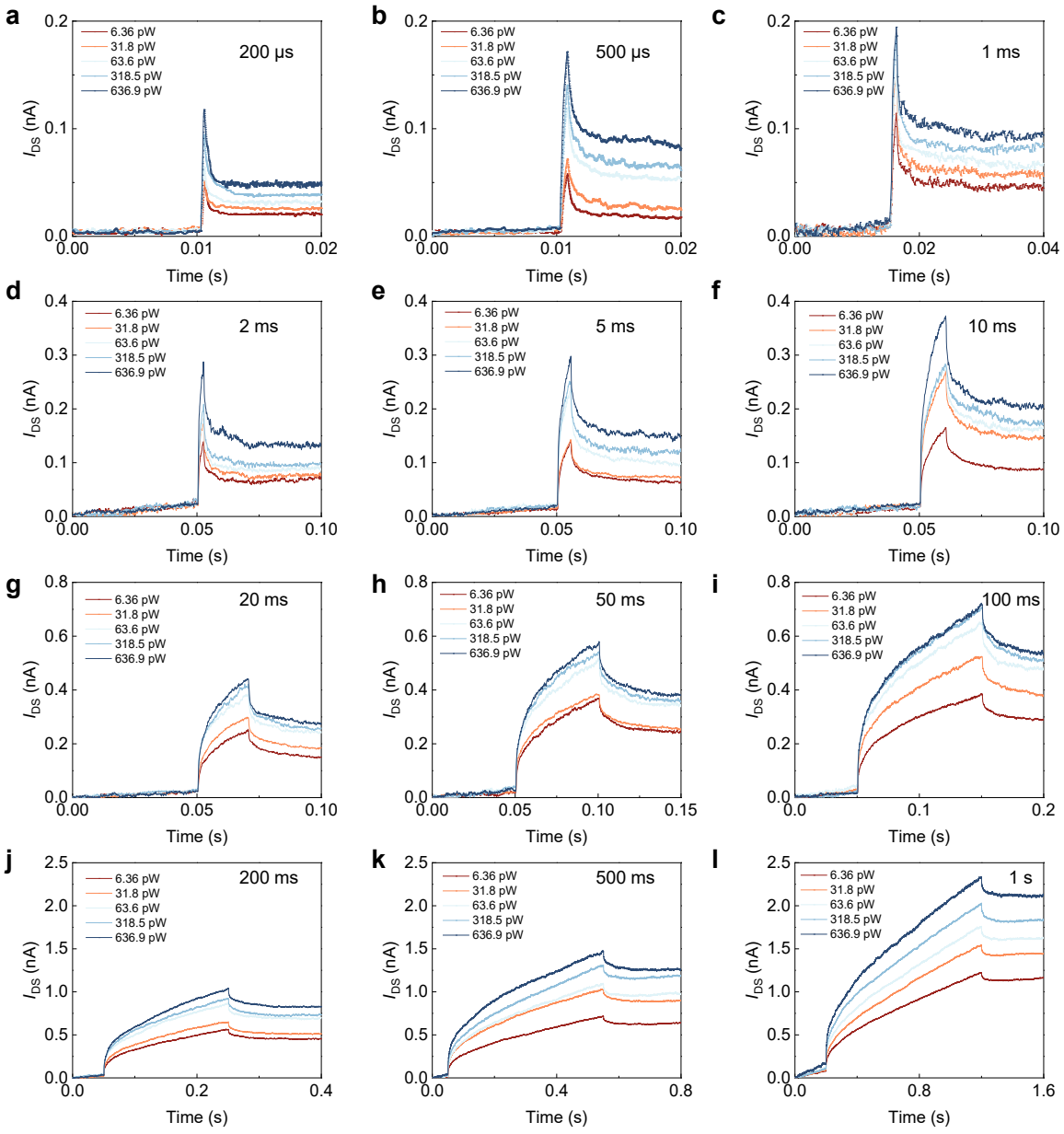


Fig. S25 Photoresponse current of the FeFET device under varying light intensity and pulse duration. **a-l**. The optical response was measured at pulse widths ranging from 200 µs to 1 s, with each subplot corresponding to a different duration. Within each condition, the device was exposed to light powers of 6.36 pW, 31.8 pW, 63.69 pW, 318.45 pW, and 636.9 pW. The results reveal how both light intensity and exposure time modulate the photocurrent, enabling a comprehensive evaluation of the device's photoresponse characteristics.

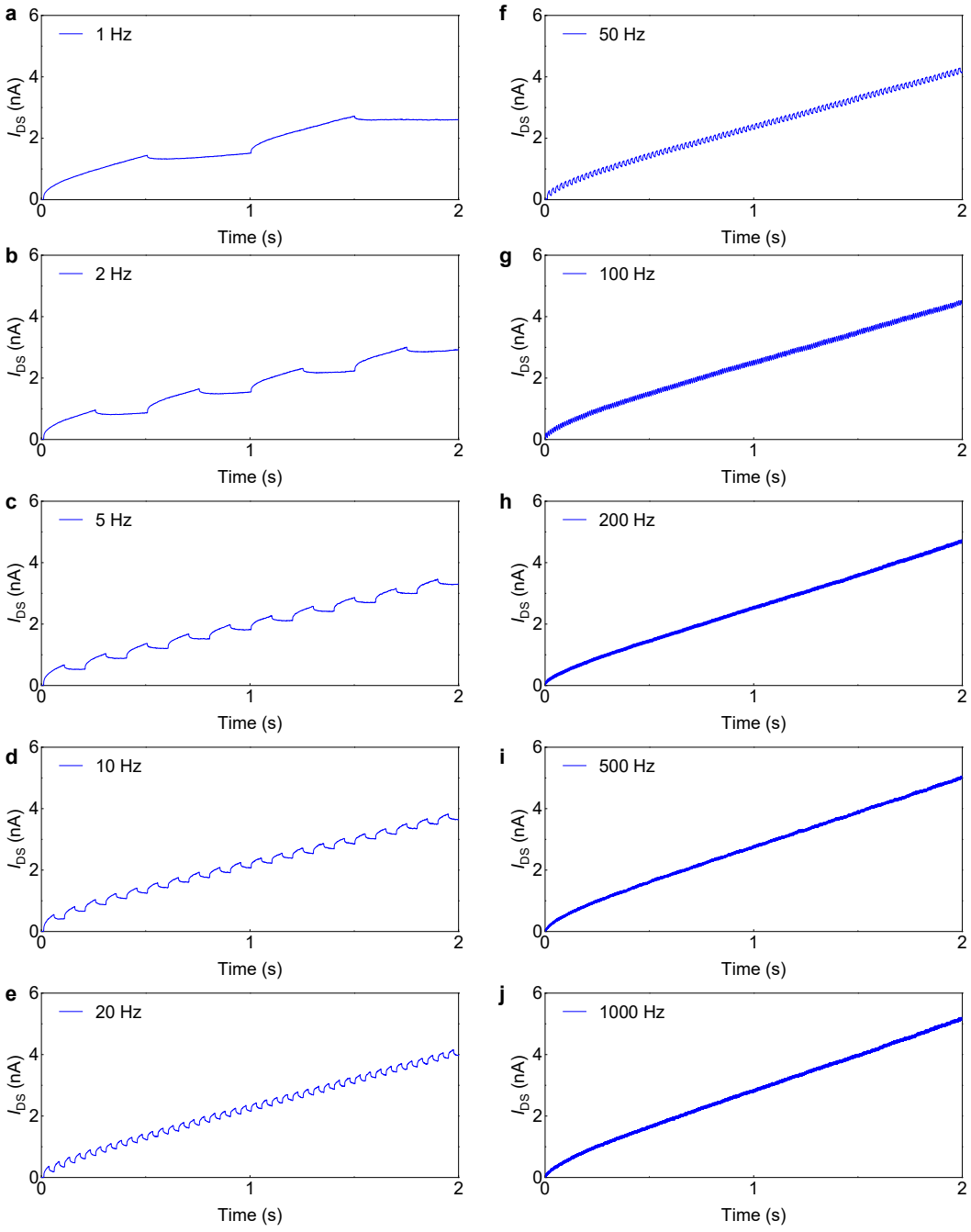


Fig. S22 Frequency-dependent optical response of the FeFET device. **a**–**j** Photocurrent responses recorded under continuous illumination at modulation frequencies ranging from 1 Hz to 1 kHz. For each frequency, the device was exposed to repeated optical on/off cycles, and the corresponding photoresponse current was measured. As the frequency increases, shorter intervals between pulses lead to enhanced temporal summation and stronger EPSC responses. This systematic evaluation highlights the device's dynamic adaptability and confirms its potential for high-speed optical signal processing and neuromorphic computing applications.

Reviewer #3

The main contents of this work can be summarized as following: (1) constructing the HZO floating gate based FeFET for non-volatile memory and suppressing dark currents of the ReS_2 photodetector (DOI: 10.1109/TED.2024.3386508; DOI: 10.1109/TED.2024.3371945; https://onlinelibrary.wiley.com/doi/full/10.1002/smll.202311630); (2) using synergetic photoelectric/electric modulation to generate synaptic plasticity to provide weight values for ANN computation (https://pubs.acs.org/doi/full/10.1021/acsnano.4c11898;https://onlinelibrary.wiley.com/doi/full/10.1002/smll.202311630).

There is a great deal of this kind of work. Therefore, the referee considered that this work has not shown sufficient differences from others and be lack of novelty.

Our response:

We appreciate the reviewer's summary and acknowledge the significant progress made in both silicon-based FeFET memory and ReS_2-based optoelectronic synaptic devices. Prior works have demonstrated excellent ferroelectric switching behavior using HZO in MFS and MFIS structures on silicon substrates, as well as strong light–matter interaction and polarization-sensitive photoresponse in two-dimensional materials such as ReS_2. The references provided by the reviewer span four representative device categories, including Si-based MFS FeFETs, Si-based MFIS FeFETs, ReS_2 devices based on charge trapping mechanisms, and ReS_2 devices incorporating graphene-based floating gates. Together, these studies offer a comprehensive foundation for evaluating current advances in ferroelectric memory and optoelectronic modulation. A detailed examination and comparison with these representative works is both necessary and valuable, as it clearly highlights the distinctive architecture, operation mechanism, and multifunctionality of our device.

Building on these advances, our work strategically integrates the strengths of both domains by combining the robust ferroelectric control of HZO with the optical sensitivity of ReS_2 in a CMOS-compatible MFMIS architecture. Critically, we introduce a floating gate (FG) between the HZO and ReS_2 layers to functionally decouple ferroelectric switching and photocarrier dynamics, enabling independent and stable electrical and optical programming. This unified design supports non-volatile electrical memory, optical programming, low-noise photodetection, and neuromorphic plasticity within a single scalable device, thereby offering a comprehensive solution that extends beyond the capabilities of previously reported systems.

To further clarify the distinctions and technical advantages of our approach, we provide a point-by-point comparison with the works cited by the reviewer in the sections below.

1) Floating Gate Integration in MFMIS Structure: Structural and Mechanistic Innovation

Our device leverages a MFMIS architecture, in which an FG is strategically introduced between the HZO ferroelectric layer and the ReS_2 channel. This structural innovation introduces a fundamentally different operating mechanism, enabling decoupled electrical and optical programming with enhanced non-volatile memory performance and long-term stability.

The FG significantly enhances the electrical memory characteristics of the device by improving both ferroelectric switching efficiency and polarization stability. By modulating the capacitive coupling and controlling the area ratio between the ferroelectric layer and the semiconductor channel, the FG increases the effective voltage drop across the HZO layer, thereby promoting stronger and more complete polarization switching. In parallel, the FG acts as an internal screening layer that suppresses depolarization fields at the ferroelectric/semiconductor interface, reducing polarization back-switching and enhancing stability. These combined effects result in a larger and more reliable memory window, improved data retention, and robust endurance over repeated cycles.

The FG also enables stable and non-volatile optical memory. Under visible illumination, the ReS_2 channel generates photocarriers that are driven by the remanent polarization field of the HZO and transferred into the FG. Due to its capacitive isolation, the FG retains these photo-induced charges even after the illumination is removed. This process allows transient optical input to be converted into a persistent change in channel conductance, enabling reliable and rewritable optical programming. In contrast to conventional 2D optoelectronic devices, where photocarriers typically dissipate rapidly or are weakly confined at interface traps, our architecture ensures robust charge retention and stable optoelectronic memory behavior.

The FG plays a critical role in decoupling electrical erasing and optical programming. Ferroelectric switching, driven by gate voltage pulses, and photocarrier trapping, induced by light absorption in the ReS_2 channel, operate independently. This separation ensures that optical programming can be reliably carried out after electrical erasing, without interference from the ferroelectric state. The remanent polarization field of the HZO layer further facilitates photocarrier injection into the FG, enabling cooperative modulation when both stimuli are applied. This combination of independent control and stimulus-responsive interaction supports reliable multi-modal memory functionality.

In addition, with a stable and well-controlled electrical foundation, the anisotropic optical properties of the ReS_2 channel, particularly its polarization sensitivity, can be fully exploited. The absence of electrical interference allows the intrinsic angular dependence of the photoresponse to emerge clearly, thereby enabling accurate and reproducible polarization-resolved optoelectronic measurements.

Finally, except for the ReS_2 transfer step, all fabrication processes, including ALD, photolithography, etching, and metallization, are fully compatible with CMOS technology. This ensures good reproducibility, scalability, and potential for future large-scale integration.

2) Superior Electrical and Optoelectronic Performance Enabled by FE–FG Coupling

Our device demonstrates a unique combination of high-performance electrical memory and optical sensing within a single ReS_2-based FeFET, surpassing prior benchmarks in both domains. Electrically, the introduction of the floating gate leads to an ultralow I_{OFF} (~100 fA), a high I_{ON} / I_{OFF} ratio of 10^7, and a wide memory window of 10.5 V with a sharp switching ratio of 75%. These results represent significant improvements over conventional MFIS FeFETs on Si substrates, which typically suffer from elevated leakage currents. Optically, the device achieves a responsivity of 4×10^5 A/W and a specific detectivity of 1.9×10^{14} Jones under visible illumination, indicating high light sensitivity and low intrinsic noise. In addition to detection, the device also supports non-volatile optical memory, which arises from the effective retention of photogenerated charges in the floating gate, enabled by ferroelectric-assisted injection. Unlike previously reported charge trapping mechanisms or graphene-based floating gate designs, our approach leverages a stable ferroelectric field to enable reliable and non-volatile optical programming.

3) Unified Functional Platform for Polarization-Sensitive Optoelectronic Neuromorphic Applications

Our device offers an application-oriented integration of multiple core functions, including ferroelectric control, optical sensing, non-volatile optical memory, and polarization sensitivity, all within a single FeFET. This compact multifunctional platform enables advanced processing capabilities in optoelectronic neuromorphic systems.

Building on these features, we demonstrate practical applications such as polarization-resolved imaging, where the device distinguishes structural features under polarized light based on angularly dependent photocurrent. We also implement optoelectronic artificial neural networks using the same FeFETs as optically programmable synapses for light-driven pattern recognition. These results showcase the potential of our device for compact and energy-efficient vision systems.

Compared to existing works, conventional Si-based FeFETs support only electrical memory and lack optical or polarization-resolved functionality. In contrast, previously reported ReS_2-based optical synaptic devices rely on unstable charge trapping mechanisms and lack CMOS-compatible ferroelectric control. By integrating stable ferroelectric modulation, optical memory, and polarization sensitivity within a single device, our platform provides a unique and scalable solution that unifies memory, sensing, and computing in one architecture. These unique structural and

functional innovations distinguish our approach from existing works, as detailed in the comparison table below.

Corresponding change:

Page: S-10

Figure: Table S2

Table S2. Comparison of Si-based FeFETs and ReS_2-based optoelectronic synapses.

Feature		**1**	**2**	**3**	**4**	**This work**
Structure		MFS FeFET	MFIS FeFET	ReS_2/h-BN/Gr	Back gate	**MFMIS FeFET**
Channel		Si	Si	ReS_2	ReS_2	**ReS_2**
Mechanism		Ferroelectric HZO	Ferroelectric HZO	Graphene FG	Charge trapping	**Hybrid ferroelectric HZO-FG**
Electrical performance	I_{OFF}	10 pA	10 nA	10 pA	1 pA	**100 fA**
	I_{ON}/I_{OFF}	10^6	10^2	10^5	10^6	**10^7**
	MW	0.8 V	4.79 V	80 V	80 V	**10.5 V**
	SR	0.3_1.5V	-2_4 V	-50_50 V	-80_80 V	**-7_7 V**
	Ratio	44%	79%	80%	50%	**75%**
Optical performance	***R***	-	-	-	-	**4×10^5 A/W**
	D*	-	-	-	-	**1.9×10^{14} Jones**
Functionality		Electrical memory	Electrical memory	Electro-optical synapse	Electro-optical synapse	**Integrated electro-optical memory & synapse**
Applications		-	-	Image recognition; optoelectronic CNN	Digit classification; optoelectronic ANN	**Polarization-resolved vision; optoelectronic ANN**

References:

1. Lee, H. J. et al. Laminated Ferroelectric FET With Large Memory Window and High Reliability. *IEEE Trans. Electron Devices* **71**, 2411-2416 (2024).

2. Cai, Z., Toprasertpong, K., Liu, Z., Takenaka, M. & Takagi, S. Understanding HZO Thickness Scaling in Si FeFETs: Low Operating Voltage, Fast Wake-Up, and Suppressed Charge Trapping. *IEEE Trans. Electron Devices* **71**, 3633-3639 (2024).
3. Li, W. et al. The Nonvolatile Memory and Neuromorphic Simulation of ReS_2/h-BN/Graphene Floating Gate Devices Under Photoelectrical Hybrid Modulations. *Small* **20**, 2311630 (2024).
4. Chen, Y. et al. Wrinkled Rhenium Disulfide for Anisotropic Nonvolatile Memory and Multiple Artificial Neuromorphic Synapses. *ACS Nano* **18**, 30871-30883 (2024).

Comment #1

1. The MFMIS device structure is shown in Fig 1c. Is the HZO point (left) on the same layer of the HZO layer under the channel (right)?

Our response:

Thank you for pointing this out. The HZO under the control gate (left) and beneath the channel (right) in **Fig. 1c** refer to the same continuous ferroelectric layer. This film is uniformly deposited across the entire gate stack, typically via a single-step ALD process. The left region is highlighted schematically to emphasize the polarization-switching area, but structurally, the HZO is continuous throughout. The HZO beneath the channel remains fully ferroelectrically active and plays a key role in modulating channel charge and enabling non-volatile memory behavior.

To improve clarity, we have added arrows and labels in **Fig. 1c** to explicitly indicate that both regions belong to the same HZO layer.

Revised in the manuscript:

"The HZO layer forms a continuous ferroelectric film spanning both the control gate and channel regions."

Corresponding change:

Page: 4

Figure: Fig.1c

Comment #2

2. What would be the difference between the MFMIS and MFIS devices with the same materials?

Our response:

We thank the reviewer for raising this important question regarding the differences between MFMIS and MFIS devices constructed using the same materials. To provide a direct comparison, we fabricated MFIS FeFETs under the same process conditions as the MFMIS counterparts, with the sole difference being the absence of the intermediate floating metal layer in the MFIS configuration. This enables an accurate assessment of how device performance is influenced by architectural differences, independent of material or fabrication variables.

MFIS FeFET Fabrication

The MFIS FeFETs were fabricated using the same ReS_2 channel material and identical process flow as the MFMIS devices. As illustrated in **Fig. S6**, the process involved W gate electrode deposition and patterning, ALD growth of HZO, capping and annealing for phase crystallization, deposition of a conformal HfO_2 interfacial layer, and ReS_2 transfer, followed by source/drain electrode formation. This ensured consistent ferroelectric layer quality and interface conditions between both device types.

Unstable Behavior in MFIS Devices

Despite the matched fabrication process, MFIS devices exhibited unstable switching behavior. As shown in **Fig. S7**, the I_{DS}-V_{GS} curves evolved over five consecutive programming cycles. In the first cycle (**Fig. S7a**), the device displayed a counterclockwise hysteresis loop indicative of ferroelectric-dominated switching. In the second cycle (**Fig. S7b**), the loop became narrower and showed signs of mixed ferroelectric and charge trapping (FE + CT) behavior. From the third cycle onward (**Fig. S7c**), the hysteresis transitioned to a clockwise direction, reflecting charge-trapping-dominated operation. This progressive evolution suggests a gradual suppression of the ferroelectric response, likely caused by the buildup of interface traps and the presence of unscreened depolarization fields at the HZO/HfO_2/ReS_2 interface.

Stable Operation in MFMIS Devices

By contrast, MFMIS FeFETs incorporating an intermediate metal layer demonstrated stable and reproducible switching characteristics across repeated cycles. The floating gate effectively screens depolarization fields and decouples the ferroelectric layer from interfacial trap effects. As detailed in the main text, this configuration enables consistent ferroelectric-dominated counterclockwise hysteresis loops with excellent endurance and switching stability.

To further elucidate the structural advantages of the MFMIS architecture, we next provide a detailed comparison between MFMIS and MFIS devices in terms of: a) voltage distribution across the ferroelectric layer, b) the influence of depolarization fields, and c) interfacial charge trapping mechanisms.

MFMIS vs. MFIS FeFETs

a) Voltage distribution across the ferroelectric layer

In both MFIS and MFMIS FeFETs, the applied gate voltage V_G is distributed across the ferroelectric layer, gate dielectric, and semiconductor channel, and can be expressed as:

$$V_G = V_{FE} + V_{OX} + V_{FB} + \varphi_S$$

Here, V_{FE} is the voltage across the ferroelectric layer, V_{OX} is the voltage across the overall oxide/semiconductor stack, V_{FB} is the flat-band voltage, and φ_S is the surface potential of the semiconductor.

The gate stack can be modeled as a series connection of the ferroelectric capacitance C_{FE} and the capacitance of the insulating layer and semiconductor (C_{OS}). In this framework, the effective voltage across the ferroelectric is given by:

$$V_{FE} = \frac{C_{OS}}{C_{OS} + C_{FE}} V_G - \frac{P_r}{C_{OS} + C_{FE}}$$

The first term reflects capacitive voltage division, while the second term accounts for the voltage contribution from the remanent polarization (P_r) of the ferroelectric layer.

To include geometric effects, the total capacitance of each layer is scaled by its physical area. The voltage drop across the ferroelectric can then be expressed as:

$$V_{FE} = \frac{C_{OS}A_{OX}}{C_{OS}A_{OX} + C_{FE}A_{FE}} V_{OX} = \frac{\frac{C_{OS}A_{OX}}{C_{FE}A_{FE}}}{1 + \frac{C_{OS}A_{OX}}{C_{FE}A_{FE}}} V_{OX}$$

where A_{OX} and A_{FE} are the physical areas of the insulating/channel and ferroelectric layers, respectively. This expression indicates that V_{FE} is influenced by both the capacitance values and area ratios of the dielectric layers.

In conventional MFIS structures, where $A_{OX} \approx A_{FE}$ and $C_{FE} \gg C_{OS}$, the ratio $\frac{C_{OS}A_{OX}}{C_{FE}A_{FE}} \ll 1$, resulting in a minimal voltage drop across the ferroelectric layer. Consequently, polarization switching is incomplete, and the device exhibits narrow hysteresis loops and reduced memory performance (**Fig. S8a**).

In contrast, the MFMIS structure introduces a floating gate between the ferroelectric and the underlying oxide/channel stack. This design electrically decouples the two regions and allows geometric tuning of A_{FE} and A_{OX}. By setting $A_{OX} > A_{FE}$, the voltage division ratio improves, allowing a larger fraction of the gate voltage to be applied across the ferroelectric. Furthermore, the floating gate functions as an equipotential surface that suppresses capacitive cross-talk, ensuring that the ferroelectric layer receives sufficient bias to achieve complete polarization reversal (**Fig. S8b**). These enhancements enable broader memory windows and more robust nonvolatile performance.

b) The influence of depolarization fields

When the gate bias is removed (i.e., during the retention phase, $V_G = 0$), the FeFET stack must satisfy electrostatic equilibrium and charge neutrality. Under this condition:

$$V_G = V_{FE} + V_{OX} = \frac{Q_{FE} - P_r}{C_{FE}} + \frac{Q_{OS}}{C_{OS}} = 0$$

Solving this yields the charge stored on the ferroelectric interface:

$$Q_{FE} = \frac{P_r C_{OS}}{C_{OS} + C_{FE}}$$

Since this charge does not fully compensate the remanent polarization P_r ($Q_{FE} \neq P_r$), a depolarization field (E_{dep}) is induced within the ferroelectric layer:

$$E_{dep} = \frac{P_r}{\varepsilon_{FE}(\frac{C_{OS}}{C_{FE}} + 1)}$$

This internal field opposes the remanent polarization and promotes gradual destabilization of the ferroelectric state. Over time, the depolarization field causes a shrinkage in the hysteresis window and degrades retention performance, particularly in scaled devices.

In MFIS structures, the large ferroelectric-to-oxide capacitance ratio ($C_{FE} \gg C_{OS}$) combined with a fixed area ratio ($A_{OX} \approx A_{FE}$) results in inefficient compensation of the remanent polarization after gate bias removal. This imbalance generates a strong E_{dep}, which counteracts the polarization and leads to gradual hysteresis degradation and retention loss.

By contrast, the MFMIS structure introduces a floating gate that effectively compensates the polarization-induced bound charges and spatially separates the ferroelectric layer from defect-prone oxide or interface regions. This configuration significantly suppresses E_{dep}, thereby stabilizing the polarization state and improving both retention and endurance.

c) Interfacial charge trapping mechanisms

Charge trapping mechanisms differ fundamentally between MFIS and MFMIS structures.

In MFIS FeFETs, trapped charges accumulate at the oxide/semiconductor interface, typically due to carrier injection from the channel. These charges generate an internal electric field that opposes the ferroelectric polarization, resulting in a competitive interaction. Over successive cycles, this antagonism leads to the suppression of ferroelectric switching, manifesting as a clockwise, charge-trapping-dominated (CT-dominated) hysteresis. This behavior is often accompanied by reduced memory window and poor endurance.

In MFMIS FeFETs, charge trapping primarily occurs at the ferroelectric/metal interface due to gate-side injection. The trapped charges possess the same polarity as the bound ferroelectric dipoles, resulting in a cooperative interaction that reinforces the spontaneous polarization. This effect enhances both P_r and V_{FE}, leading to a strengthened counterclockwise hysteresis. In this case, charge trapping acts as an assistive mechanism that stabilizes ferroelectric domains and improves long-term

retention. This favorable interfacial behavior explains the superior endurance and wider memory window observed in MFMIS devices (**Fig. S9**).

The realization of stable ferroelectric switching is a prerequisite for reliable optoelectronic functionality. Accordingly, the MFMIS structure is adopted to provide a robust electrical foundation for the subsequent integration of optical memory and sensing capabilities.

The relevant additions have been incorporated into the main text, as well as **Supplementary Note S1**, **Fig. S6**–**S9**, **Table S1**.

Corresponding change:

Page: 8, S-4_S-9

Figure: Fig. S6–S9, Table S1, Supplementary Note S1

Table S1. Summary of key differences between MFIS and MFMIS FeFET architectures.

Features	MFIS (without FG)	MFMIS (with FG)
A_{ox} / A_{FE}	≈ 1(fixed)	>1 (tunable)
V_{FE}	Small	Large
E_{dep}	Strong E_{dep} due to incomplete charge compensation	Suppressed by FG
Charge trapping	Oxide/channel interface Channel-side injection Opposes FE Reduces MW	FE/metal interface Gate-side injection Assist FE Enbances MW
Hysteresis loop	Clockwise (trap-dominated)	Counterclockwise (FE-dominated)

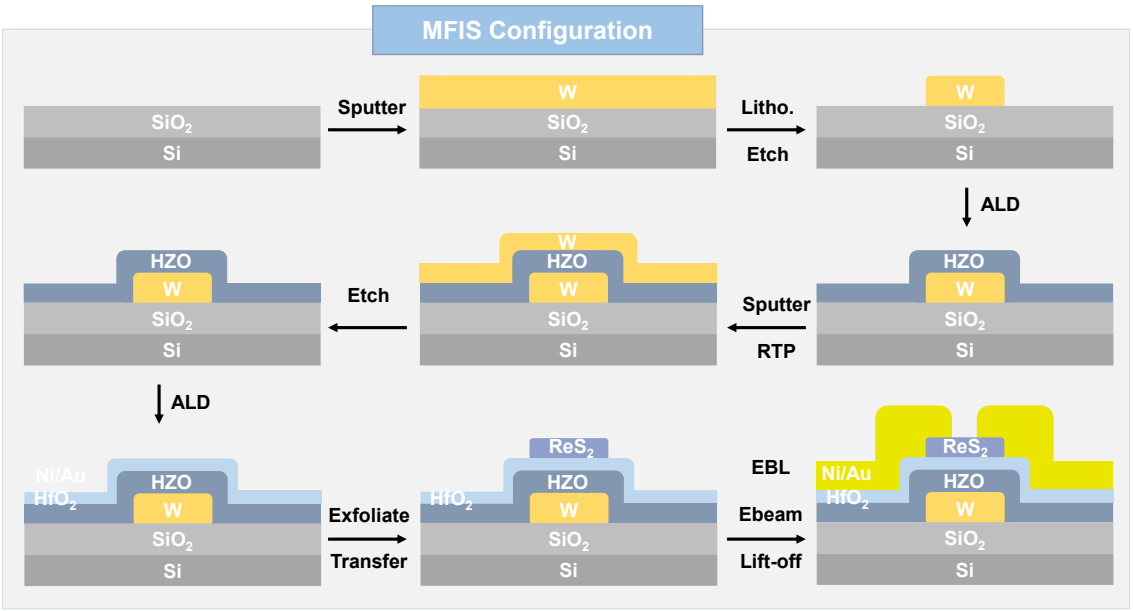


Fig. S6 Fabrication process flow of the ReS_2-based MFIS-FeFET. The device is built by first depositing a tungsten (W) layer and patterning it into the control-gate electrode. A ferroelectric HZO layer is then deposited uniformly by atomic-layer deposition (ALD), followed by W capping and an annealing step to crystallize the HZO. The cap is subsequently removed, and a high-k HfO_2 dielectric interfacial layer is deposited via ALD. The ReS_2 channel is then transferred onto the dielectric stack, and the source/drain electrodes are formed to complete the MFIS FeFET architecture.

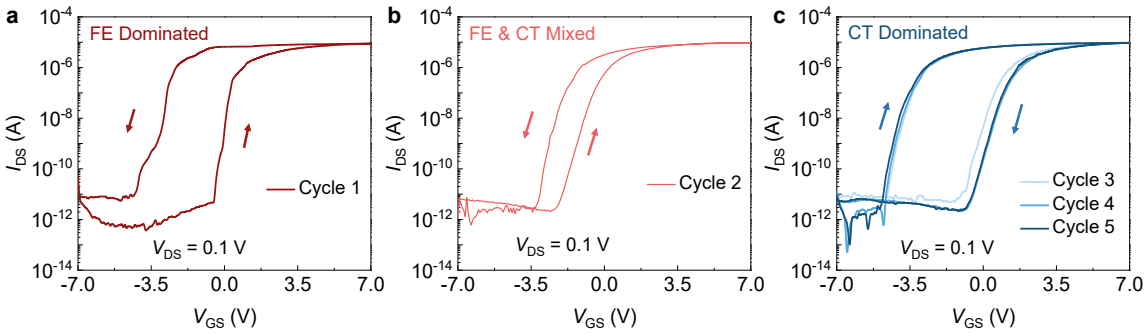


Fig. S7 The I_{DS}–V_{GS} characteristics of a ReS_2-based MFIS FeFET measured at V_{DS} = 0.1 V over successive cycles. a. The device initially exhibits a ferroelectric (FE)-dominated hysteresis. b. It then transitions to a mixed FE and charge trapping (CT) state. c. Finally, it becomes CT-dominated, indicating the progressive suppression of ferroelectric switching due to competing interface charge trapping.

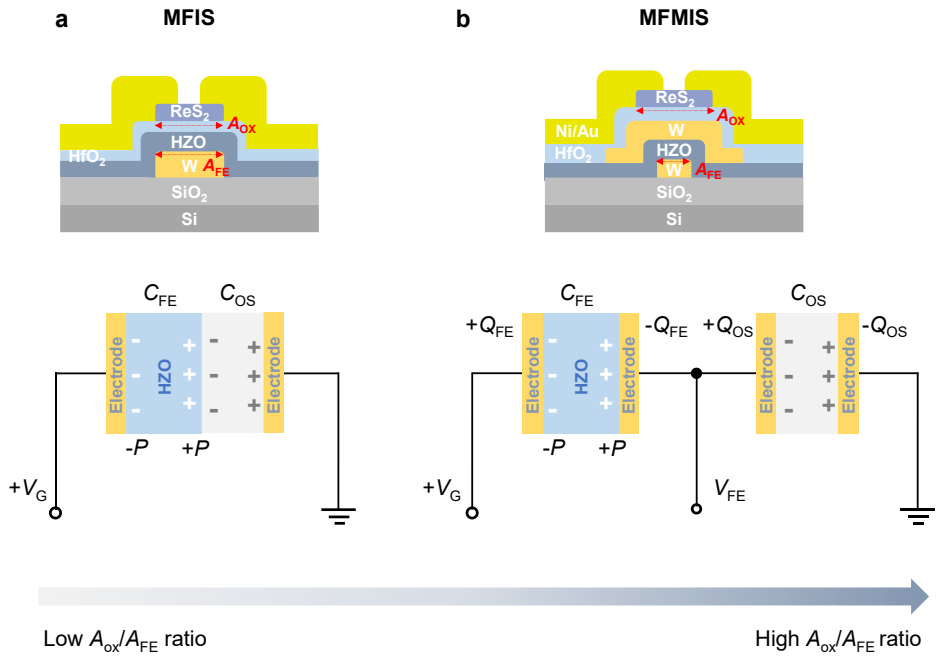


Fig. S8 a. Cross-sectional schematic and corresponding voltage and charge distribution of the MFIS FeFET, illustrating a fixed A_{OX} / A_{FE} ratio and incomplete charge compensation. **b**. Cross-sectional schematic and voltage/charge distribution of the MFMIS FeFET, demonstrating a tunable A_{OX} / A_{FE} ratio and enhanced charge compensation enabled by the inserted floating gate.

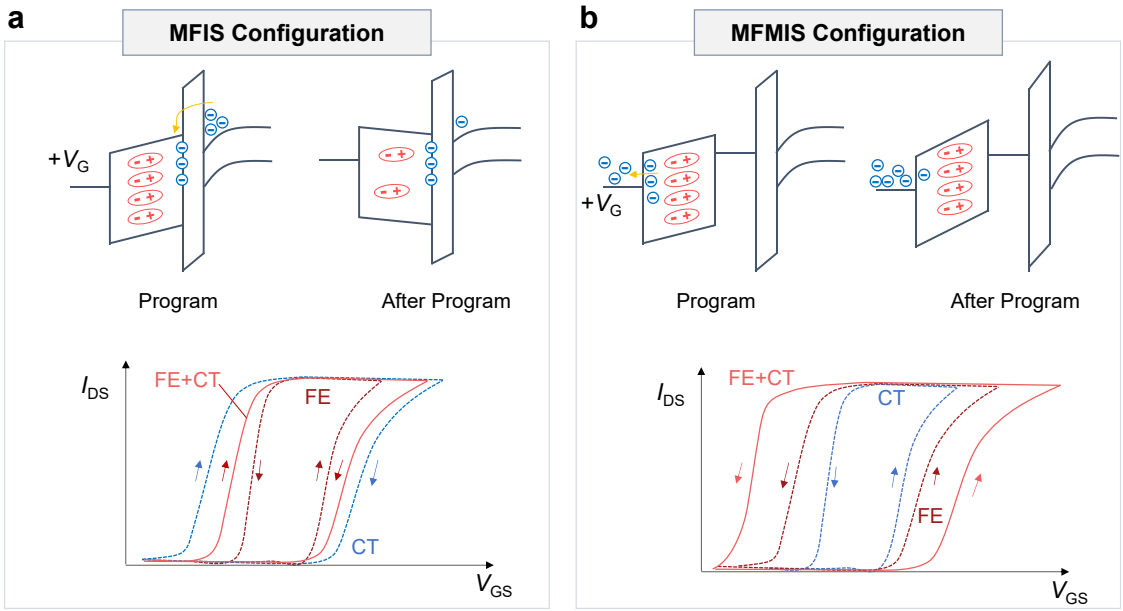


Fig. S9 a. In the MFIS configuration, charge trapping occurs at the oxide/semiconductor interface, generating an internal electric field that opposes the ferroelectric polarization. This competition

reduces the effective V_{FE} and gradually suppresses domain switching, resulting in clockwise hysteresis dominated by charge trapping (CT > FE). **b**. In the MFMIS configuration, the inserted metal layer spatially separates the ferroelectric from interface traps and shifts charge trapping to the ferroelectric/metal interface. The trapped charges align with ferroelectric dipoles, reinforcing polarization switching. This cooperative effect enhances V_{FE} and leads to a stable counterclockwise hysteresis dominated by ferroelectric switching, with CT acting as a supporting mechanism.

Reviewer #2

The authors have made considerable efforts to address the previous reviewers' comments. Nevertheless, they have not provided a clear or satisfactory resolution to the most critical weakness of this work–the lack of sufficient novelty. Furthermore, for many of the previously raised concerns, their responses remain unconvincing or insufficiently clear. Therefore, consistent with my earlier assessment, it is difficult to recommend this work for publication.

Our response:

We sincerely thank the reviewer for the careful evaluation and for raising the concern regarding novelty. We fully acknowledge the rapid progress in both FeFET memory and ReS_2-based optoelectronic devices, and we agree that a clear distinction of our contribution is essential. We therefore highlight below the unique innovations and advantages of our work.

1) Suitability of the MFMIS Architecture for Optoelectronic Studies

Conventional MFIS FeFETs often face challenges such as strong depolarization fields, poor interfacial coupling between the ferroelectric and the 2D channel, and fixed ferroelectric-to-channel area ratios that limit capacitive voltage division. As a result, the effective voltage drop across the ferroelectric layer is reduced, weakening polarization switching and leading to unstable memory characteristics. In our comparative measurements (**Fig. R2a**), the MFIS device shows a clear evolution from ferroelectric-dominated switching, to a mixed ferroelectric–charge-trapping regime, and finally to predominantly defect-driven behavior. Such instability highlights that MFIS devices cannot provide a reliable electrical foundation for further optical studies.

By contrast, the MFMIS configuration, through the insertion of a floating gate between the HZO ferroelectric and the ReS_2 channel, not only suppresses depolarization fields and improves interfacial quality but also allows precise tuning of the effective area ratio and capacitive voltage division between the ferroelectric and channel. This design ensures a larger voltage drop across the ferroelectric layer, promoting robust polarization switching, and thereby yielding more stable and reproducible memory characteristics (**Fig. R2b**). Such

stable ferroelectric control is essential to maintain ultralow dark current and long retention, ultimately providing a solid and reliable platform for subsequent exploration of optoelectronic functionalities. Therefore, unlike MFIS devices that often suffer from instability and charge-trapping–dominated behavior, the MFMIS architecture provides the necessary stability and tunability to unlock reliable polarization-sensitive and optoelectronic operations.

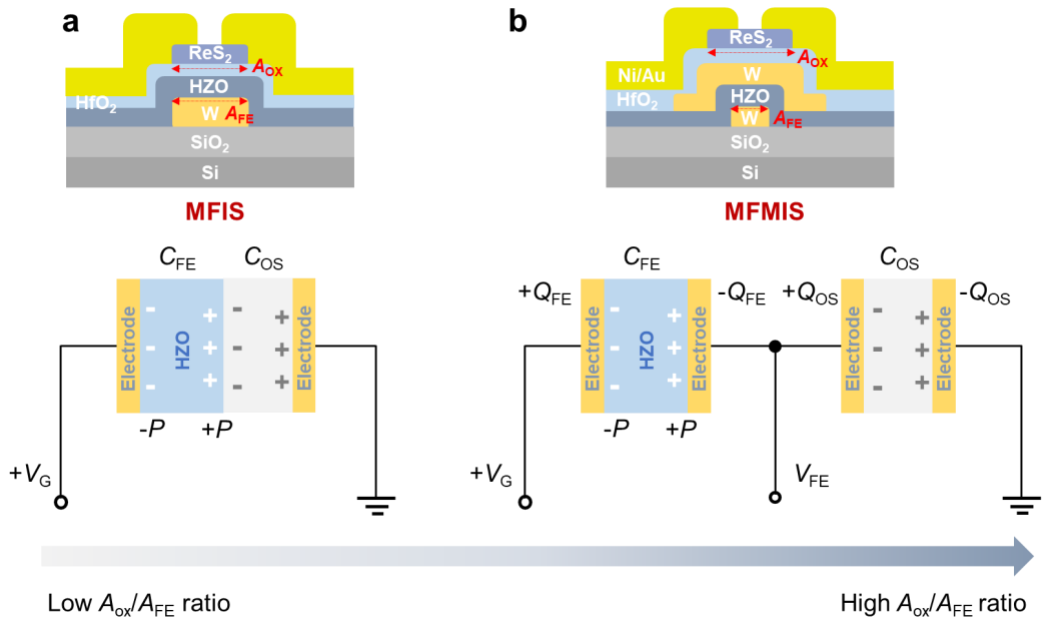


Fig.R1. (**a**) Cross-sectional schematic and corresponding voltage and charge distribution of the MFIS FeFET, illustrating a fixed A_{OX}/A_{FE} ratio and incomplete charge compensation. (**b**) Cross-sectional schematic and voltage/charge distribution of the MFMIS FeFET, demonstrating a tunable A_{OX}/A_{FE} ratio and enhanced charge compensation enabled by the inserted floating gate.

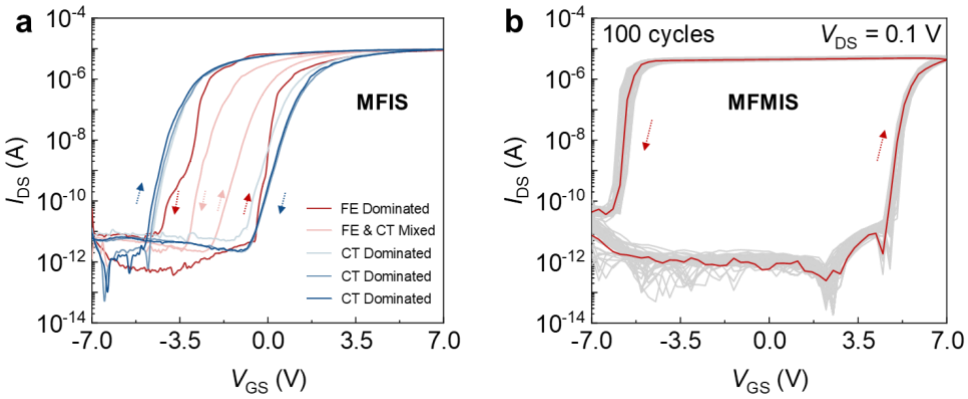


Fig.R2. (**a**) The I_{DS}-V_{GS} characteristics of a ReS_2-based MFIS FeFET measured at V_{DS}=0.1 V over successive five cycles. The device initially exhibits a ferroelectric (FE)-dominated hysteresis. It then transitions to a mixed FE and charge trapping (CT) state. Finally, it becomes CT-dominated, indicating the progressive suppression of ferroelectric switching due to competing interface charge trapping. (**b**) The I_{DS}-V_{GS} characteristics of a ReS_2-based MFMIS FeFET measured at V_{DS}=0.1 V over successive 100 cycles.

Thus, in our work, we extend this architecture into the optoelectronic domain. The strong and durable ferroelectric polarization control provided by the MFMIS design not only ensures stable electrical memory characteristics but also supports an ultralow dark current and excellent retention. These stable electrical features form a robust foundation for optical studies, where the suppression of background fluctuations is essential for reliably extracting photoresponse signals. On this basis, the intrinsic anisotropy of the ReS_2 channel can be fully expressed, allowing us to demonstrate polarization-sensitive photodetection, ferroelectric-assisted optical programming, and long-lived optoelectronic memory.

We respectfully believe that this extension highlights the novelty of our work: by leveraging the inherent advantages of the MFMIS architecture, we establish a ferroelectric FeFET platform that is not only electrically stable but also ideally suited for exploring and realizing polarization-resolved optoelectronic functionality.

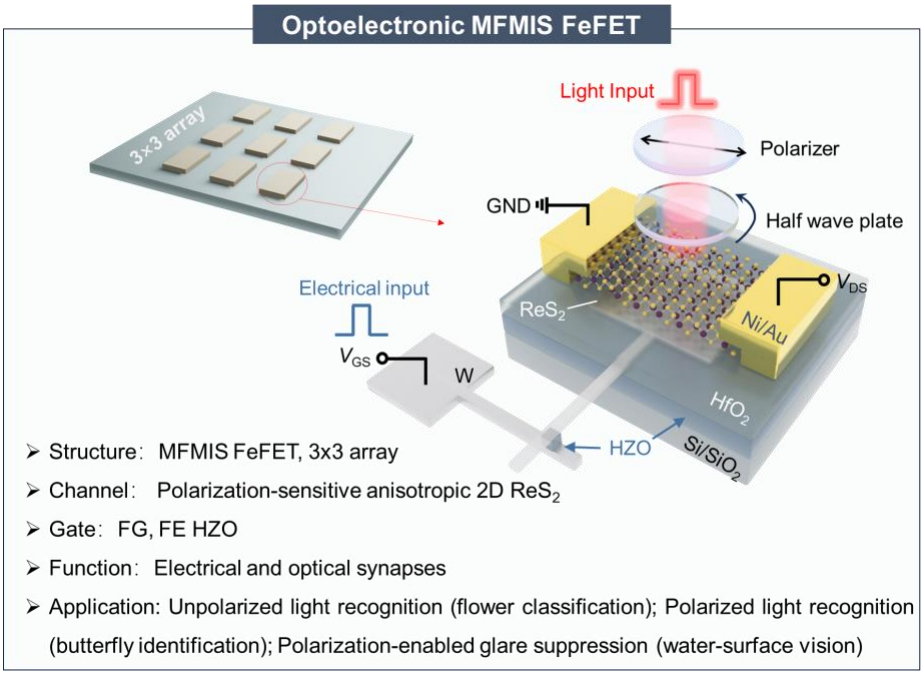


Fig.R3. Proposed polarization-sensitive optoelectronic MFMIS FeFET for in-sensor computing.

2) Synergistic Coupling of Ferroelectricity, Charge Trapping and 2D-material Anisotropy

Building on the stable electrical foundation provided by the MFMIS architecture, our device uniquely integrates stable ferroelectric control, polarization-sensitive photoresponse, and non-volatile optical storage into a single framework. This multifunctional coupling extends FeFET operation beyond conventional electrical memory.

The ferroelectric layer ensures long-retention polarization with suppressed leakage, offering a stable and noise-free baseline for optical operation. On this foundation, the polarization-sensitive ReS_2 channel introduces intrinsic in-plane anisotropy and strong light–matter interaction, giving rise to directional photocarrier generation and anisotropic photoresponse that cannot be achieved with isotropic semiconductors such MoS_2. Meanwhile, the floating gate (FG) couples these effects by stabilizing ferroelectric polarization and capturing photogenerated carriers as persistent memory states, thereby enabling reliable and rewritable optical programming.

Through this cooperative mechanism, our MFMIS FeFET achieves a synergy of sensing, memory, and computation that is inaccessible to prior FeFET designs. By unifying

stable electrical control, polarization-resolved photodetection, and optoelectronic memory within one platform, it establishes a compact and scalable route toward polarization-sensitive neuromorphic vision applications.

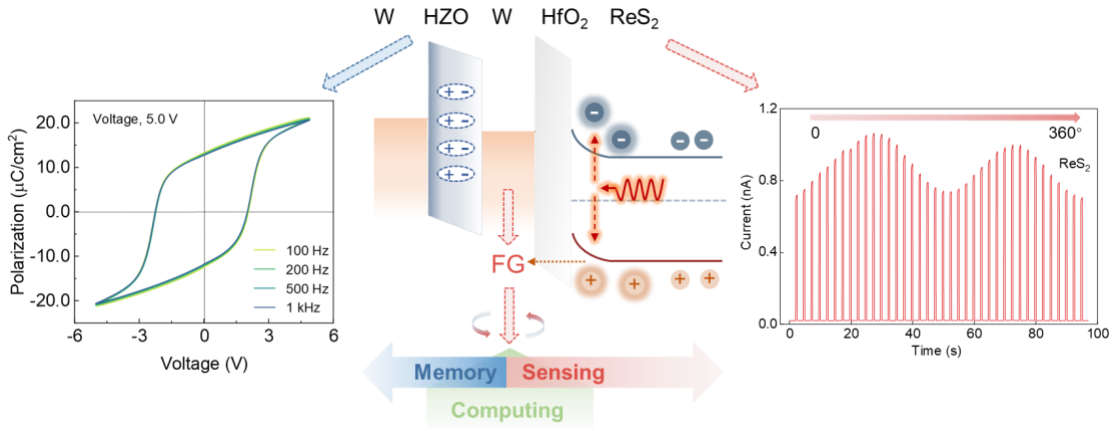
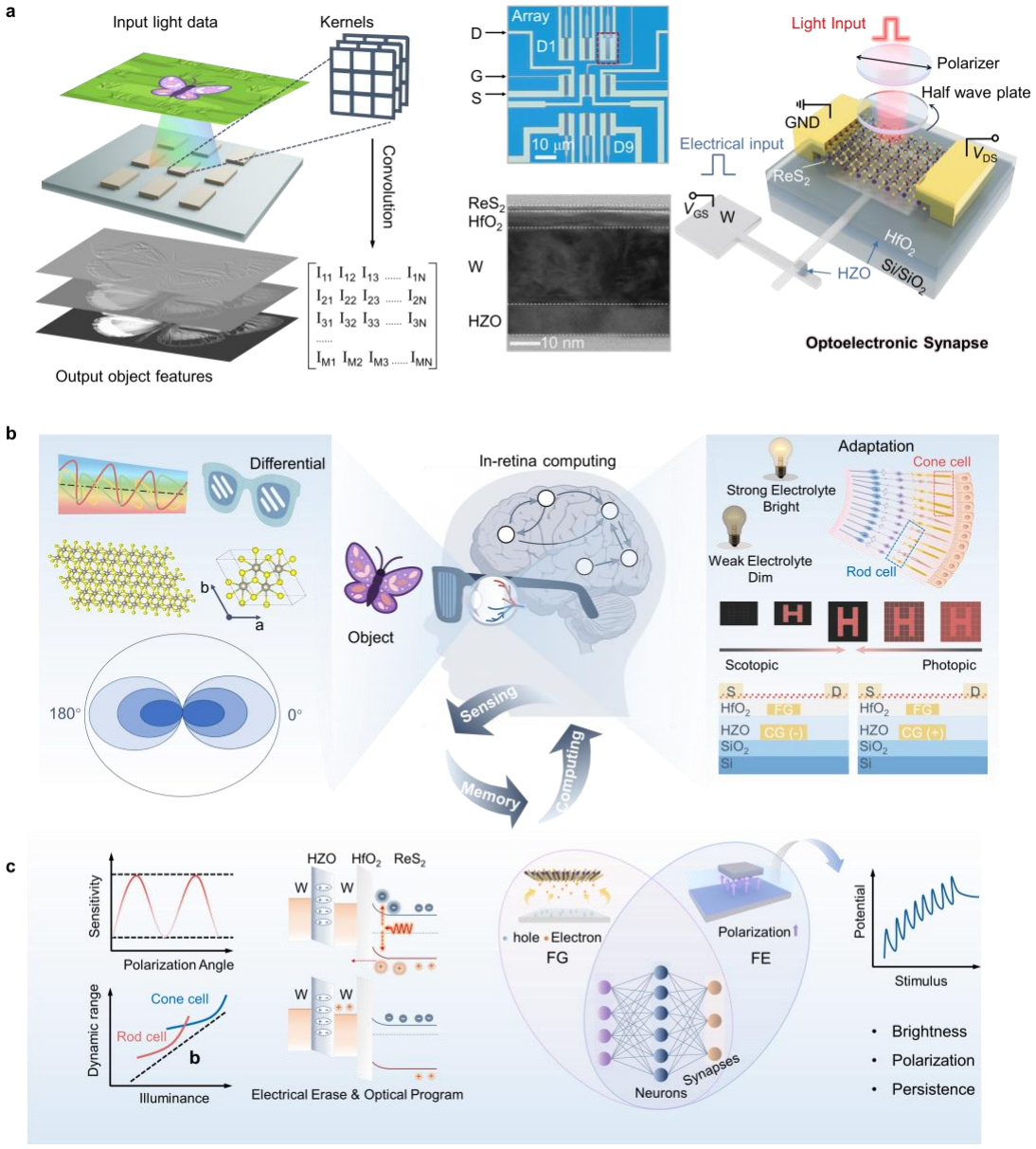


Fig.R4. Schematic illustration of the integrated sensing–memory–computing mechanism in the proposed MFMIS FeFET. Photogenerated carriers in the anisotropic ReS_2 channel are driven into the floating gate (FG) under the assistance of the ferroelectric polarization field, enabling non-volatile optical memory. Meanwhile, ferroelectric polarization stabilizes electrical memory states and suppresses background leakage, providing a reliable baseline for optoelectronic modulation. This cooperative mechanism unifies sensing, memory, and computing within a single FeFET platform.



3) Enhanced Photodetection Performance by Coupling Effect

Previous studies on ReS_2 optoelectronic devices have generally advanced along two main directions. On the one hand, ReS_2-based vdW heterostructure photodetectors (e.g., ReS_2/PVK, ReS_2/Gr) have achieved reduced dark current and high responsivity, but their functionality has been limited to light sensing only, without any capability for information storage or processing. On the other hand, ReS_2-based synaptic devices have demonstrated non-volatile conductance modulation, but their reliance on non-CMOS-compatible approaches (e.g., defect-mediated charge trapping in Si substrates or mechanically

transferred Cr floating gates) makes them unsuitable for large-scale integration. These limitations highlight the importance of developing a unified architecture that can simultaneously provide high-performance photodetection, stable non-volatile memory, and scalability for practical neuromorphic hardware.

In contrast, our work uniquely integrates both high-performance photodetection and non-volatile optoelectronic memory within a single MFMIS FeFET. The ferroelectric HZO gate ensures **ultralow dark current (100 fA)** and **long retention (10^4 s)**, while the ReS_2 channel provides strong light–matter interaction and intrinsic polarization sensitivity. Together with the floating gate that stores photocarriers and couples with ferroelectric polarization, our device achieves state-of-the-art photodetection (**responsivity of 4×10^5 A/W and detectivity of 1.9×10^{14} Jones**), while simultaneously supporting rewritable optical–electrical memory and synaptic plasticity with an ultralow energy consumption of only **2 fJ per event**. This unified platform not only reduces system complexity but also extends FeFET functionality into the optoelectronic domain, offering a compact, polarization-sensitive hardware solution for advanced neuromorphic vision applications.

Table S2. Comparison of ReS_2-based vdW heterostructures photodetectors and photoelectronic synapses.

Feature		Photodetector [1]	Photodetector [2]	Optical synapse [3]	Optical synapse [4]	This work
Structure		ReS_2/PVK	ReS_2/Gr	ReS_2/h-BN/Gr	Back gate	MFMIS FeFET
Channel		ReS_2	ReS_2	ReS_2	ReS_2	ReS_2
Mechanism		vdW heterostructures	vdW heterostructures	Graphene FG	Charge trapping	Hybrid FE-FG
Electrical performance	I_{OFF}	-	10 pA	10 pA	1 pA	**100 fA**
	I_{ON}/I_{OFF}	-	10^5	10^5	10^6	**10^7**
	MW **SR** **Ratio**	-	-	80 V -50_50 V 80%	80 V -80_80 V 50%	10.5 V -7_7 V 75%
Optical performance	***R***	2.2 A/W	10^6A/W	-	-	4×10^5 A/W
	D*	1.8×10^{14} Jones	3.2×10^{12} Jones	-	-	**1.9×10^{14} Jones**

	PR	-	-	-	-	**1~12**
Functionality		photodetector	photodetector	Electro-optical synapse	Electro-optical synapse	Integrated electro-optical memory & synapse
Array implementation		-	-	No	No	Yes (3×3 Array)
Applications		-	-	Image recognition; optoelectronic CNN	Digit classification; optoelectronic ANN	Polarization-resolved vision; Unpolarized light optoelectronic ANN; Polarized light CNN

References:

[1]. Su, W. et al. Interlayer Transition Induced Infrared Response in ReS_2/2D Perovskite van der Waals Heterostructure Photodetector. *Nano Lett.* **22**, 10192–10199 (2022).

[2]. Mukherjee, S. et al. Achieving nearly barrier free transport in high mobility ReS_2 phototransistors with van der Waals contacts. *npj 2D Mater. Appl.* **8**, 71 (2024).

[3]. Li, W. et al. The Nonvolatile Memory and Neuromorphic Simulation of ReS_2/h-BN/Graphene Floating Gate Devices Under Photoelectrical Hybrid Modulations. *Small* **20**, 2311630 (2024).

[4]. Chen, Y. et al. Wrinkled Rhenium Disulfide for Anisotropic Nonvolatile Memory and Multiple Artificial Neuromorphic Synapses. *ACS Nano* **18**, 30871–30883 (2024).

4) Unique Polarization-Sensitive Applications and Array-Level Validation

To further illustrate the practical relevance of these functionalities, we explored representative vision-related tasks that leverage different aspects of our device operation.

For unpolarized light conditions such as natural flower recognition, we implemented an optoelectronic artificial neural network (ANN) in which the synaptic weights are regulated by both non-volatile electrical modulation and optically assisted tuning. This cooperative control provides stable and energy-efficient pattern classification, demonstrating how the integration of electrical and optical memory states can be directly utilized for neuromorphic learning under natural illumination.

For polarized light scenarios, the intrinsic in-plane anisotropy of the ReS_2 channel provides a distinct advantage. As a representative example, we fabricated a small-scale 3×3 ReS_2 FeFET array and employed it to perform convolutional neural network (CNN)

simulations of butterfly recognition. In this case, the polarization-resolved photoresponse of ReS_2 enabled the discrimination of subtle polarization cues, analogous to how butterflies recognize conspecifics through wing reflection patterns.

In addition, we simulated polarization-enabled glare suppression, where the device distinguishes strongly polarized glare (e.g., from sky reflections) from unpolarized underwater signals. This bio-inspired functionality reproduces strategies used by aquatic organisms for contrast enhancement and highlights how ReS_2-based FeFETs can be applied to advanced imaging scenarios that cannot be realized with isotropic channel materials such as MoS_2.

These demonstrations collectively emphasize that our platform not only unifies non-volatile electrical and optical memory, but also uniquely leverages the anisotropic nature of ReS_2 to enable a broad range of neuromorphic vision tasks, from conventional pattern classification to polarization-sensitive recognition and glare-resilient imaging. The results underscore the distinctive role of ReS_2 in extending FeFET functionality and point toward future opportunities for polarization-resolved vision applications.

[FIGURE REDACTED]

Fig. R5. Neuromorphic vision demonstrations based on ReS_2 MFMIS FeFETs. (**a**) Schematic illustration of polarization-dependent natural light and its role in biological recognition. (**b**) Device-level synaptic characteristics under electrical and optical stimuli. (**c**) ANN simulation for iris flower recognition under unpolarized light. (**d**) CNN-based convolution simulation for butterfly recognition under polarized light.

Reviewer #4

The author reports an optoelectronic synapse based on a 2D ReS_2 channel and a ferroelectric $HfZrO_2$ (HZO) gate dielectric in a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) ferroelectric field-effect transistor (FeFET). Moreover, linear and tunable synaptic behavior is achieved via optical-electrical dual-mode modulation, with energy consumption as low as 2.0 fJ per synaptic event. I believe the author chose ReS_2 as the channel material because of its polarization properties. However, the research on polarization properties in this paper is quite limited, and the advantages of using ferroelectric gate dielectrics and the MFMIS structure for polarization properties have not been demonstrated. Therefore, the article lacks a clear novelty and is not recommended for publication in NC.

Please note that the following comments can be used to further improve the quality of the manuscript.

Our response:

We sincerely thank the reviewer for the constructive comments and suggestions. Following the reviewer's advice, we have carried out a more in-depth investigation of the polarization properties in our ReS_2-based MFMIS FeFETs. In particular, we have clarified how the ferroelectric gate dielectric and the MFMIS architecture enhance polarization-related behaviors, and we have added additional analysis and new supporting data to illustrate these effects. We believe these clarifications better highlight the novelty of our work and strengthen the overall conclusions.

Suitability of the MFMIS architecture for optoelectronic operation (MFMIS vs. MFS/MFIS)

Compared with conventional MFS or MFIS structures, which often suffer from strong depolarization fields, limited tunability of the ferroelectric-to-channel area ratio, unfavorable voltage division across the dielectric/semiconductor stack, and poor interfacial quality between the 2D semiconductor and the ferroelectric, stable ferroelectric control is difficult to achieve. As a result, the electrical performance of these devices is frequently unstable, making them a weak foundation for further exploration of optical functionalities.

In contrast, the MFMIS configuration, by introducing a floating gate between the HZO ferroelectric layer and the ReS_2 channel, effectively suppresses depolarization fields, improves interfacial coupling, and ensures more robust and durable ferroelectric polarization with more symmetric and reproducible switching.

In our work, this stable and well-controlled electrical behavior provides a strong platform to support polarization-sensitive optoelectronic functions. Specifically, the reduced dark current and improved retention raise the signal-to-noise ratio and allow the intrinsic anisotropy of ReS_2 to be more clearly expressed, enabling reliable polarization-resolved photodetection. At the same time, the stable ferroelectric polarization field assists in trapping photogenerated carriers in the floating gate, giving rise to non-volatile optical programming and long-lived memory states. Together, these features ensure that optical modulation in our device is both robust and reproducible, which is essential for advancing from basic photodetection toward functional applications such as bio-inspired recognition and neuromorphic vision.

Polarization-Sensitive High-Performance Photodetection

Building on the stable and well-controlled electrical characteristics provided by the MFMIS structure, the optical performance of our device can be fully exploited. The suppressed dark current and excellent retention ensure that optical measurements are highly reliable, free from spurious background fluctuations. As a result, the device exhibits high responsivity and detectivity, establishing it as a high-performance photodetector. Moreover, the intrinsic in-plane anisotropy of the ReS_2 channel enables a pronounced polarization dependence in the photoresponse. This property opens opportunities for specialized applications such as polarization-assisted recognition, anti-glare imaging, and bio-inspired vision—functionalities that are not achievable in FeFETs based on isotropic channel materials like MoS_2.

Integration of photodetection and memory functions

In conventional system designs, photodetection and memory are realized in separate components, requiring additional interfacing circuits to capture, transfer, and store optical signals. This separation inevitably increases hardware complexity, energy consumption, and latency, and also introduces potential noise at the sensor–memory interface. By contrast, our MFMIS FeFET integrates these two essential functions within a single device. On the

one hand, it operates as a high-performance photodetector, exhibiting low dark current, high responsivity, and strong polarization-dependent sensitivity. On the other hand, it simultaneously provides optical–electrical cooperative memory and synaptic plasticity, allowing photogenerated carriers to be directly trapped and stored through ferroelectric-assisted modulation.

This functional unification enables direct conversion of transient optical inputs into persistent and rewritable memory states, without the need for external memory units. Such integration not only reduces system complexity but also enhances efficiency, scalability, and noise immunity. More importantly, it establishes a versatile platform where sensing, storage, and synaptic learning can be seamlessly combined, paving the way for compact, energy-efficient optoelectronic neuromorphic systems.

From Electrical Memory to a Polarization-Sensitive Optoelectronic Neuromorphic Platform

Taken together, our results move beyond the scope of previously reported FeFET-based in-memory computing *(Nat. Commun. 2021; Nat. Nanotechnol. 2023; Sci. Adv. 2024)*, which have primarily focused on electrical memory and weight modulation. These pioneering studies established FeFETs as strong candidates for non-volatile electrical memory and in situ learning hardware, but did not address the potential for integrating optical sensing or polarization-dependent functionalities.

In contrast, our study introduces, to our knowledge, a novel demonstration of polarization-sensitive optoelectronic functionality integrated directly into a ferroelectric-gated MFMIS FeFET. By combining robust electrical memory with high-performance photodetection and intrinsic anisotropic polarization sensitivity, our device unifies three essential functions—sensing, memory, and computation—within a single scalable platform. This integration not only reduces circuit complexity and energy cost, but also enables unique capabilities such as polarization-resolved imaging, glare suppression, and bio-inspired recognition tasks that are unattainable in conventional FeFET systems based on isotropic channels.

We respectfully believe that this represents a substantive advance: extending the well-established FeFET paradigm beyond electrical in-memory computing toward a multifunctional, polarization-resolved optoelectronic neuromorphic vision platform.

Unique Polarization Sensitivity and Application Relevance

A particularly distinctive aspect of our ReS_2-based MFMIS FeFET lies in its intrinsic polarization sensitivity, which directly translates into unique functional applications. The in-plane anisotropy of ReS_2 enables the device to resolve polarization cues that are invisible to FeFETs built on isotropic materials such as MoS_2. This characteristic makes possible specialized vision-related tasks that mimic biological systems—for example, the ability of butterflies to recognize conspecifics through polarization patterns on their wings. Likewise, the device can suppress glare from reflective surfaces such as water or glass, supporting anti-glare imaging in complex environments. These polarization-driven capabilities are fundamentally beyond the reach of isotropic-channel FeFETs and highlight the unique material–architecture synergy of our platform.

Comment#1:

Has the polarization property of ReS_2 been improved by using ferroelectric gate dielectric and MFMIS? In what aspects is this manifested? For example, maximum polarized responsivity? dichroic ratio?

Our response:

We thank the reviewer for this important question regarding the polarization properties of ReS_2 and how they are manifested in our ferroelectric MFMIS architecture.

As shown in the newly added figure (**Fig.R2**), the polarization-resolved photoresponse of our ReS_2 FeFET clearly demonstrates the combined effect of the intrinsic anisotropy of ReS_2 and the stabilization provided by ferroelectric gating. In **Fig.R2a**, the polarization ratio (PR, defined as $I_{b\text{-axis}}/I_{a\text{-axis}}$) is plotted against V_{GS}. The PR increases significantly near the ferroelectric-polarized operating points, providing direct evidence that ferroelectric gating enhances polarization selectivity. **Fig. R2b** presents the normalized photocurrent as a function of polarization angle θ, where the two-lobed pattern along the crystalline axes becomes increasingly asymmetric under ferroelectric modulation. This observation is consistent with the gate-enhanced PR in **Fig. R2a**, confirming improved polarization selectivity. It should be noted that panel (b) is normalized to emphasize angular dependence rather than absolute current level.

Mechanistically, this enhancement originates from the ferroelectric HZO layer, whose remanent polarization generates a stable electrostatic field that shifts the Fermi level and modulates the carrier concentration in the ReS_2 channel. Because anisotropic 2D materials such as ReS_2, black phosphorus, and WTe_2 exhibit direction-dependent band structures and optical transition strengths, this Fermi-level shift affects the *a*- and *b*-axes unequally. Specifically, the allowed optical transitions in different directions undergo unequal filling and screening, altering the relative absorption strength of each axis.

Consequently, the *b*-axis exhibits stronger absorption and photocurrent, while the *a*-axis response is comparatively suppressed, leading to an enhanced dichroic ratio and more pronounced angular selectivity. This unequal modulation directly explains the increased PR in Fig. R2a and the stronger polarization contrast in Fig. R2b.

In addition, the floating gate in the MFMIS stack traps and stabilizes photocarriers, reducing recombination and suppressing dark current. This synergistic effect ensures that the intrinsic anisotropy of ReS_2 is more effectively translated into device-level performance.

Thus, the integration of a ferroelectric gate dielectric does not alter the fundamental in-plane anisotropy of ReS_2; rather, it amplifies and stabilizes the polarization-resolved response. This is manifested in (**i**) a gate-enhanced dichroic ratio, evidencing stronger polarization selectivity, and (**ii**) a more asymmetric angular dependence in the normalized polar plot. Together, these results highlight the synergistic role of ferroelectric modulation in strengthening polarization-sensitive optoelectronic functionality.

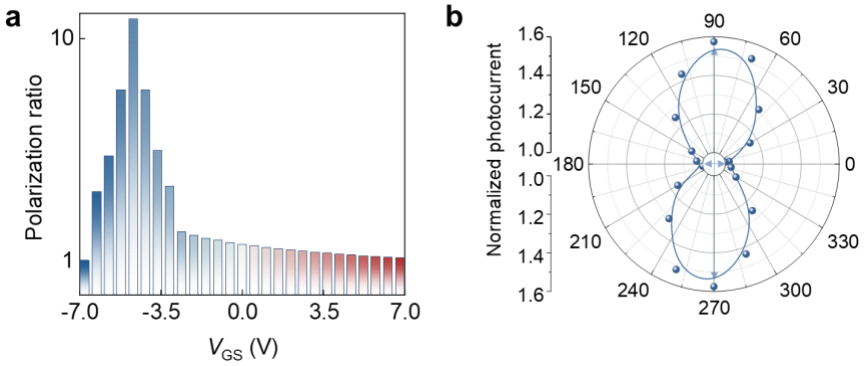


Fig.R2. Polarization-resolved photoresponse of the ReS_2 MFMIS FeFET. a. The polarization ratio (PR; $I_{b\text{-axis}}/I_{a\text{-axis}}$) is plotted as a function of V_{GS}. **b.** The normalized photocurrent versus the incident polarization angle θ. These results confirm the intrinsic in-

plane anisotropy of ReS_2 and demonstrate that ferroelectric modulation enhances both the maximum polarized response and the polarization contrast.

Comment #2:

Please explain in detail what the symbol "T" represents in Figure 4j and how it is related to the device. Is the application of this scenario only possible with devices that have ferroelectric long-time plasticity? If not, what are the advantages of the ferroelectric device proposed by the author in such scenarios?

Our response:

We appreciate the reviewer's insightful question and the opportunity to clarify.

Definition of "T" and Relation to the device

In the original version, "T" referred to the time window used in the simulation, ranging from 100 μs up to 25,600 μs (i.e., 25.6 ms). Importantly, this parameter is not arbitrary but directly corresponds to the experimental measurements shown in Fig. 4i (**Fig. R3**), where polarization-resolved learning is demonstrated. In Fig. R3b, the device response surface under repeated optical stimulation clearly reflects how extended time windows enable gradual signal accumulation, while Fig. R3c, progressive recognition of sky glare and underwater features emerges with increasing time steps. These measured behaviors, arising from the polarization-sensitive conductance modulation of the ferroelectric ReS_2 MFMIS FeFET, form the basis of the simulation. We acknowledge that the labeling of "T" may have caused confusion and have therefore removed it from the revised figure.

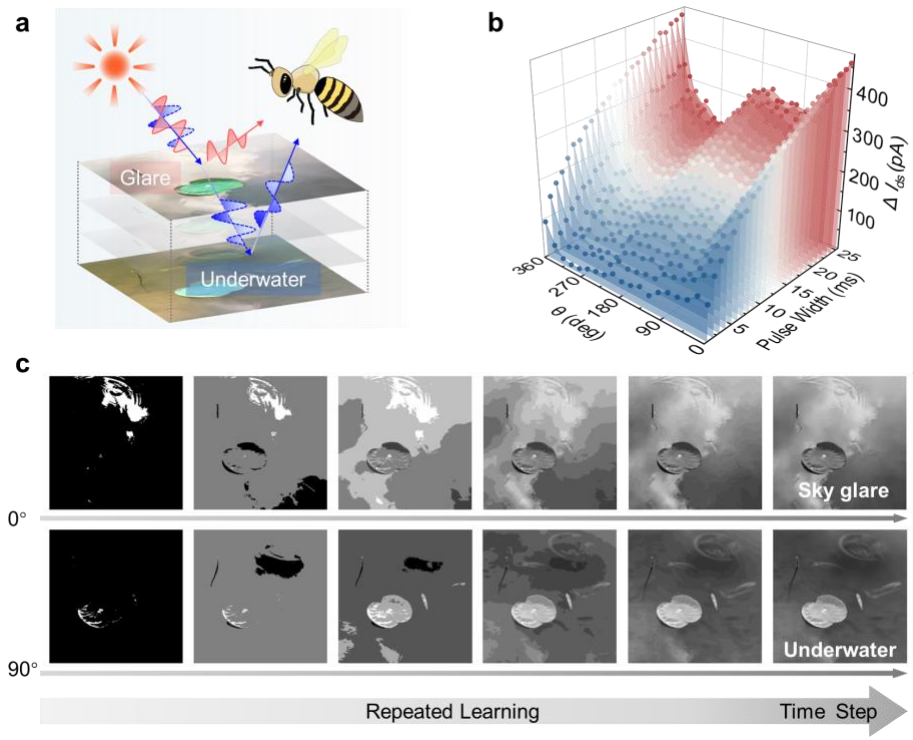


Fig. R3. Polarization-resolved learning and recognition. (**a**) Schematic illustration of polarization cues, where insects can distinguish between sky glare and underwater targets by analyzing reflected polarized light. (**b**) Device response surface showing the dynamic evolution of polarization-sensitive signals under repeated optical stimulation. (**c**) Progressive learning outcomes for polarization-resolved vision tasks, where the FeFET array gradually enhances recognition of sky glare (top row) and underwater features (bottom row) with increasing time steps.

Relevance to ferroelectric long-time plasticity

The scenario directly illustrates the role of ferroelectric long-time plasticity in our devices. As shown in **Fig. R4a**, a conventional architecture without this property requires a photodetector to be paired with an external memory and computing unit in order to accumulate and process optical signals. By contrast, in our proposed ReS_2 MFMIS FeFET (**Fig. R4b**), the stable remanent polarization of the HZO layer inherently provides long-time plasticity, enabling gradual and accumulative modulation of synaptic weights under repeated optical and electrical stimuli. This behavior is analogous to biological synapses, where repeated inputs progressively strengthen synaptic connections. A key implication is that extending the effective integration time window allows the device to suppress short-

term noise fluctuations while highlighting the desired signal. In practice, this results in progressively clearer reconstructed patterns as transient disturbances are averaged out and relevant features are retained, providing a direct pathway to improved image quality and signal fidelity in optoelectronic neuromorphic tasks.

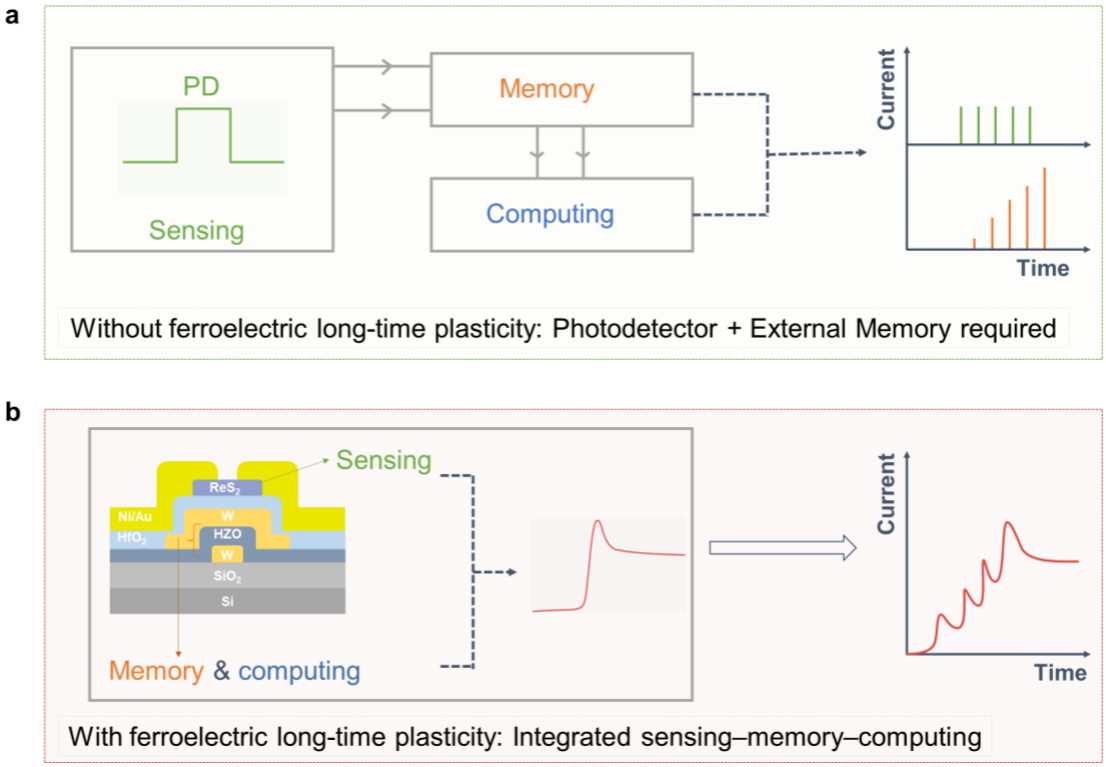


Fig. R4. Comparison of system architectures with and without ferroelectric long-time plasticity. (**a**) Conventional architecture without ferroelectric long-time plasticity, where a photodetector (PD) must be combined with an external memory and computing unit to accumulate and process optical signals. (**b**) Proposed ReS_2 MFMIS FeFET with ferroelectric long-time plasticity, in which sensing, memory, and computing are inherently integrated within a single device. The embedded ferroelectric polarization enables direct conversion of optical inputs into persistent current responses, eliminating the need for external memory and reducing system complexity, latency, and noise.

Essential role and advantages of ferroelectricity

If ferroelectric long-time plasticity were absent, equivalent functionality could only be realized by pairing a simple photodetector with an external memory unit, as shown in Fig. R4a. Such a two-component system inevitably increases circuit complexity, energy

consumption, and latency, while also introducing interface noise. By contrast, as shown in Fig. R4b, our ferroelectric MFMIS FeFET inherently embeds the memory function: ferroelectric polarization provides stable non-volatile states, and the floating gate allows cumulative trapping of photogenerated carriers. As a result, optical inputs are directly converted into persistent current responses within a single device, eliminating the need for external memory and ensuring efficient, low-noise operation.

Moreover, the ferroelectric design offers distinct advantages, including (i) enhanced retention through stable polarization, (ii) reliable multilevel weight programming under combined optical/electrical stimuli, and (iii) ultralow energy consumption. These attributes make the proposed device particularly well suited for neuromorphic vision scenarios where stable, efficient, and integrated sensing–memory–computing are required.

Comment #3:

Similarly, what is the connection between the algorithm shown in Figure 5 and ferroelectric polarization and polarization characteristics, and why is it employed here?

Our response:

We thank the reviewer for this important question.

In the original version, Fig. 5 (**Fig. R5**) presented an ANN-based iris recognition task under unpolarized light, chosen as a representative vision-related classification example. The connection between the device and the algorithm was established by mapping the gradual, multilevel conductance states—originating from ferroelectric polarization switching in the HZO layer—into synaptic weights of the ANN. The stable and analog-like conductance modulation enabled by ferroelectric polarization ensured reliable multilevel weight programming, while the non-volatile polarization states guaranteed retention of the trained weights. In this way, ferroelectric polarization directly supported the essential requirements of synaptic learning and classification in the ANN framework.

Nevertheless, we recognize that this initial ANN demonstration, while illustrative, did not fully capture the unique polarization-sensitive functionality of ReS_2. In response to the reviewer's suggestion, we have therefore added a new CNN-based demonstration of

butterfly recognition under polarized light (**Fig. R6**). This task was implemented on our experimentally fabricated small-scale FeFET array, thereby directly linking the intrinsic anisotropic photoresponse of ReS_2 to polarization-resolved neuromorphic vision. This new example highlights how the polarization characteristics of the channel material can be exploited for bio-inspired sensing and pattern recognition.

In the revised manuscript, we now present two complementary demonstrations in the updated **Fig. 5** (**Fig. R7**):

- ANN under unpolarized light: illustrating how ferroelectric polarization provides robust and stable weight updates for general neuromorphic learning.
- CNN under polarized light: showing how the intrinsic polarization sensitivity of ReS_2 enables polarization-resolved visual recognition.

By combining these two aspects into a unified "dome-shaped" framework in **Fig. R7**, we demonstrate that our FeFET platform integrates both ferroelectric polarization–driven synaptic weight modulation and polarization-sensitive optoelectronic sensing. To our knowledge, this represents the first demonstration that bridges these two functionalities within a single device–application system, thereby expanding the scope of ferroelectric optoelectronic synapses toward polarization-resolved vision.

[FIGURE REDACTED]

Fig. R5. ANN simulation for iris flower recognition based on ReS_2 FeFET synaptic characteristics.

[FIGURE REDACTED]

Fig. R6. CNN-based image processing with the FeFET array, where butterfly features are extracted under horizontal, vertical, and sharpening filters, and the combined polarization-resolved outputs enhance orientation contrast and enable reliable recognition.

[FIGURE REDACTED]

Fig. R7. Neuromorphic vision demonstrations based on ReS_2 MFMIS FeFETs. (**a**) Schematic illustration of polarization-dependent natural light and its role in biological recognition. (**b**) Device-level synaptic characteristics under electrical and optical stimuli. (**c**) ANN simulation for iris flower recognition under unpolarized light. (**d**) CNN-based convolution simulation for butterfly recognition under polarized light.

Reviewer #5

Optical performance of ReS_2 FeFET is very impressive. I would suggest following clarifications to make what is based on real experiment or not.

Our response:

We sincerely thank the reviewer for the positive comments on the optical performance of our ReS_2 FeFET and for highlighting the importance of clarifying what results are based on experiments and what are obtained from simulations.

To provide clarity, we specify the sources of each result as follows: Fig.s 4b–i are measured experimental results, while Fig. 4j is a simulation derived directly from the experimental data in Fig. 4i. In Fig. 5, panel (a) is a schematic illustration, panel (b) includes experimentally measured device performance (electrical LTP, optically modulated LTD, and the I_{DS}–V_{GS} characteristics of nine devices in a 3×3 array), and panels (c) and (d) present ANN and CNN simulations for iris and butterfly recognition, respectively, both parameterized using the experimentally obtained device characteristics. We hope this clarification makes clear which results are based on direct experiments and which are simulations grounded in experimental data.

Comment #1:

Even Figure 1c shows device using very small ReS_2 crystal piece, but the next figure is a schematic of large array. Is this array actually fabricated?

Our response:

We sincerely thank the reviewer for this thoughtful comment and for the opportunity to clarify. We understand the concern that the original **Fig. 1c** only showed a single device, while the following schematic illustrated an array, which may have caused ambiguity. To address this, in the revised manuscript we have replaced Fig. 1c with the optical micrograph of a fabricated **3×3 ReS_2 FeFET array**, so that the presented data directly reflects an experimentally realized array structure.

We also acknowledge that the fabrication of large-scale arrays would require mature wafer-scale ReS_2 growth and more advanced integration techniques, which are important directions for the field but not yet within the scope of the present study. Our primary goal here is to establish and validate the ferroelectric MFMIS device concept and its optoelectronic synaptic functionality.

To nevertheless provide supporting evidence for array-level feasibility, we have fabricated a small 3×3 array using a sequence of standard microfabrication steps (**Fig.R1**). First, the ReS_2 flake was mechanically exfoliated onto the pre-deposited $Si/SiO_2/W/HZOW/HfO_2$ gate stack. The flake was then patterned by photolithography and etched to define the device array and isolate individual channels. Following this, source and drain electrodes were formed through lithographic alignment and metal deposition, enabling independent addressing of all nine devices. After lift-off and cleaning, the completed array was electrically characterized to confirm device-to-device uniformity and reproducibility (**Fig. R2**).

The successful operation of this array, together with its application demonstration (now included in the revised **Fig. 5**), shows that our device concept can indeed be extended beyond single-device studies and provides a first step toward future neuromorphic applications.

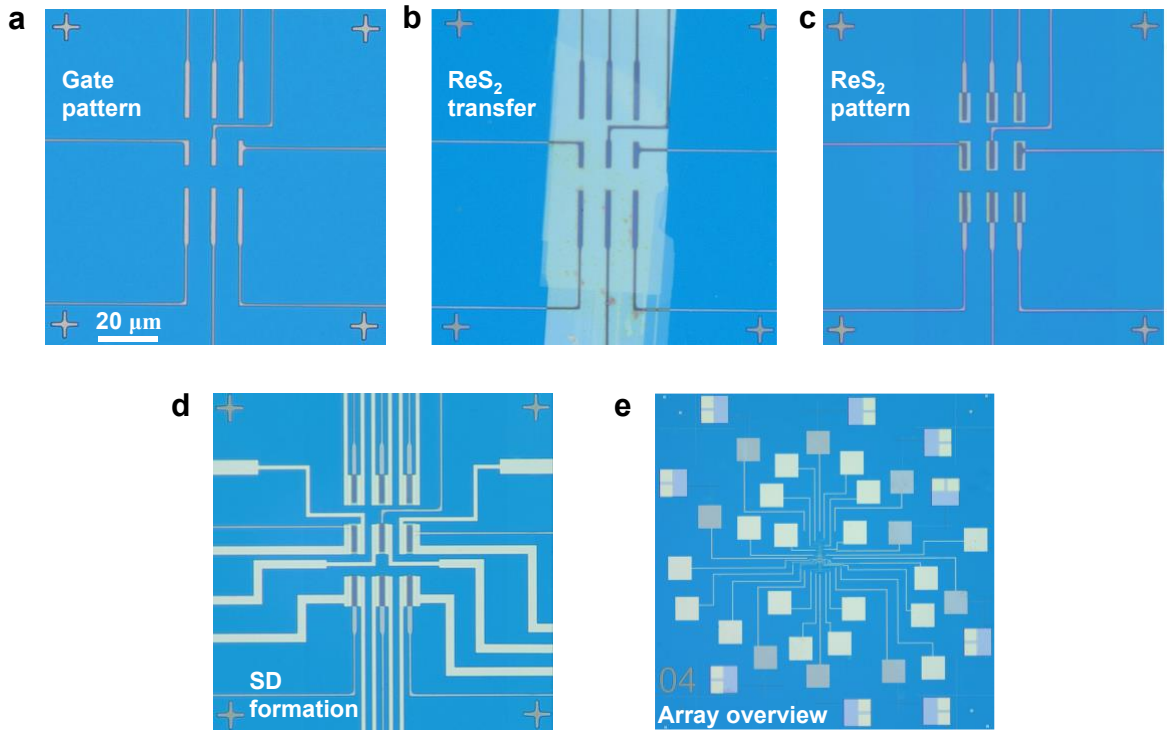


Fig. R1. Fabrication process of the ReS_2 FeFET array. (**a**) Gate electrode patterning on the substrate. (**b**) Transfer of a relatively large-area ReS_2 flake onto the predefined gate region. (**c**) Lithographic definition and etching of the ReS_2 channel patterns. (**d**) Formation of source/drain (S/D) electrodes to complete the device structure. (**e**) Optical micrograph of the fabricated 3×3 ReS_2 FeFET array, showing the overall layout.

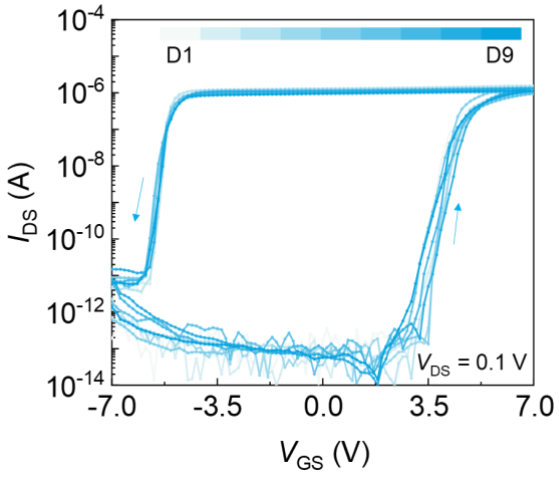


Fig. R2. I_{DS}-V_{GS} characteristics of nine devices from the fabricated 3×3 ReS_2 FeFET array, showing uniform ferroelectric switching and well-defined hysteresis, confirming array-level feasibility.

Comment #2：

Fig.4. Fig.5 assumes large array operation, but it doesn't look like the authors made actual array.

Our response:

We sincerely thank the reviewer for raising this important point and for the opportunity to clarify. We acknowledge that our work does not yet demonstrate large-scale circuit implementation, as this would require mature wafer-scale ReS_2 growth and advanced integration technologies that are still under development in the field. Instead, in this study our aim is to establish the fundamental device concept and provide initial array-level evidence. Accordingly, we fabricated a small 3×3 ReS_2 FeFET array, which, although limited in scale, offers concrete experimental support for the feasibility of extending our approach beyond single devices. In the revised manuscript, we have updated Fig. 5 to incorporate results based on this array, thereby ensuring that the discussion is closely aligned with experimentally realized structures and application demonstrations.

Regarding Fig. 4

Figs. 4a–i are all experimentally measured results from individual ReS_2 FeFET devices. In particular, Fig. 4j is not based on an assumed large array, but rather is a simulation directly derived from the polarization-resolved photocurrent data shown in Fig. 4i. The purpose of including this simulation was to provide a proof-of-concept illustration of how the intrinsic polarization sensitivity of ReS_2 could be exploited in practical vision-related applications. Specifically, the simulation highlights the potential of our device for suppressing glare at water surfaces, where the rejection of strongly polarized reflection is critical. We wish to emphasize that this example is intended only as an application-oriented demonstration grounded in our experimental data, and not as a claim of a fully realized system. Our main

focus remains on establishing the fundamental device characteristics, while the translation of such concepts into system-level implementation will be an important subject of future work.

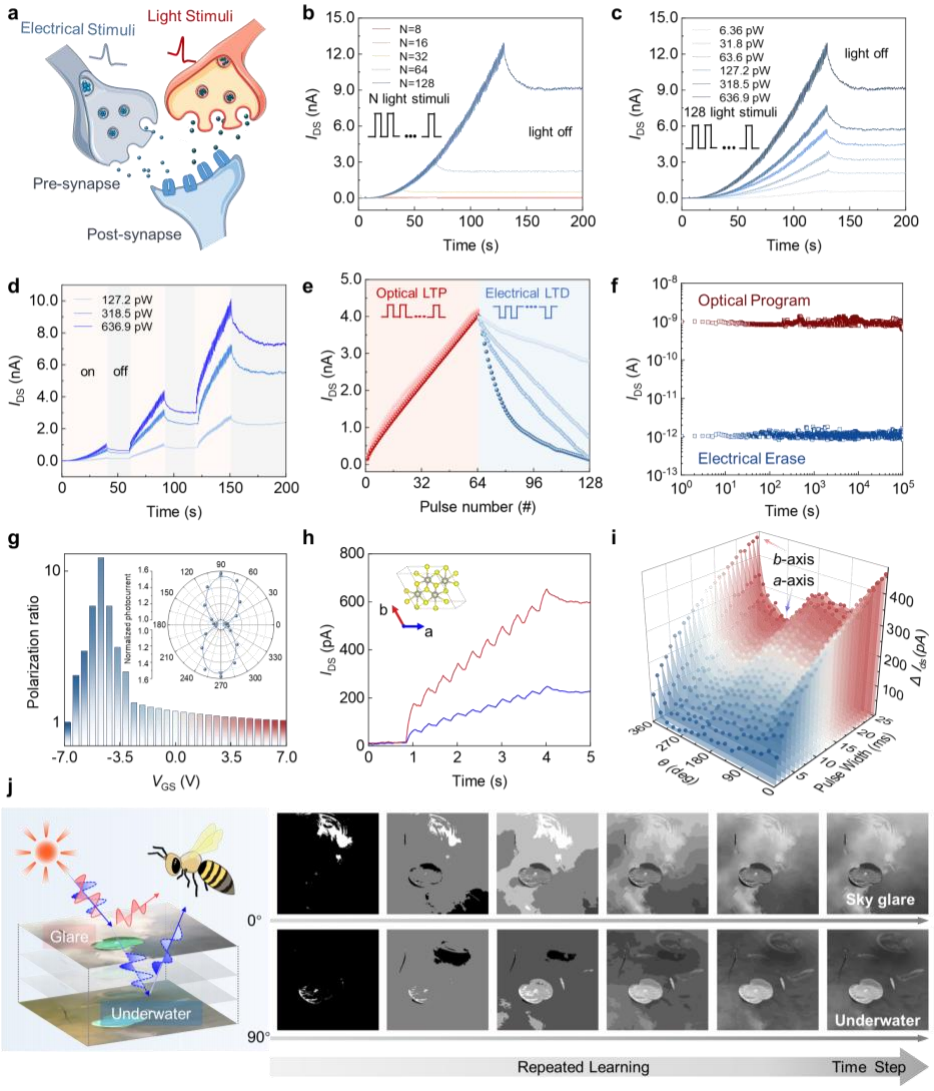


Fig. R3. xxx

Regarding Fig. 5

We have fabricated a 3×3 ReS_2 FeFET array, as shown in the revised **Fig. 5b**, to provide direct experimental support for array-level feasibility. The array was intentionally kept at a small scale, since realizing wafer-scale integration would require mature and

uniform CVD growth of ReS_2 together with advanced circuit integration, which are not yet fully established and therefore lie beyond the present scope of this work. Instead, for this study we adopted a reliable approach based on mechanical exfoliation of a relatively large-area ReS_2 flake, followed by lithographic patterning, etching, and source–drain electrode formation to define the nine-device array. Although this approach does not yet enable large-scale integration, it allows us to directly validate the extension of our device concept from single devices toward multi-device operation.

To further strengthen the link between our device characteristics and functional applications, we demonstrate two representative neuromorphic vision tasks. First, we employed the experimentally measured device characteristics to perform an ANN-based recognition of iris flowers under unpolarized light, highlighting the optoelectronic synaptic learning capability enabled by ferroelectric polarization–assisted weight modulation. Second, leveraging the fabricated array, we conducted a CNN-based convolution simulation for butterfly recognition under polarized light, which directly reflects the intrinsic polarization sensitivity of the ReS_2 channel.

Thus, these two demonstrations illustrate complementary aspects of our device: reliable synaptic weight programming under unpolarized optical inputs, and polarization-resolved pattern recognition enabled by the anisotropic ReS_2 channel. This dual demonstration provides a stronger connection between the physical properties of our ferroelectric MFMIS FeFETs and application-level neuromorphic vision, while the fabricated array offers concrete experimental validation that the concept can indeed be extended beyond single devices. Looking ahead, we believe that continued progress in large-area CVD growth of ReS_2 and integration technologies will make it possible to scale this concept toward wafer-level arrays, ultimately paving the way for practical polarization-sensitive neuromorphic hardware.

[FIGURE REDACTED]

Fig. R4. Neuromorphic vision demonstrations based on ReS_2 MFMIS FeFETs. (**a**) Schematic illustration of polarization-dependent natural light and its role in biological recognition. (**b**) Device-level synaptic characteristics under electrical and optical stimuli. (**c**) ANN simulation for iris flower recognition under unpolarized light. (**d**) CNN-based convolution simulation for butterfly recognition under polarized light.

Comment #3:

The authors should include the time scale discussion on the operation mechanism whether the current speed of sensing and programming is suitable for the operation/ image sensing claimed by the authors.

Our response:

We thank the reviewer for the helpful suggestion. We agree that discussing the time scale of operation is essential for evaluating the practicality of our proposed applications. Below we provide a detailed clarification for both the ANN and CNN scenarios.

ANN simulation (unpolarized vision task)

In the ANN-based demonstration, inputs and outputs are handled electrically, and the training process relies on weight updates driven by electrical and optical pulses. From our experimental characterization (**Fig. R5**, showing the electrical operation speed under programming pulses with widths ranging from 100 μs to 100 ms), the minimum pulse width that can reliably induce a stable conductance change is about 100 μs. This update time defines the temporal resolution of weight programming. Once the training is completed, however, the ferroelectric polarization ensures long-term retention of the programmed states without the need for continuous refreshing. As a result, the inference stage, in which the network is used for classification, operates at a speed limited only by signal encoding and data transfer in the peripheral circuitry rather than by the intrinsic device dynamics. In other words, the intrinsic device speed mainly governs the training phase, whereas the inference phase can proceed at much higher effective rates. This behavior is consistent with the operation of biological synapses, where learning occurs more slowly than recall.

CNN scenario (polarization-sensitive vision task)

In the CNN-based demonstration, where sensing and computing are integrated within the FeFET array, the operation speed is primarily constrained by the optical sensing step. Our measurements (**Fig. R6**, showing the optical operation speed under light stimulation with pulse widths ranging from 200 μs to 100 ms) indicate that the minimum usable optical pulse width is about 200 μs, which sets the timescale for one convolutional operation per layer. For tasks such as polarization-resolved butterfly recognition, this timescale is sufficiently fast to capture static or slowly varying optical scenes, such as images or frames

in neuromorphic vision systems. While the device response is not yet in the nanosecond range of conventional CMOS photodetectors, it is already well matched to bio-inspired vision tasks, where temporal integration over hundreds of microseconds can be advantageous for noise suppression and reliable pattern recognition.

These results confirm that the demonstrated device dynamics (100 μs for electrical programming and 200 μs for optical sensing) provide a practical and sufficient timescale to support the neuromorphic and image-sensing applications targeted in this study. The current programming and sensing speeds are adequate for proof-of-concept demonstrations of both ANN- and CNN-based vision tasks. Looking forward, further optimization of ferroelectric switching dynamics and optical coupling strategies could reduce the effective pulse width below the present 100–200 μs limit, paving the way toward faster and more scalable neuromorphic hardware.

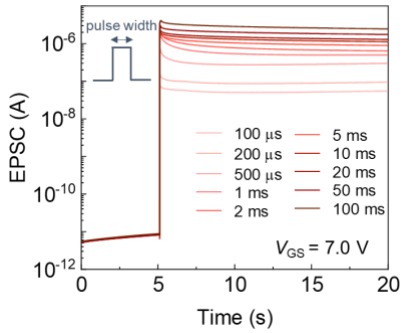


Fig. R5. Electrical operation speed of the ReS_2 FeFET under programming pulses with widths ranging from 100 μs to 100 ms.

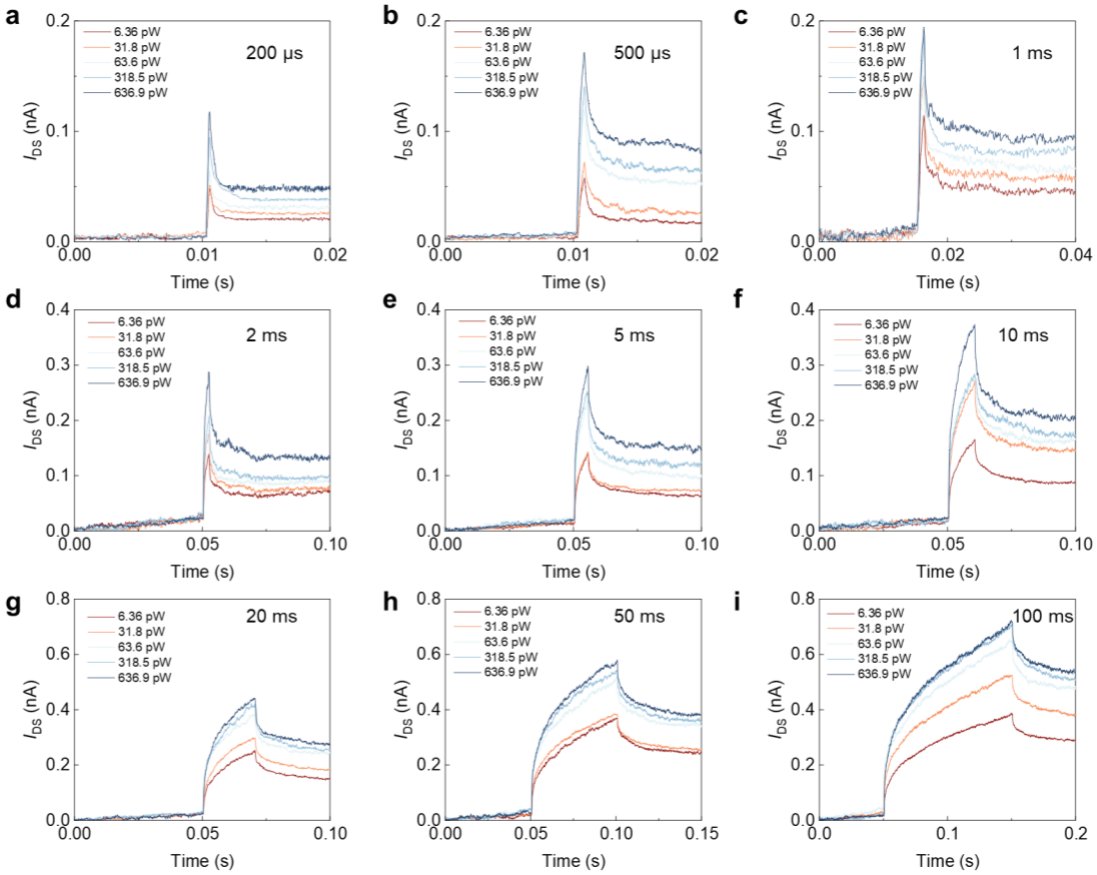


Fig. R6. Optical operation speed of the ReS_2 FeFET under light stimulation with pulse widths ranging from 200 µs to 100 ms.

Dear Editor,

The manuscript has been carefully revised according to the reviewers' comments and the editorial requests. All changes have been incorporated into the revised manuscript and are highlighted in yellow. The point-by-point responses to the reviewers' comments are provided below.

========== Authors' responses to the reviewer's comments ==========

Reviewer #2

Although the authors have made efforts to address prior reviewer feedback, their revisions remain inadequate. The most critical weakness—the lack of sufficient novelty—has not been resolved. In addition, many of their responses are vague, unconvincing, or insufficiently detailed, leaving key concerns unaddressed. This lack of clarity undermines confidence in the robustness of the study and reinforces the earlier conclusion that the manuscript does not meet the standards required for publication.

Moreover, the study relies solely on a single unit device for computing, rather than demonstrating an array configuration as indicated in Figure 5b. Devices fabricated with small flakes inherently suffer from non-uniformity, instability, and poor reliability. Without presenting an array of ReS_2 devices with consistent and reproducible characteristics, the work fails to convincingly demonstrate realistic functionality or scalability. This omission substantially weakens the practical relevance and impact of the reported results.

Our response：

We thank the reviewer for the comment. As shown in our previous submission, a 3×3 ReS_2 FeFET array with experimentally validated uniform switching behavior was already provided. In the revised manuscript, we have now explicitly highlighted the reproducible switching performance of the crossbar devices, underscoring the excellent uniformity achieved across the array.

Using EBL patterning and dry-etch processes, we accurately defined the channel sizes and achieved highly consistent flake geometry. Importantly, the array consists of nine independently patterned ReS_2 channels rather than variations within a single flake. Electrical measurements further confirm uniform device behavior across all nine cells. Electrical characterization further reveals uniform I_{DS}–V_{GS} switching behavior across all nine devices, with narrow distributions in I_{ON}, I_{OFF}, V_{th+}/V_{th-}, I_{ON}/I_{OFF} ratio, and MW. These results confirm excellent device-to-device consistency and robust ferroelectric switching performance at the array level.

These results have been added to the revised manuscript to address the concerns regarding scalability and reproducibility.

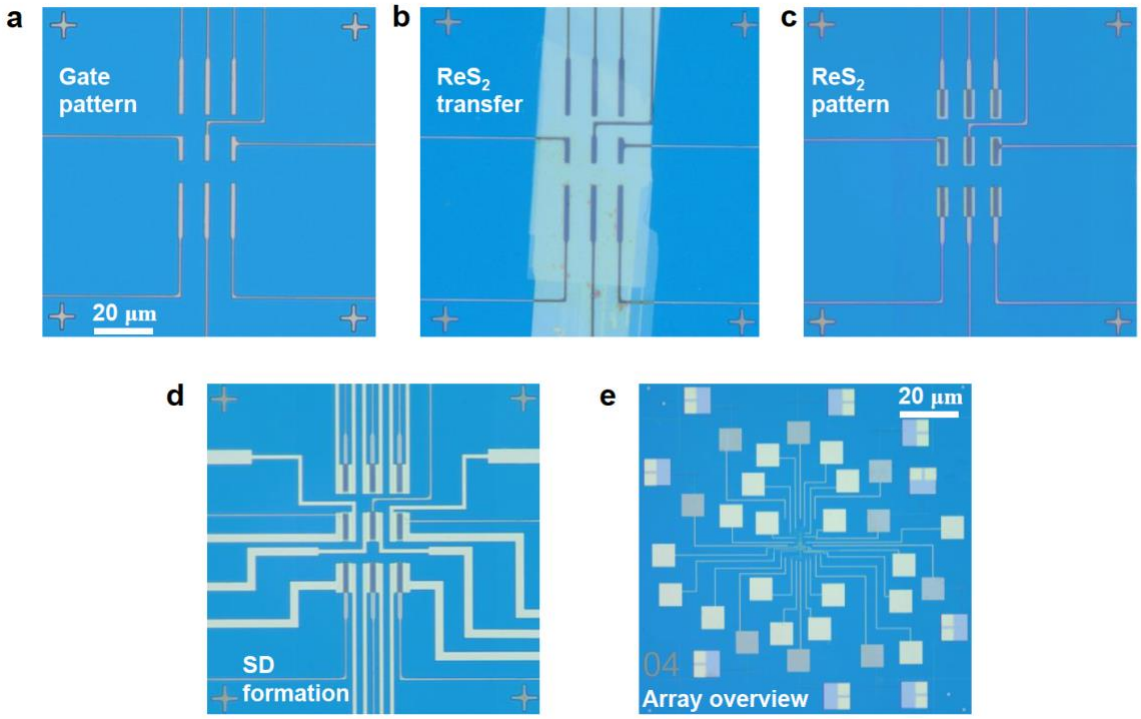


Fig. R1. Fabrication process of the ReS_2 FeFET array. a. Gate electrode patterning on the substrate. **b.** Transfer of a relatively large-area ReS_2 flake onto the predefined gate region. **c.** Lithographic definition and etching of the ReS_2 channel patterns. **d.** Formation of source/drain (S/D) electrodes to complete the device structure. **e.** Optical micrograph of the fabricated 3×3 ReS_2 FeFET array, showing the overall layout.

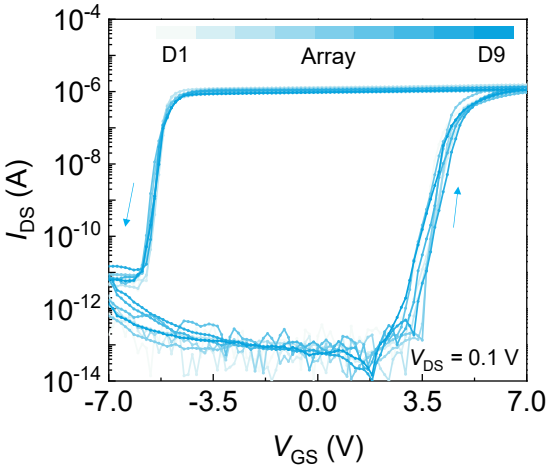


Fig. R2. Transfer characteristics (I_{DS}–V_{GS}) of the 3×3 ReS_2 MFMIS FeFET array measured at V_{DS}=0.1 V. All nine devices show uniform threshold voltages (V_{th}), consistent ON/OFF ratios (I_{ON}/I_{OFF}), and stable bidirectional switching, demonstrating good device-to-device uniformity across the array.

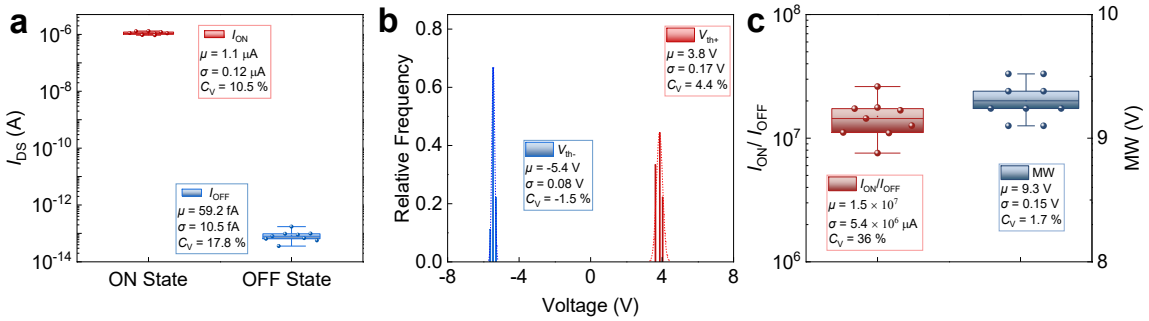


Fig. R3. Statistical evaluation of the 3×3 ReS_2 MFMIS FeFET array. a. ON-state and OFF-state I_{DS} distributions, showing clearly separated current levels with low variation among devices. **b.** Distributions of the positive and negative threshold voltages (V_{th+} and V_{th-}), illustrating narrow spreads and consistent switching characteristics across the array. **c.** Summary of the I_{ON}/I_{OFF} ratios and memory windows (MW), both exhibiting high uniformity and small coefficients of variation, confirming reliable ferroelectric memory behavior for all nine devices.

Corresponding change:

Page: 21, S-24

Figure: Supplementary Figure 30

Reviewer #4

It has been well revised, and can be accepted.

Our response:

We sincerely appreciate the positive and supportive comment.

Reviewer #5

The authors clarified many concerns and revised manuscript to restrict the application to neuromorphic vision applications. I am not fully convinced what is the role of neuromorphic vision processing whose speed is limited to ~ KHz operation. Yet, I think this manuscript has enough novelty for the publication.

Our response:

We sincerely appreciate the constructive comment and the positive evaluation.