Supplementary Information:

Monolithic integration of p- and n-type doped 2D WSe2 for wafer scale complementary logic circuits

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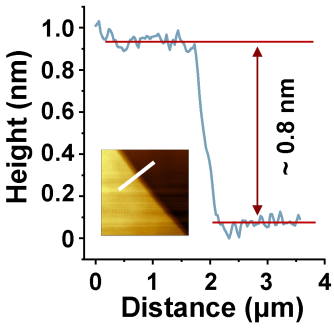
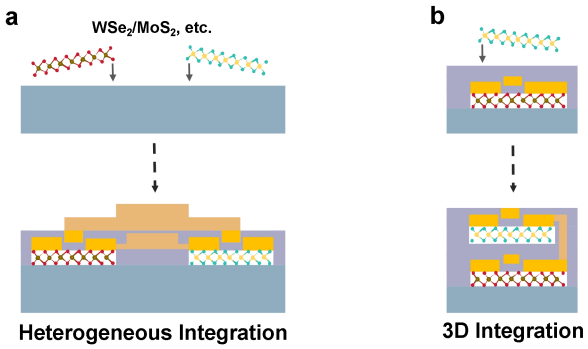
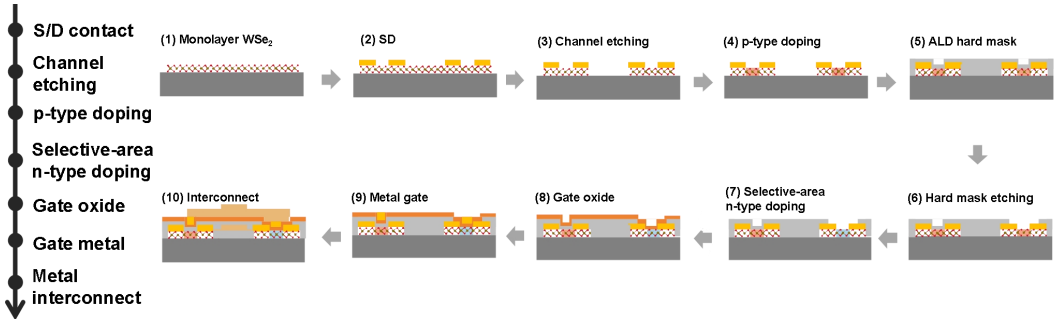


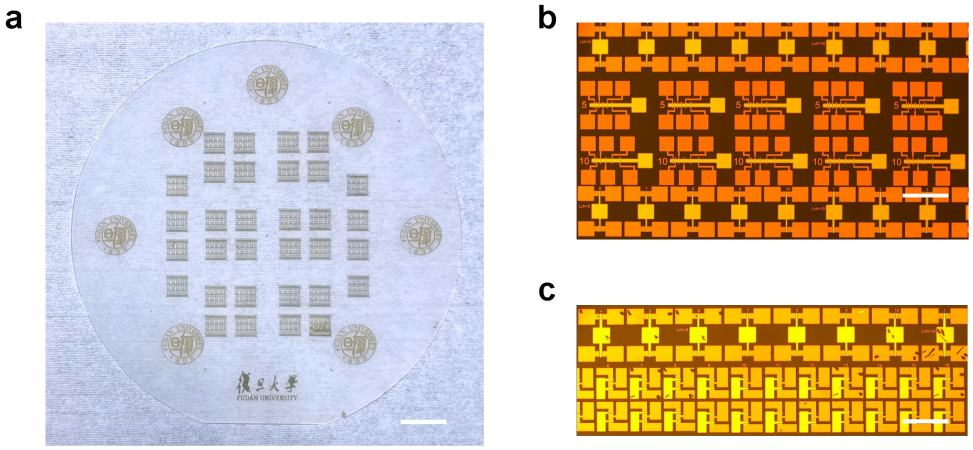
Supplementary Fig. 1. AFM image of monolayer WSe_2 film with measured thickness of ~ 0.8 nm.



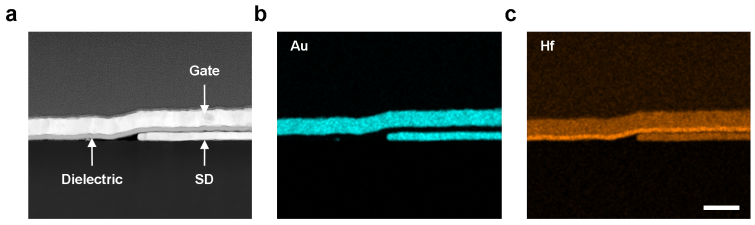
Supplementary Fig. 2. Two mainstream approaches to fabricate 2D CMOS, planar heterogeneous integration (a) and 3D integration (b). Both approaches require the transfer of distinct 2D materials, such as n-type (e.g., MoS_2) and p-type (e.g., WSe_2 or $MoTe_2$) channel materials.



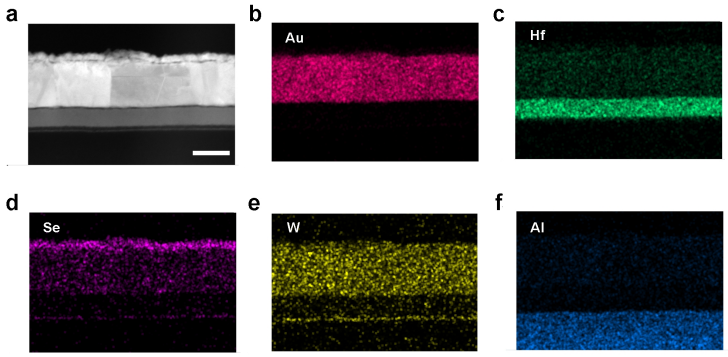
Supplementary Fig. 3. Fabrication process flow of WSe_2 transistors and CMOS inverters. The processes include growth of WSe_2 thin film, deposition of source/drain electrodes, channel isolation and etching, p-doping, ALD deposition of hard mask layer, etching of hard mask layer, selective-area n-doping, ALD deposition of top-gate dielectric, fabrication of top gate electrodes, and deposition of interconnect layers.



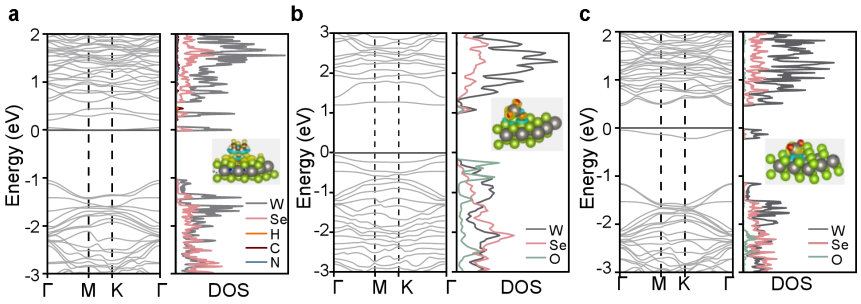
Supplementary Fig. 4. a, Photograph of a 4-inch wafer, with a scale bar of 1 cm. b, c, Optical microscope images of device arrays, with a scale bar of 300 μm.



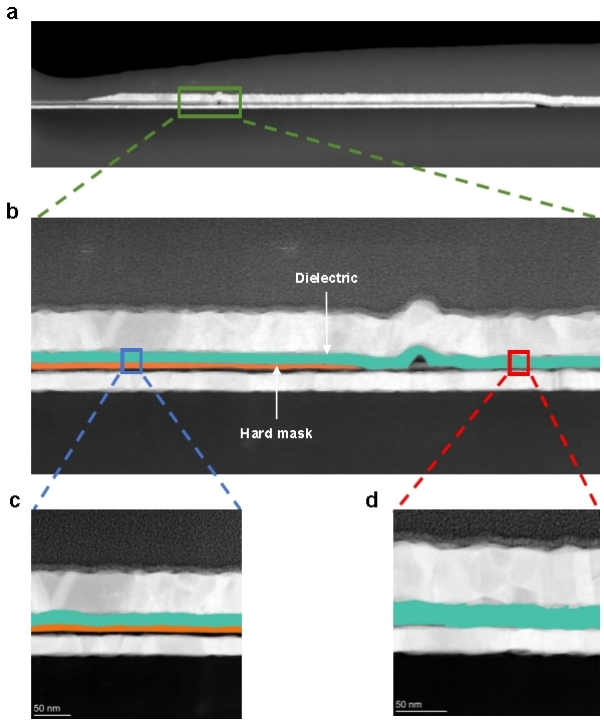
Supplementary Fig. 5. Cross-sectional TEM image of WSe_2 FET source/drain region and the corresponding EDS mapping. Scale bar: 50 nm.



Supplementary Fig. 6. Cross-sectional TEM image of WSe_2 FET gate stack region and the corresponding EDS mapping. Scale bar: 50 nm.

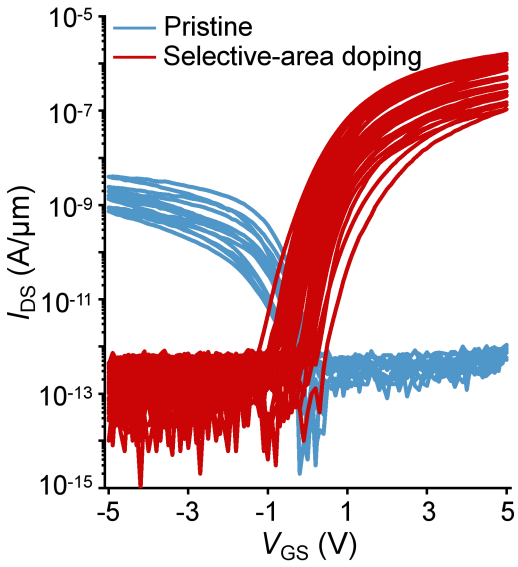


Supplementary Fig. 7. Theoretical calculations of n- and p-doping mechanisms. a, Density of states (DOS) versus energy level for WSe_2 with a $N(CH_3)_4$ group adsorbed at a Se vacancy site. Inset shows the charge transfer diagram (gray, W; green, Se; brown, C; orange, H; blue: N), illustrating electron accumulation in WSe_2 and charge depletion from the $N(CH_3)_4$ group. b, DOS profile of WO_4 group adsorbed on WSe_2. Inset shows charge transfer diagram (gray, W; green: Se; red: O) demonstrating charge depletion from WSe_2 to WO_4 group. c, DOS analysis of WO_3 group adsorbed WSe_2 at a Se vacancy. Inset shows charge transfer diagram (gray, W; green, Se; red, O) showing electron transfer from WSe_2 to WO_3 group.

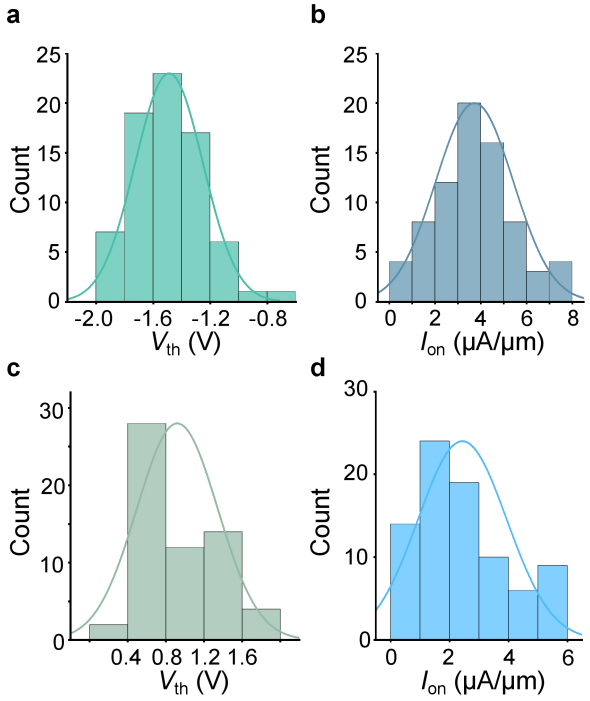


Supplementary Fig. 8. Cross-sectional TEM image of the bilayer hard mask for selective-area n-doping. a. Cross-sectional TEM image of the full bilayer hard mask structure at source/drain region. b. Magnified view of the boxed region in a, highlighting intact bilayer mask (blue-dashed) and etched mask regions (red-dashed). c.TEM image of the bilayer hard mask and gate dielectric (blue-dashed area in b). d.

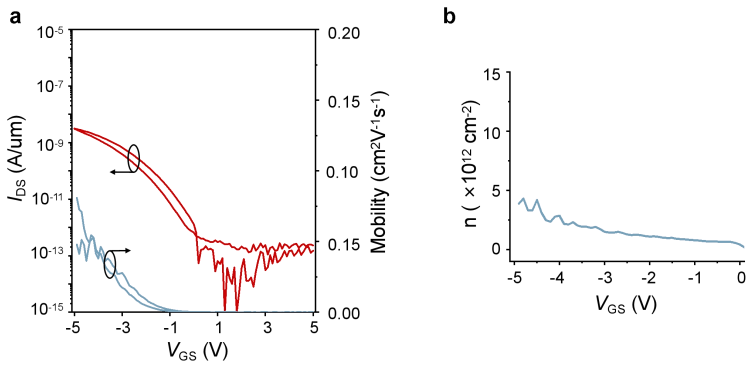
TEM image of the gate dielectric at the etched mask regions within red-dashed region in b, showing complete removal of hard mask layers. Scale bars: 50 nm.



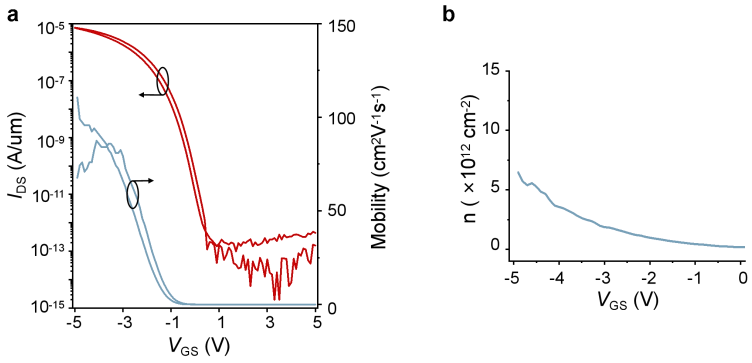
Supplementary Fig. 9. Transfer characteristics of pristine and selective-area n-doped WSe_2 transistors. The pristine WSe_2 transistors exhibit p-type behavior, while the transistors in the selective-area n-doping regions transform from p-type to n-type electrical characteristics.



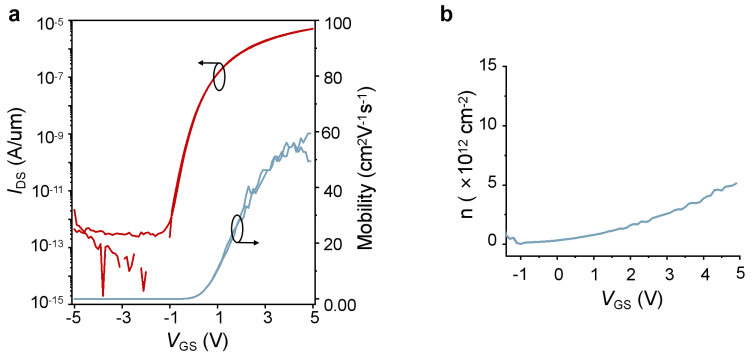
Supplementary Fig. 10. Statistical distribution of threshold voltage and on-state current of approximately 70 PMOS and 70 NMOS devices. a, b, Statistical distribution of PMOS. c, d, Statistical distribution of NMOS.



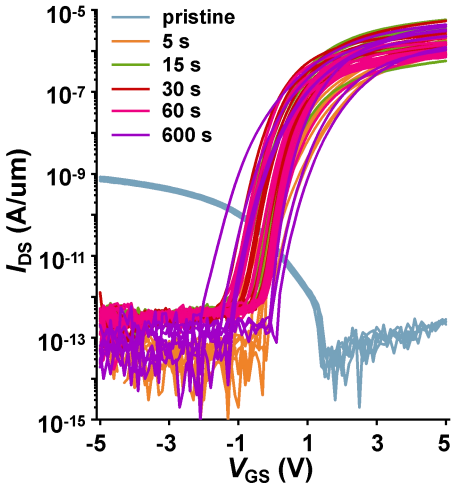
Supplementary Fig. 11. Transfer characteristics, carrier mobility, and carrier concentration of a typical pristine WSe_2 transistor. a. Transfer characteristics and field-effect mobility of pristine WSe_2 transistor. b. Carrier concentrations of WSe_2 FET channel region under different gate voltages.



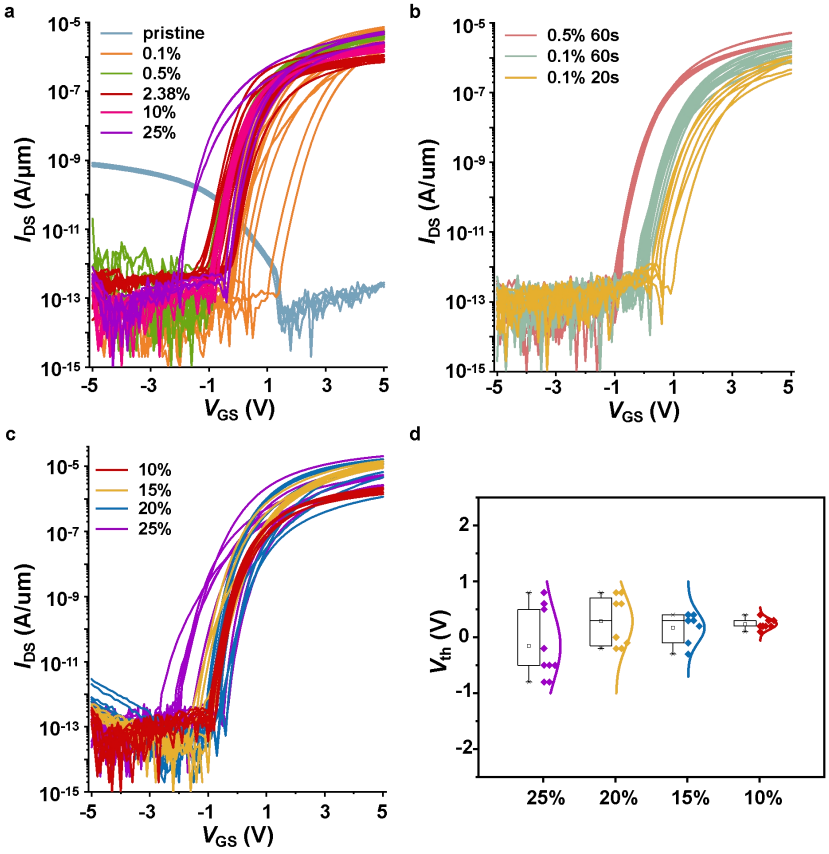
Supplementary Fig. 12. Transfer characteristics, carrier mobility, and carrier concentration of p-doped WSe_2 transistor. a. Transfer characteristics and field-effect mobility of p-doped WSe_2 transistor. b. Carrier concentrations under different gate voltages. Compared to pristine WSe_2 transistors, the on-state current increased by approximately three orders of magnitude (10^3 times), the carrier mobility reaches ~ 100 $cm^2\ V^{-1}\ s^{-1}$, and the hole concentration in the channel is enhanced by ~ 50% under the same gate voltage.



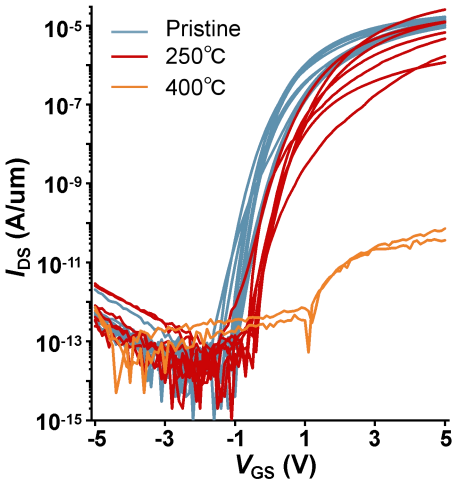
Supplementary Fig. 13. Transfer characteristics, carrier mobility, and carrier concentration of n-doped WSe_2 transistor. a. Transfer characteristics and field-effect mobility of p-doped WSe_2 transistors. b. Carrier concentrations under different gate voltages. Compared to pristine WSe_2 transistor, it exhibits n-type transistor behavior, with the on-state current increasing by approximately three orders of magnitude (10^3 times), an electron mobility of ~ 60 $cm^2V^{-1}s^{-1}$, and an electron concentration reaching 5×10^{12} cm^{-2} at gate voltage of 5 V.



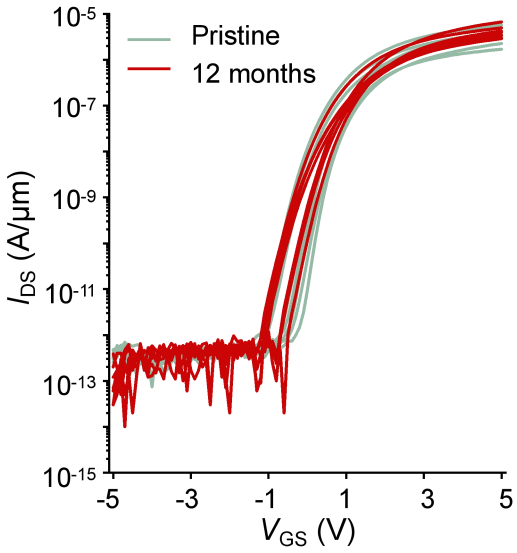
Supplementary Fig. 14. Transfer characteristics of n-type doped WSe_2 FETs treated with 5-600 s. The pristine WSe_2 transistors exhibit p-type behavior, while the n-doped WSe_2 transistors display fully n-type transfer characteristics. The electrical characteristics of 47 WSe_2 transistors, such as threshold voltage and on-state current, keep stable when the doping treatment duration varies from 5 s to 600 s, which indicates WSe_2 is highly sensitive to the n-type dopant and can be fully n-doped.



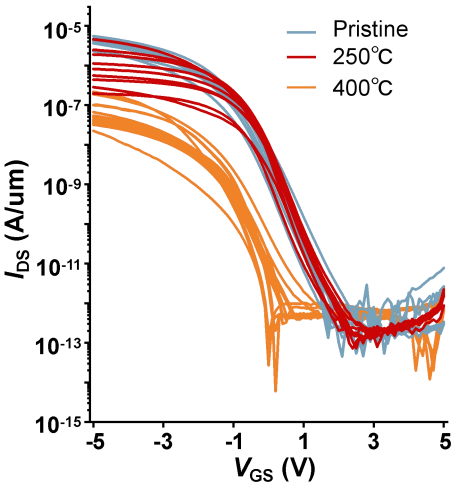
Supplementary Fig. 15. a, Transfer characteristics of n-type doped WSe_2 transistors treated with 0.1%-25 wt% TMAH solution. b, Transfer characteristics of WSe_2 transistors treated with lower concentration solution and shorter doping time. The pristine WSe_2 transistors exhibit fully p-type behavior, while the n-doped WSe_2 transistors display fully n-type transfer characteristics. The electrical characteristics of 40 WSe_2 transistors, such as threshold voltage and on-state current, remain stable when the concentration varies from 0.5 wt% to 10 wt %. Under the concentration of 0.1 wt%, the threshold voltage shift slight positively. Notably, under the concentration of 25 wt%, significant variability is observed. c, Transfer characteristics of WSe_2 transistors treated with high concentration of 10-25 wt% TMAH solution. d, Boxplots with Gaussian fitting of V_{th}.



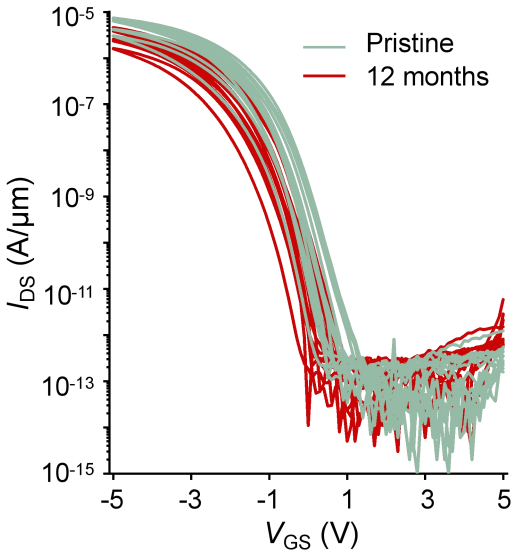
Supplementary Fig. 16. Thermal stability of the n-type doping process. The transfer characteristics of 10 n-doped WSe_2 transistors which were annealed in a tube furnace under Ar atmosphere at 250℃ or 400℃ for 1 hour.



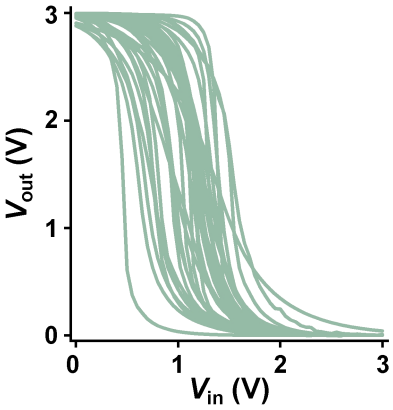
Supplementary Fig. 17. Long-term stability of the n-type doping process. The transfer characteristics of nine n-type WSe_2 transistors which were stored in a glovebox for 12 months, show good consistency with pristine device. The threshold voltage and on-state current, remain largely unchanged, which indicates that the doping process exhibits good long-term stability.



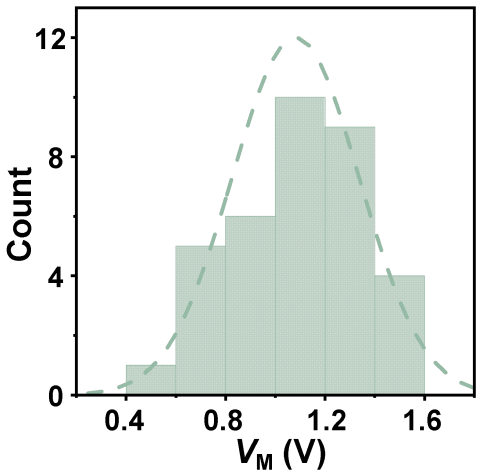
Supplementary Fig. 18. Thermal stability of the p-type doping process. The transfer characteristics of p-type WSe_2 transistors which were annealed in a tube furnace under Ar atmosphere at 250°C (9 transistors) or 400°C (12 transistors) for 1 hour.



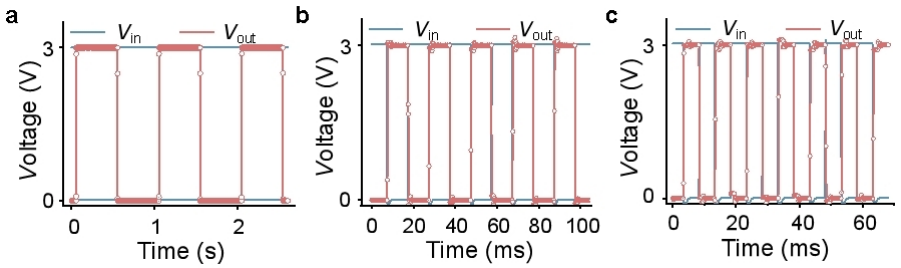
Supplementary Fig. 19. Long-term stability of the p-type doping process. The transfer characteristics of eight n-type WSe_2 transistors which were stored in a glovebox for 12 months, showing good consistency with pristine devices. Threshold voltage and on-state current, remain largely unchanged. This also indicates that the p-doping process exhibits a good long-term stability.



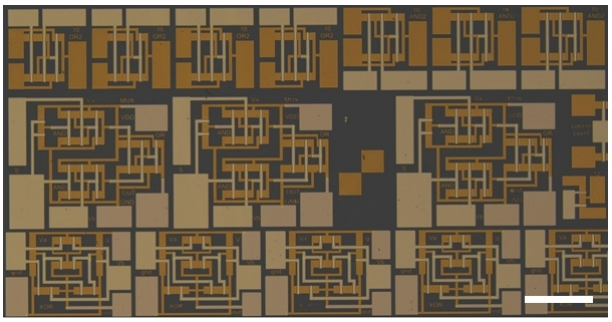
Supplementary Fig. 20. Yield and uniformity of 35 WSe_2 CMOS inverters. The voltage transfer characteristics of 35 randomly selected CMOS inverters, demonstrates a high yield.



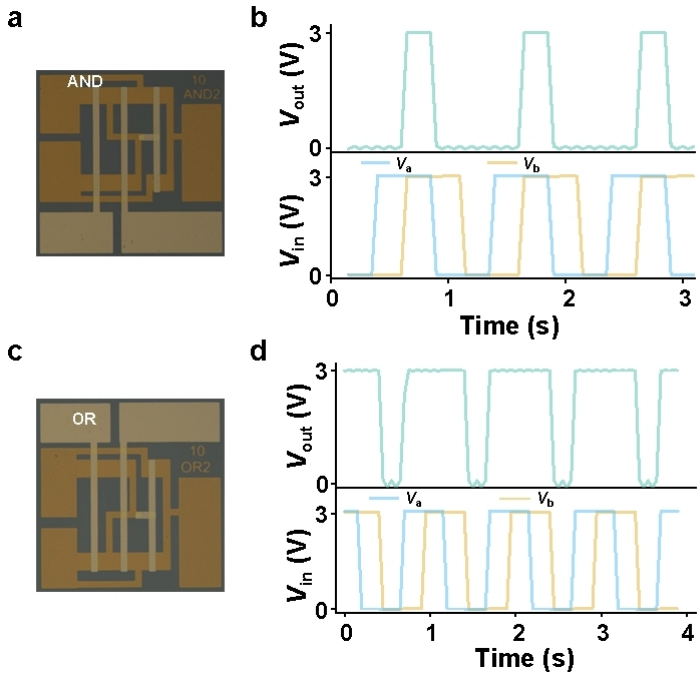
Supplementary Fig. 21. Statistical distribution of switching voltages of 35 CMOS inverters. The histogram of switching voltages for statistically sampled CMOS inverters shows a central tendency ~ 1.1 V.



Supplementary Fig. 22. Temporal response characteristics of the CMOS inverter. a-c, The dynamic output characteristics of CMOS inverters at frequencies of 1, 50 and 100 Hz, respectively.



Supplementary Fig. 23. Optical microscope image of CMOS circuit arrays. Scale bar, 200 μm.



Supplementary Fig. 24. Temporal response characteristics of AND and OR logic gates. a, The optical microscope image of AND logic gate. b, The temporal response of AND logic gate at 1 Hz operational frequency, which displays correct response. c, The optical microscope image of OR logic gate. d, The temporal response of OR logic gate at 1 Hz operational frequency, which shows correct output.

Supplementary Table 1. Comparison of TMDs-based CMOS inverter with previous literature.

Ref.	Voltage gain	Static power	Norise margin	Homogeneity	Scalability
this work	200@2V	tens of pW	~ 90@2V	good	4 inch
Ref. 6	18@3V	a few pW	~ 80@2V	bad	Ex.
Ref. 28	5@2V	tens of pW	~ 83@3V	bad	Ex.
Ref. 29	90@2V	tens of pW	~ 90@2V	bad	Ex.
Ref. 30	80@3V	tens of pW	~ 75@3V	good	2 inch