nature portfolio

Peer Review File

Monolithic integration of p- and n-type doped 2D WSe2 for wafer-scale complementary logic circuits

Corresponding Author: Professor Wenzhong Bao

This file contains all reviewer reports in order by version, followed by all author rebuttals in order by version.

Version 0:

Reviewer comments:

Reviewer #1

(Remarks to the Author)
This article demonstrates CMOS technology using WSe2 homogeneous channels, achieving p- and n-type doping of WSe2 through adsorption doping, and further realizing CMOS circuit modules with top-gate structures. This homogeneous technology is valuable for implementing 2D integrated circuits, as current 2D CMOS mostly uses heterogeneous channels. However, this paper contains excessive claims in many descriptions and has some obvious technical flaws. Before considering acceptance, I believe the following issues need to be addressed:
1. The authors claim "wafer scale" or "large-scale" in the abstract and title, yet the discussion about "wafer scale" in this paper is very limited, with only Raman characterization of materials. The key aspects of this work—whether it's the doping technology or circuit units—lack analysis of wafer-level yield and variability distribution. Furthermore, I believe the current circuit unit modules cannot be called large-scale. Just as merely having device repeating unit arrays without substantial electrical interconnections cannot be called large-scale integrated circuits.
2. The authors claim "novel silicon-compatible doping methods," but both "novel" and "silicon-compatible" are difficult to define. As a high-level scientific paper, such expressions should be avoided. Moreover, silicon processes typically do not use solution etching, and the dopant materials in this paper need verification. Additionally, since the circuits in this paper are fabricated on sapphire substrates, the necessity of "silicon-compatible" is unclear.
3. The authors claim to "modulate carrier polarity and concentration for WSe2" and demonstrate polarity modulation in experiments, but there seems to be no systematic discussion about carrier concentration modulation. In the supplementary figures (S13, S14), the devices do not show significant dependence on concentration and doping time, which is likely masked by variation.
4. The high gain and low power consumption in the abstract are taken from different supply voltages. However, whether it's high gain at 5V or "low power consumption" at 2V, the key issue is that the operating voltage is too high, which does not match "next-generation" electronic devices and "low-power applications." The authors should demonstrate high performance of devices and circuits at voltages below 1V, including gain, power consumption, noise margin, etc. Performance at voltages as high as 5V has no practical value (Fig. 3c-d).
5. Regarding device size scalability: First, the channel length and width of devices throughout the paper are missing. Second, based on the scale bar in Fig. 1g, the channel length and width are on the order of several micrometers. Since the conclusions of this paper are based on long-channel devices, my key concern is whether effective doping can be achieved in short channels (sub-100 nm or even smaller dimensions). This part should be demonstrated to support the scalability benchmark in Fig. 3f.
6. Similarly, since the doping technology in this paper is still based on adsorption, I suspect that the performance variation of this technology in short channels and narrow channels is also a non-negligible challenge. Therefore, I recommend adding experiments in this part to clarify this issue.
7. Furthermore, since this is adsorption-based doping, will this method affect the electrical reliability of devices, such as PBTI/NBTI? The authors should supplement relevant experimental data.
8. The quality of Supplementary Fig. 3 is poor, affecting readability. Additionally, according to this process, are the dielectric thicknesses of PMOS and NMOS different? What is the actual gate dielectric of PMOS?
9. The electrical properties in Fig. 1h and Fig. 3 seem inconsistent. Fig. 1h clearly shows different threshold voltages. This may still be due to excessive variation.
10. Regarding image readability, the insets in Fig. 3a-c are too small.
11. Supplement Figure 1. Please double-check. The horizontal position of the edge of WSe2 corresponds to approximately 0.8 microns. I doubt the authenticity of the test data.

12. Supplementary Fig. 5a: There seems to be an air gap (about 30-50 nm) between the SD edge and the top gate dielectric? This could be a major challenge for device scaling.
13. Supplementary Figs. 10-11: How is the enhancement of carrier concentration calculated? The threshold voltage does not seem to change significantly.
14. Supplementary Figs. 13-18: Information about the number of devices is missing. Supplementary Figs. 13-14: The variation seems to increase after doping.
15. Supplementary Fig. 19: The description of yield with 20 devices is insufficient. Additionally, this figure does not demonstrate "rail-to-rail." Rail-to-rail refers to the input and output ranges being consistent.

Reviewer #2

(Remarks to the Author)
This manuscript presents a wafer-scale integration of homogeneous complementary metal-oxide-semiconductor (CMOS) circuits based on monolayer WSe_2, utilizing a bilayer hard mask process and charge transfer doping methods. By employing ammonium tungstate for p-type and TMAH for n-type doping, the authors demonstrate a practical approach to overcome the challenges of heterogeneous integration, realizing functional inverters with high voltage gain (396 V/V) and complex logic gates such as XOR and MUX. The demonstration of ultra-low static power consumption and the successful fabrication of logic arrays highlight the potential of this technology for next-generation low-power electronics. However, serious concerns remain regarding the fundamental stability of the doping mechanism and the integrity of the channel interface along with deep academic insights required for publication. These issues must be addressed to enhance the scientific reliability and practical scalability of the proposed technology.

COMMENT 1
The proposed doping mechanism relies on the surface adsorption of functional groups (WO_4 and $N(CH_3)_4$), which induce charge transfer to the WSe_2 channel. Since surface-adsorbed molecules are inherently susceptible to thermal desorption or migration, the provided stability data at 200 °C is insufficient to define the operational limits. The authors should identify the actual thermal failure point where the doping effect begins to degrade. By providing electrical data up to 400 °C, the authors should clearly define the thermal budget of their devices up to BEOL compatibility of the devices.

COMMENT 2
In Supplementary Fig. 14, hysteresis is observed when the TMAH concentration reaches 25%. This suggests that aggressive chemical treatment might induce interface traps or surface defects. Although the authors optimized the concentration to window, the physical origin of this hysteresis is not thoroughly discussed. The authors are encouraged to compare the interface trap density (Dit) of pristine and processed devices to quantitatively verify the surface integrity. A detailed discussion on the trade-off between doping efficiency and interface quality would provide valuable insights to the readers rather than just presenting the final optimized result.

COMMENT 3
The mechanism of n-type doping through TMAH treatment requires further clarification regarding its effect on the pre-existing p-doping. Since the entire WSe_2 channel is initially p-doped, the n-type regions must undergo a significant polarity inversion. While the DFT calculations in Supplementary Fig. 7 provide insights into the electronic states of $N(CH_3)_4$ groups, the manuscript does not explicitly discuss whether the TMAH treatment physically removes the p-type dopants or if the electron-donating effect of the $N(CH_3)_4$ groups simply overwhelm the previous carrier concentration. A clearer experimental or theoretical explanation of this mechanism would add significant depth to the discussion of the homogeneous integration process.

COMMENT 4
Figure 3f serves as a benchmarking figure but lacks legibility and a transparent representation of critical performance metrics. Specifically, while the authors claim to establish new performance standards, the benchmark plot omits operation frequency or switching speed, which are fundamental to logic circuit performance. Furthermore, the current visualization in Fig. 3f makes it difficult to quantitatively assess how the reported WSe_2 CMOS compares to recent state-of-the-art literature. The authors are encouraged to improve the clarity of Figure 3f and provide a detailed comparison table in the main text, including specific values for mobility, delay, and gain at comparable supply voltages to ensure an objective evaluation of the work. Typographical errors in the figure should be revised as well.

COMMENT 5
The authors utilized Au electrodes for both PMOS and NMOS devices. Could the authors clarify the reason behind using a single metal (Au) for both cases? It would be informative to know if other contact metals have been evaluated to improve the contact resistance for the n-type region. Additionally, there is a difference in the top-gate dielectric thickness between the p-type (~30 nm) and n-type (~20 nm) regions due to the bilayer hard mask process. The manuscript would benefit from including a discussion on how this structural asymmetry was considered in the device design and threshold voltage optimization.

Reviewer #3

(Remarks to the Author)
This study addresses the critical bottleneck issues in the field of two-dimensional (2D) semiconductors and proposes a novel CMOS-compatible p/n-type doping strategy. It has successfully realized a wafer-scale uniform array of WSe_2 top-gate CMOS circuits. The research demonstrates prominent innovation, a clear technical route, and comprehensive experimental

data. The fabricated WSe2 CMOS inverters exhibit outstanding metrics, which rank among the leading levels in the current 2D CMOS technology. Thereby providing a crucial solution for advancing the practical application of 2D semiconductors in low-power large-scale integrated circuits. It holds significant academic value and application potential.
The manuscript is suitable for publication after addressing the following minor issues:
1. The inverter exhibits optimal performance (e.g., highest gain) at a supply voltage of 5 V and minimal power consumption at 2 V; however, the logic gates operate at a supply voltage of 3 V. The authors should clarify the rationale behind this voltage selection.

2. The maximum operating frequency of the CMOS circuits reported in this work is 100 Hz. Can this frequency be further increased? The authors are suggested to discuss the factors that limit the switching frequency of the AND and OR gates in their revision.

3. In the device fabrication section, the function of the 2 nm SiO2 seeding layer should be clearly explained.

4. Given the excellent transistor and logic-gate performance and yield, the absence of larger-scale circuit demonstrations requires clarification. The authors should discuss the main challenges currently hindering the realization of large-scale integrated circuits based on this platform.

5. The thickness of the monolayer WSe2 should be indicated in Supplementary Figure 1 for clarity.

6. The notation “WO4” is potentially misleading. Since tungsten has a valence state of +6, it would be more accurate to use “(WO4)2-” to avoid misunderstanding.

7. Several minor grammatical and typographical issues should be corrected. For example, in line 32, “IC” should be revised to “ICs,” and in line 75, “a positive” should be capitalized to “A positive” at the beginning of the sentence.

Version 1:

Reviewer comments:

Reviewer #1

(Remarks to the Author)
The authors’ responses and the revised manuscript have been carefully evaluated. Although efforts have been made to provide additional data, clarify statements, and address part of the concerns raised, leading to an overall improvement in manuscript quality, the scalability of the doping strategy and the variability it introduces still require further clarification to ensure that the central contribution of this work is clearly defined. Detailed comments are provided below:
1. According to Figure R2, no pronounced dependence on doping concentration or doping time is observed. The transfer curves under different doping conditions largely overlap. While the doping effect is clearly significant compared with the pristine state, the comparison among different doping conditions does not appear to demonstrate effective carrier concentration modulation. The authors need to clarify whether this behavior arises from saturation of the doping effect under the selected conditions or from other underlying mechanisms. If saturation occurs, the doping dose should be reduced (e.g., lower concentration or shorter doping time) to explore the controllable regime. In other words, if the effective doping level cannot be precisely tuned, the limitations of this approach could become significant.
2. In Figure R4, I note that the pristine maximum current (ID,max) of the 200 nm channel-length devices increases compared with long-channel pristine devices (as shown in Fig. R2 and Fig. 1h), from approximately 10-9 A/μm to 10-7 A/μm. However, after doping, the maximum current does not improve relative to the results shown in Fig. R2 and Fig. 3a,b; instead, a slight decrease is observed for both p- and n-doped devices. This behavior may reflect scaling-induced limitations during device scaling, and the authors should clarify this point. Furthermore, scaling of channel width should also be experimentally investigated to elucidate potential limitations of the doping strategy. If pronounced scaling-related constraints are observed, they should be explicitly discussed in the manuscript.
3. The authors mention that a 25% dopant concentration leads to degraded device variation. It is strongly recommended that additional experiments be conducted to clarify the direct relationship between doping concentration and variability degradation, so that the trade-off between doping strength and device uniformity can be quantitatively understood.

Reviewer #2

(Remarks to the Author)
The authors have made considerable efforts to address the concerns raised during the first round of review, including performing additional experiments and providing additional responses. However, after a careful evaluation of the revised manuscript and the accompanying response letter, I find that several critical issues remain unresolved. Specifically, the fundamental novelty of the doping strategy remains limited, the underlying physical mechanisms are not adequately explained in the revised text, and there are significant performance limitations regarding the operating frequency that contradict the claims of scalability. Furthermore, significant discrepancies exist between the claims made in the rebuttal and the actual content of the revised manuscript. Given the lack of thorough physical analysis and these critical inconsistencies, I believe this work is not suitable for publication in Nature Communications.
The core mechanism relies on surface charge transfer doping using WO4 and N(CH3)4 functional groups. While presented as a novel breakthrough, adsorption-based doping is a conventional approach in 2D materials research. The manuscript

lacks new fundamental physics, charge transport mechanisms, mechanistic explanations for this surface chemistry application. Regarding thermal instability, the authors acknowledge a device failure at 400 C in the rebuttal and state the necessity of "further engineering." However, the revised manuscript merely reports this experimental failure without offering any meaningful discussions, physical analysis, or specific engineering strategies to overcome this limitation. Furthermore, the authors concede in the rebuttal that the limited operating frequency (100 to 500 Hz) is primarily constrained by unoptimized parasitic resistances and capacitances. Relying on long-channel devices with such critical frequency bottlenecks demonstrates that this platform lacks sufficient switching speeds and is not yet ready for realistic large-scale logic applications.

Reviewer #3

(Remarks to the Author)
The authors have addressed all my comments. I recommend acceptance.

Version 2:

Reviewer comments:

Reviewer #1

(Remarks to the Author)
I would like to thank the authors for their detailed responses and the thorough revisions made to the manuscript. The additional experimental significantly strengthen the conclusions of the paper and address my core concerns regarding the scalability and variability of the proposed process. I recommend this manuscript for acceptance.

Responses to Reviewer #1

General comment: This article demonstrates CMOS technology using WSe_2 homogeneous channels, achieving p- and n-type doping of WSe_2 through adsorption doping, and further realizing CMOS circuit modules with top-gate structures. This homogeneous technology is valuable for implementing 2D integrated circuits, as current 2D CMOS mostly uses heterogeneous channels.

General response: We gratefully acknowledge the referee for the insightful and constructive evaluation of our manuscript. We sincerely appreciate the recognition of our work on CMOS technology based on WSe_2 homogeneous channels, particularly the demonstration of both p- and n-type doping via adsorption engineering and the successful implementation of top-gated CMOS circuit modules. We agree that this homogeneous approach represents a promising pathway toward monolithic 2D integrated circuits, offering distinct advantages over prevailing heterogeneous channel configurations. In response to the referee's valuable feedback, we have carried out additional experiments, performed in-depth analyses, and refined our discussion to further strengthen the scientific rigor and clarity of the manuscript. Below, we provide a detailed, point-by-point response to each of the referee's comments, accompanied by a summary of the corresponding revisions and their locations in the manuscript.

Comment 1: The authors claim "wafer scale" or "large-scale" in the abstract and title, yet the discussion about "wafer scale" in this paper is very limited, with only Raman characterization of materials. The key aspects of this work—whether it's the doping technology or circuit units, lack analysis of wafer-level yield and variability distribution. Furthermore, I believe the current circuit unit modules cannot be called large-scale. Just as merely having device repeating unit arrays without substantial electrical interconnections cannot be called large-scale integrated circuits.

Response to Comment 1: We sincerely thank the referee for the insightful comments. We fully acknowledge the important distinction raised regarding the terminology of "wafer-scale" or "large-scale" integration. Upon careful consideration, we agree that the circuit modules demonstrated in this work—while representing a step toward monolithic CMOS integration using homogeneous WSe_2 channels—do not yet meet the rigorous standards expected of large-scale or wafer-scale integrated circuits, particularly in terms of complex electrical interconnections, functional density, and system-level integration.

The title of the paper has been revised to "**A Monolithic Integration of Two Dimensional Semiconductors for Complementary Logic Circuits**". Additionally, we have conducted additional experiments and tests, including wafer-level yield and variability analysis results in Fig. R1. The referee's comment has been instrumental in helping us refine both the claims and the presentation of our work, and we appreciate this valuable feedback.

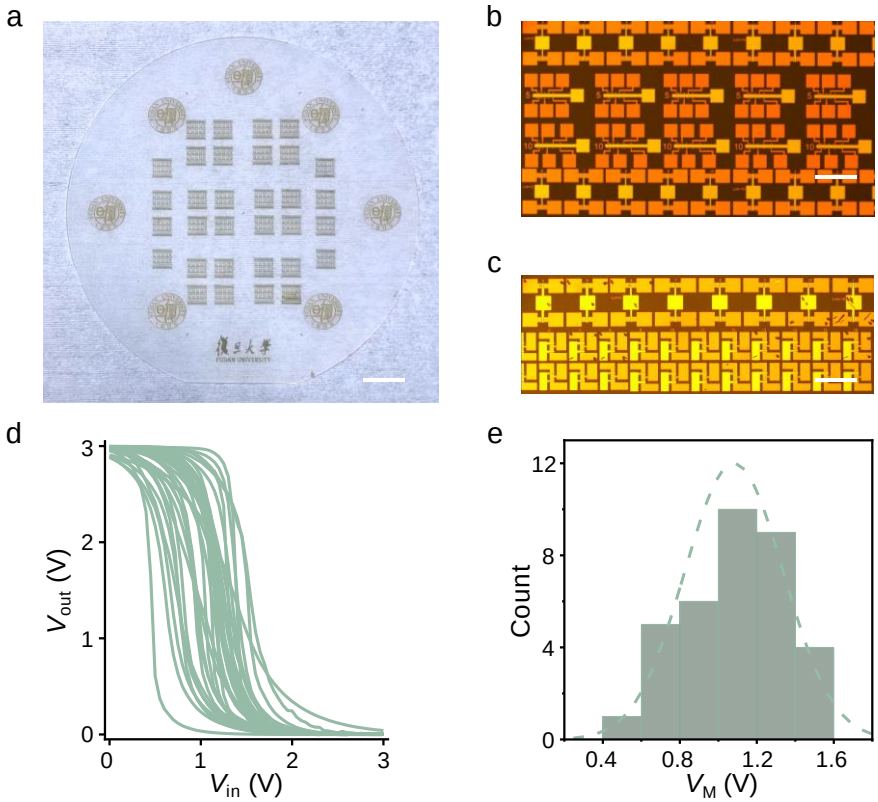

Fig. R1. a, Optical photograph of a 4-inch wafer, with a scale bar of 1 cm. b, c, Optical

microscope images of device arrays. Scale bar, 300 μm. d, Transfer characteristics curves of 35 CMOS inverters, measured under input voltages ranging from 0 to 3 V. e, Statistical distribution of threshold voltages extracted from the CMOS inverters.

Comment 2: The authors claim "novel silicon-compatible doping methods," but both "novel" and "silicon-compatible" are difficult to define. As a high-level scientific paper, such expressions should be avoided. Moreover, silicon processes typically do not use solution etching, and the dopant materials in this paper need verification. Additionally, since the circuits in this paper are fabricated on sapphire substrates, the necessity of "silicon-compatible" is unclear.

Response to Comment 2: We sincerely thank the reviewer for these thoughtful and insightful observations.

With regard to the term “novel”, we acknowledge that its use can be subjective and potentially vague in high-level scientific discourse. In our original manuscript, it was intended to highlight the distinct mechanism and procedural innovation of our adsorption-based doping strategy, which differs fundamentally from conventional substitutional doping or plasma-assisted techniques commonly used in 2D materials. While the underlying principles (e.g., charge transfer, interface engineering) are well-established in materials science, the specific implementation and integration flow we report have not been previously demonstrated for monolithic fabrication of WSe_2-based complementary logic. To maintain scientific precision, we have revised the manuscript to replace generic claims of “novel” with more concrete descriptions of the method’s distinguishing features, such as spatial uniformity, and scalable material integration.

Regarding “silicon-compatible”, we recognize that this term requires careful qualification. It was not intended to imply that every processing step directly mirrors standard Si-CMOS fabrication, nor to suggest that solution-based processing is mainstream in advanced silicon nodes. However, key aspects of our integration flow,

including photolithography, metal deposition, and dielectric integration, are designed to be compatible with back-end-of-line (BEOL) constraints. This allows us to leverage mature silicon-based CMOS technologies to accelerate the practical application of two-dimensional semiconductors. The use of wet chemical treatments (e.g., for resist development or native oxide removal) does occur in certain stages of Si manufacturing (e.g., cleaning, post-etch residue removal), and while aggressive solution etching of silicon is indeed avoided in critical steps, our process does not involve bulk etching of the semiconductor channel.

As the reviewer correctly points out, the current devices are fabricated on sapphire substrates, which are non-standard in Si-CMOS fabs. However, the core process modules—such as patterned doping, high-k metal gate stack, and metal interconnects—are designed with scalability and eventual transfer to silicon wafers in mind. We agree that a direct path to Si integration requires further validation, including demonstration on SiO_2/Si or hybrid substrates, which we identify as an important direction for future work.

In response to these concerns, we have made revisions in the manuscript to avoid overusing terms like "novel" and "silicon-compatible". The reviewer's feedback has been invaluable in helping us sharpen both the technical claims and the contextual framing of this work.

Comment 3: The authors claim to "modulate carrier polarity and concentration for WSe_2" and demonstrate polarity modulation in experiments, but there seems to be no systematic discussion about carrier concentration modulation. In the supplementary figures (S13, S14), the devices do not show significant dependence on concentration and doping time, which is likely masked by variation.

Response to Comment 3: We sincerely thank the reviewer for the insightful comment. We agree that a clear and systematic discussion of carrier concentration modulation is essential to fully support our claim of simultaneous control over both

carrier polarity and concentration in WSe_2.

In our study, n-type doping serves to modulate the carrier polarity, effectively switching the dominant charge carriers from holes to electrons. In contrast, p-type doping is employed to tune the carrier concentration, specifically, to increase the hole density, while maintaining the intrinsic p-type character of the material. This strategy enables independent control over carrier type and density, which is critical for advanced device engineering.

As the reviewer noted, the initial version of the supplementary data (Figs. S13 and S14) did not sufficiently highlight the dependence of carrier concentration on doping parameters. To address this, we have performed additional controlled experiments using a lower doping concentration (0.1%) and shorter processing time (5 s). The experiments data, presented in Fig. R2 and now included in the revised Supplementary Information (updated Figs. S13 and S14), clearly demonstrate a measurable increase in carrier concentration upon p-type doping compared to pristine devices. This trend is consistent across multiple samples and supports our assertion that p-type doping effectively modulates carrier density.

We have also strengthened the relevant discussion in the manuscript to better clarify the distinct roles of n-type and p-type doping in regulating carrier polarity and concentration, respectively. We are grateful for the valuable feedback, which has helped us enhance the quality and impact of the manuscript.

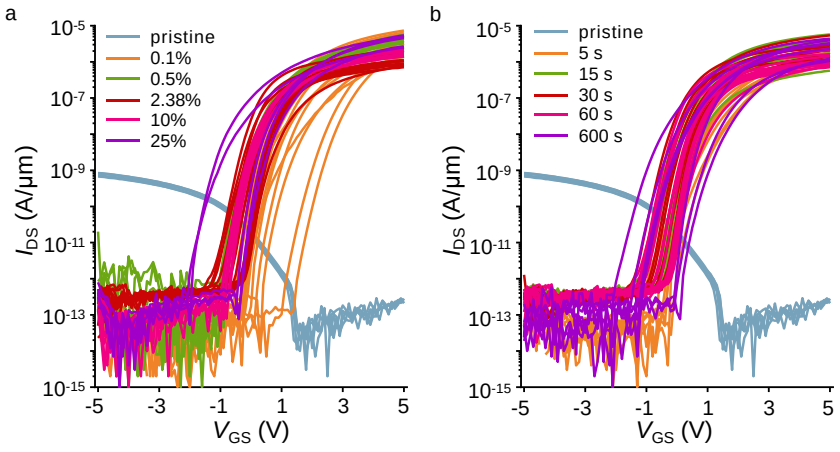

Fig. R2. a, Transfer characteristics of WSe_2 transistors treated with 0.1-25 wt% TMAH solution. b,

Transfer characteristics of WSe_2 FETs with treatment time (5–600 s).

Comment 4: The high gain and low power consumption in the abstract are taken from different supply voltages. However, whether it's high gain at 5 V or "low power consumption" at 2 V, the key issue is that the operating voltage is too high, which does not match "next-generation" electronic devices and "low-power applications." The authors should demonstrate high performance of devices and circuits at voltages below 1 V, including gain, power consumption, noise margin, etc. Performance at voltages as high as 5 V has no practical value (Fig. 3c-d).

Response to Comment 4: We sincerely appreciate the reviewer's valuable comment regarding the operating voltage and its implications for low-power, next-generation electronics. We fully acknowledge that ultra-low-voltage operation is a critical requirement for future low-power applications, and we thank the reviewer for prompting us to further clarify and extend our analysis in this direction. The measurements presented in the original manuscript, high gain at 5 V and low power consumption at 2 V, were intended to demonstrate the functional versatility of our doping strategy across different bias conditions, rather than to claim optimal performance for ultra-low-power scenarios. As correctly pointed out by the reviewer, the device architecture in this study is based on long-channel transistors (channel length: 10 μm), with relatively thick gate oxides (16 nm for NMOS and 25 nm for PMOS). Such dimensions are not optimized for sub-1 V operation, which explains the reduced drive current and non-saturation behavior at lower supply voltages (e.g., 1 V). Consequently, while operation at 5 V enables clear demonstration of high gain and circuit functionality, it is indeed less relevant for ultra-low-voltage applications.To directly address the reviewer's concern, we have conducted additional experiments to evaluate device and circuit performance at V_{DD} = 1 V. The results, now included as Fig. R3 in the revised manuscript, show that the doped WSe_2 transistors remain functional at this low supply voltage, with measurable gain and significantly reduced

power consumption. While the current drive is naturally lower due to the long-channel design, the devices maintain clear switching behavior and acceptable noise margins, demonstrating the potential of our doping approach even in low-voltage regimes.We also emphasize that the contribution of this work lies in establishing a robust doping methodology for 2D semiconductors, which can be readily applied to scaled device geometries. Future optimization of channel length and gate dielectric thickness will enable efficient sub-1 V operation without compromising performance. We thank the reviewer again for this constructive suggestion, which has enabled us to provide a more comprehensive evaluation of our devices across a broader range of operating conditions.

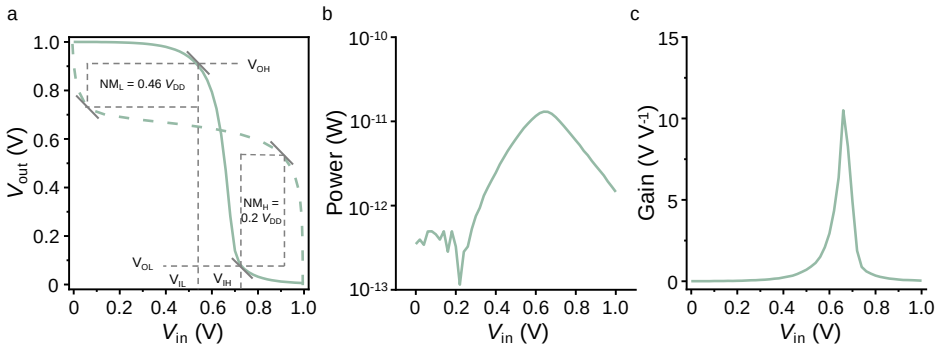

Fig. R3. a, Voltage transfer characteristics of homogeneous WSe_2 CMOS inverter showing rail-to-rail output swing at V_{DD} = 1 V, with noise margin exceeding 65% V_{DD}. b, Power consumption profiling demonstrating ultralow static power of several pW at V_{DD} = 1 V. c, Voltage gain analysis revealing maximum gain of ~ 12 V/V at V_{DD} = 1 V.

Comment 5: Regarding device size scalability: First, the channel length and width of devices throughout the paper are missing. Second, based on the scale bar in Fig. 1g, the channel length and width are on the order of several micrometers. Since the conclusions of this paper are based on long-channel devices, my key concern is whether effective doping can be achieved in short channels (sub-100 nm or even smaller dimensions). This part should be demonstrated to support the scalability benchmark in Fig. 3f.

Response to Comment 5: We sincerely apologize for the omission of key device dimensions in the original submission. As requested, the channel length and width have now been explicitly stated in the experimental section: the devices used in this study have a channel length of 10 μm and a channel width of 30 μm. We also thank the reviewer for noting the feature sizes from Fig. 1g—our fabrication process indeed initially targeted micrometer-scale devices to establish the proof-of-concept for our doping strategy in a controlled, reproducible manner.

The reviewer raises a crucial point concerning the scalability of effective doping into the short-channel regime, particularly below 100 nm, which is highly relevant for advanced technology nodes. While the current study focuses on long-channel devices to isolate and evaluate the fundamental doping mechanism, we fully agree that demonstrating scalability to smaller dimensions is essential for assessing the technology's potential. Due to current limitations in our lithography capabilities, we were unable to fabricate devices with channel lengths below ~200 nm. However, to address the reviewer's concern, we have conducted additional experiments on devices with 200 nm channel length, which represent the smallest scalable dimension achievable in our current process flow. The electrical characteristics and doping efficiency in these scaled devices are now presented in Fig. R4, showing that our doping approach remains effective even at this sub-micron scale, with well-defined threshold voltage control and on/off ratio.

Regarding the scalability benchmark in Fig. 3f, we acknowledge that the term may have been ambiguous in the original version. This figure illustrates the large-area scalability and uniformity of our doping and fabrication process across a 4-inch wafer, emphasizing the compatibility with industrial-scale manufacturing, as opposed to small-scale, transfer-based methods commonly used in 2D material devices. We agree that further scaling down the channel length is an important next step, to explore sub-100 nm devices in future work.

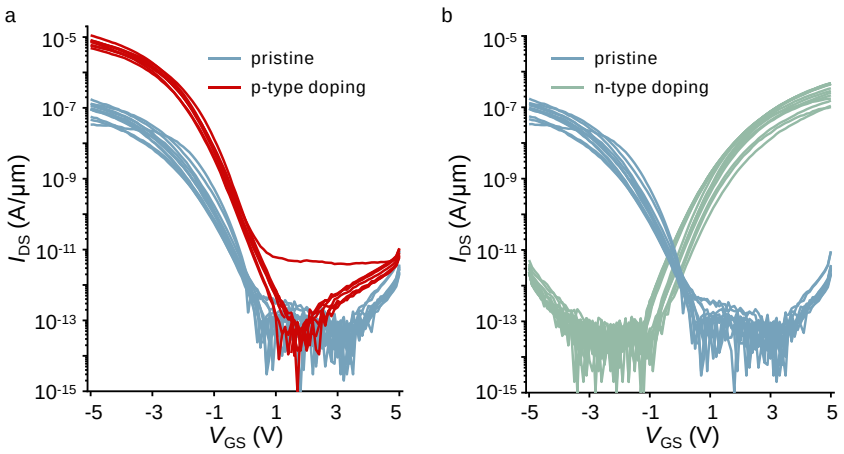

Fig. R4. a, Transfer characteristic curves of p-type doped devices and pristine devices with a channel length of 200 nm. b, Comparison of transfer characteristic curves of n-type doped devices and pristine devices with a channel length of 200 nm.

Comment 6: Similarly, since the doping technology in this paper is still based on adsorption, I suspect that the performance variation of this technology in short channels and narrow channels is also a non-negligible challenge. Therefore, I recommend adding experiments in this part to clarify this issue.

Response to Comment 6: We sincerely thank the reviewer for this insightful and constructive comment. We fully agree that the performance stability of adsorption-based doping in short-channel and narrow-width devices is a critical consideration, particularly as device scaling intensifies challenges related to dopant uniformity and short-channel behavior.

In response to this important concern, we have conducted additional experiments to evaluate the effectiveness and uniformity of our doping strategy at scaled dimensions. While the current lithography process limits the minimum achievable channel length and width to 200 nm—preventing direct exploration of the sub-100 nm regime—we emphasize that this dimension still serves as a meaningful benchmark for assessing scalability.

As shown in Fig. R4, the experimental results demonstrate clear and reproducible modulation of device characteristics (e.g., threshold voltage shift and on-current) in 200 nm devices, confirming that the adsorption-based doping remains effective even under scaled conditions. Furthermore, the low device-to-device variability observed across multiple samples indicates good uniformity and process reliability, suggesting that the adsorption process is sufficiently conformal and stable at these dimensions.

These findings support the scalability of our approach within the experimentally accessible range. While further studies at smaller scales will require advanced techniques, the current results provide a solid experimental foundation for understanding the behavior of adsorption-based doping in scaled device geometries. We believe the experimental results strengthens the manuscript, and we are grateful to the reviewer for this valuable suggestion.

Comment 7: Furthermore, since this is adsorption-based doping, will this method affect the electrical reliability of devices, such as PBTI/NBTI? The authors should supplement relevant experimental data.

Response to Comment 7: We sincerely appreciate the reviewer's insightful and professional comments. We fully acknowledge that, for adsorption-based doping, potential impacts on electrical reliability, particularly under bias temperature stress conditions such as PBTI and NBTI, are critical concerns that must be rigorously evaluated.

We have conducted comprehensive reliability assessments on both NMOS and PMOS devices. Specifically, PBTI measurements were performed on NMOS transistors under elevated gate bias (3 V) and temperature stress (90 ℃), while NBTI tests were carried out on PMOS devices under gate bias (- 3 V) and temperature stress (90 ℃). As shown in Fig. R5, the threshold voltage shift (ΔV_{th}) over stress time remains minimal for both device types, with no significant degradation The small ΔV_{th} and stable subthreshold swing indicate excellent interface quality and minimal trap

generation, demonstrating that the adsorption process does not introduce detrimental defects that compromise long-term reliability.

We believe these additional experimental results significantly strengthen the technical rigor and practical relevance of our work. The reviewer's suggestion has been invaluable in deepening the reliability analysis of our approach, and we are grateful for this constructive feedback.

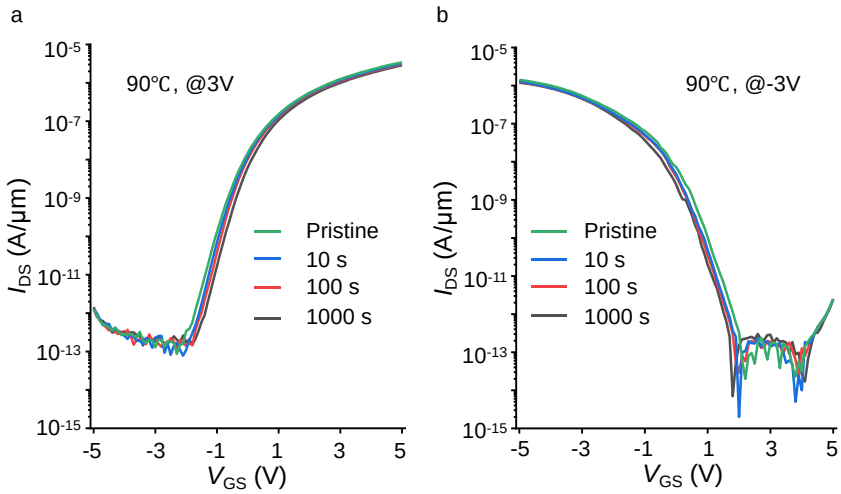

Fig. R5. a, PBTI characteristics for NMOS device under a positive stress voltage of 3 V at an elevated temperature of 90℃. b, NBTI characteristics for PMOS device under a negative stress voltage of -3 V at an elevated temperature of 90℃.

Comment 8: The quality of Supplementary Fig. 3 is poor, affecting readability. Additionally, according to this process, are the dielectric thicknesses of PMOS and NMOS different? What is the actual gate dielectric of PMOS?

Response to Comment 8: We appreciate the reviewer's constructive comments. We have carefully revised Supplementary Fig. 3 to significantly improve its resolution, clarity, and overall readability. The reviewer's observation regarding the difference in gate dielectric thicknesses between PMOS and NMOS is correct and well taken. In

our fabrication process, the PMOS and NMOS devices employ distinct dielectric stack architectures to accommodate their respective process requirements and doping strategies. Specifically, the PMOS gate dielectric consists of a bilayer hard mask composed of Al_2O_3 and HfO_2, followed by an additional 16 nm-thick HfO_2 layer deposited via atomic layer deposition (ALD), resulting in a relatively thicker overall dielectric stack. In contrast, the NMOS device utilizes a simpler and thinner gate dielectric structure, comprising only the 16 nm HfO_2 layer grown by ALD. This deliberate design choice arises from process integration considerations, particularly the need for selective doping and etch resistance in the PMOS region, where the additional hard mask layers serve both as a doping barrier and a gate dielectric component. Thank you again for this insightful comment.

Comment 9: The electrical properties in Fig. 1h and Fig. 3 seem inconsistent. Fig. 1h clearly shows different threshold voltages. This may still be due to excessive variation.

Response to Comment 9: We sincerely thank the reviewer for this perceptive and insightful observation. We acknowledge the apparent discrepancy in V_{th} between Fig. 1h and Fig. 3.

The differences in V_{th} values arise from the intentional selection of devices with distinct electrical characteristics to highlight different aspects of our adsorption-based doping approach. Specifically, Fig. 1h presents a representative comparison of transistors with higher on-currents, primarily to emphasize the core demonstration of effective p-type and n-type doping, our primary focus in the initial figure. These devices were selected to clearly illustrate the successful realization of complementary conductivity types and the modulation of carrier polarity.

In contrast, Fig. 3 focuses on devices for low-power CMOS applications, where subthreshold swing, V_{th} control, and switching performance are prioritized. The threshold voltages in this figure reflect devices fabricated under refined process

conditions that minimize variability and enhance uniformity—thus better representing the potential for practical low-power integration.

That said, we recognize that residual device-to-device variations—attributable to subtle fluctuations in the adsorbed dopant profile, interfacial trap density, or thin-film morphology—can contribute to V_{th} shifts across different samples. While the overall doping trend is consistent and reproducible, we agree with the reviewer that further reduction of variation is important for large-scale deployment. As part of our ongoing process optimization, we are actively investigating strategies such as improved adsorption control, interface passivation, and process uniformity enhancement to minimize such fluctuations.

We are grateful to the reviewer for highlighting this important aspect, which has helped us strengthen the presentation and interpretation of our data.

Comment 10: Regarding image readability, the insets in Fig. 3a-c are too small.

Response to Comment 10: We sincerely thank the reviewer for the valuable feedback regarding image readability. We fully agree with the concern that the original insets in Figures 3a–c were too small to be clearly read. To address this, we have carefully revised the presentation of these insets to improve clarity and accessibility.

Specifically, the insets originally shown in Fig. 3a have been expanded and relocated to Supplementary Fig. 10, where they are now displayed at higher resolution with enhanced labeling and improved contrast for better visualization. Additionally, we have redesigned the insets in Figs. 3b and 3c by increasing their size, optimizing font clarity, and adjusting the layout within the main figure to ensure legibility without compromising the overall composition.

These updates are included in the revised manuscript and supplementary file. We believe these improvements significantly enhance the clarity and impact of the data presentation. We greatly appreciate the reviewer's attention to detail, which has

helped us strengthen the graphical communication of our results.

Comment 11: Supplement Figure 1. Please double-check. The horizontal position of the edge of WSe_2 corresponds to approximately 0.8 microns. I doubt the authenticity of the test data.

Response to Comment 11: We are deeply grateful to the reviewer for the meticulous scrutiny and constructive feedback regarding Supplementary Fig. 1. We have rechecked our test data and revised Supplementary Fig. 1 accordingly.

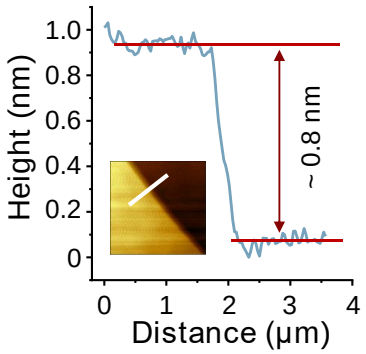

Fig. R6. AFM Characterization of Monolayer WSe_2 Film with measured thickness of ~ 0.8 nm.

Comment 12: Supplementary Fig. 5a: There seems to be an air gap (about 30-50 nm) between the SD edge and the top gate dielectric? This could be a major challenge for device scaling.

Response to Comment 12: We sincerely thank the reviewer for this highly insightful and technically profound observation. The reviewer is correct in identifying the presence of an apparent air gap, estimated to be approximately 30–50 nm, between the source/drain (S/D) electrodes and the edge of the top-gate dielectric in Supplementary Fig. 5a. We fully acknowledge that such a gap can indeed undermine gate electrostatic control over the channel region, potentially leading to degraded

device performance, including increased short-channel effects and reduced switching efficiency. This is particularly critical as the field moves toward scaled, high-performance 2D electronic devices. This gap primarily arises from the sequential fabrication process employed in our current top-gate device architecture, where the deposition of the gate dielectric (e.g., Al_2O_3 or HfO_2) via atomic layer deposition (ALD) or physical vapor deposition (PVD) does not perfectly conform to the patterned S/D electrodes due to limitations in edge coverage and interfacial adhesion. As a result, a small but non-negligible misalignment or poor conformity persists, leading to the observed discontinuity. We agree with the reviewer that this issue represents a significant materials and processing challenge in the realization of scaled top-gate 2D transistors. It not only limits the minimum achievable effective channel length but also constrains efforts to reduce gate dielectric thickness for enhanced gate capacitance and lower operating voltage. We will work on advanced device architectures to overcome this limitation, and we believe that highlighting this challenge in our manuscript will serve as a valuable reference for the community.

Comment 13: Supplementary Figs. 10-11: How is the enhancement of carrier concentration calculated? The threshold voltage does not seem to change significantly.

Response to Comment 13: We appreciate the reviewer's comments, which has provided a valuable opportunity to clarify our methodology and strengthen the presentation of our results. The formula we used to calculate the carrier concentration is as follows. The V_{th} has shown significant changes, which can be observed by comparing transfer characteristics curves of pristine and doped devices.

$$\mu = \frac{L}{C_{ox} * W * V_{DS}} * \frac{dI_{DS}}{dV_{GS}}$$

$$n = \frac{L * I_{DS}}{q * W * V_{DS} * \mu}$$

Comment 14: Supplementary Figs. 13-18: Information about the number of devices is missing. Supplementary Figs. 13-14: The variation seems to increase after doping.

Response to Comment 14: We appreciate the reviewer's comments. We have added device number information to the supplementary materials, making the manuscript more comprehensive. Regarding the observed increase in variation after doping, as highlighted in Supplementary Figs. 13–14, we appreciate the reviewer's keen observation. Indeed, under a doping concentration of 25% and a treatment duration of 10 minutes, we do observe an increased variability in device characteristics, compared to the pristine samples. We attribute this enhanced variability primarily to two interrelated factors: (i) localized surface degradation of the two-dimensional WSe_2 lattice induced by prolonged exposure to the doping agent, and (ii) non-uniform dopant adsorption or diffusion at the atomic-layer interface, which becomes more pronounced under aggressive doping conditions. We thank the reviewer for highlighting this important aspect, which not only strengthens our data presentation but also provides meaningful insight into the practical limitations and scalability of the doping strategy for 2D semiconductor devices.

Comment 15: Supplementary Fig. 19: The description of yield with 20 devices is insufficient. Additionally, this figure does not demonstrate "rail-to-rail." Rail-to-rail refers to the input and output ranges being consistent.

Response to Comment 15: We sincerely thank the reviewer for the insightful observations, which have enabled us to significantly improve the rigor and clarity of our experimental presentation.

With regard to the first point, we acknowledge that the initial description of device yield based on 20 devices was limited in statistical scope. In response, we have

substantially expanded our data by including additional fabrication and characterization results. This expanded data is now fully presented in the updated Supplementary Fig. 19, which includes a comprehensive yield analysis with detailed categorization of device performance.

Concerning the second point about the "rail-to-rail" operation, we appreciate the reviewer’s precise technical clarification. Upon careful evaluation, we agree that the original version of Supplementary Fig. 19 did not adequately demonstrate true rail-to-rail behavior, which, as correctly noted, requires both input and output signal ranges to extend fully from the lower to upper supply voltage rails. To address this, we have revised the measurement protocol and device biasing conditions to ensure full-swing operation. Specifically, we have adjusted the input signal range to span the entire supply voltage window and confirmed that the output faithfully follows across all tested devices. The updated Supplementary Fig. 19 now includes transfer characteristics and dynamic response traces that clearly illustrate both input and output signals achieving rail-to-rail swing under operational conditions. We are grateful to the reviewer for prompting these clarifications, which have led to a more thorough and precise representation of our results.

Responses to Reviewer #2

General comment: This manuscript presents a wafer-scale integration of homogeneous complementary metal-oxide-semiconductor (CMOS) circuits based on monolayer WSe_2, utilizing a bilayer hard mask process and charge transfer doping methods. By employing ammonium tungstate for p-type and TMAH for n-type doping, the authors demonstrate a practical approach to overcome the challenges of heterogeneous integration, realizing functional inverters with high voltage gain (396 V/V) and complex logic gates such as XOR and MUX. The demonstration of ultra-low static power consumption and the successful fabrication of logic arrays highlight the potential of this technology for next-generation low-power electronics. However, serious concerns remain regarding the fundamental stability of the doping mechanism and the integrity of the channel interface along with deep academic insights required for publication. These issues must be addressed to enhance the scientific reliability and practical scalability of the proposed technology.

General response: We sincerely appreciate the recognition of our advances in wafer-scale monolayer WSe_2 CMOS integration, including the demonstration of high-performance inverters, complex logic functionality, and ultra-low power operation. We also fully acknowledge the reviewer's valid and scientifically rigorous concerns regarding the stability of the doping strategy and the interfacial quality of the channel. These points are indeed critical for assessing the robustness and scalability of any emerging semiconductor technology. In response, we have conducted a series of additional experiments, performed in-depth analyses, and incorporated enhanced discussions into the manuscript to directly address each concern. Below, we provide a detailed, point-by-point response to all comments, outlining the experimental and theoretical efforts undertaken to strengthen the scientific foundation and technical clarity of our work.

Comment 1: The proposed doping mechanism relies on the surface adsorption of functional groups (WO_4 and $N(CH_3)_4$), which induce charge transfer to the WSe_2 channel. Since surface-adsorbed molecules are inherently susceptible to thermal desorption or migration, the provided stability data at 200 °C is insufficient to define the operational limits. The authors should identify the actual thermal failure point where the doping effect begins to degrade. By providing electrical data up to 400 °C, the authors should clearly define the thermal budget of their devices up to BEOL compatibility of the devices.

Response to Comment 1: We gratefully acknowledge the reviewer's critical insight regarding the thermal stability of our surface-mediated doping approach—an essential consideration for integration with back-end-of-line (BEOL) processes. In response, we have carried out systematic thermal stability tests by annealing both p-type and n-type doped WSe_2 transistors at elevated temperatures (250 °C and 400 °C) under an Ar atmosphere for 1 hour, followed by comprehensive electrical characterization. The results are now presented in Fig. R7. Our findings reveal that at 250 °C, both n-type and p-type devices retain their doping characteristics with only minor degradation in performance, indicating good thermal resilience at this temperature. However, at 400 °C, a significant deterioration is observed: the p-type doping effect is substantially weakened, and n-type doping fails completely, as evidenced by the loss of clear electron conduction. These results establish a clear thermal budget for device processing and operation, confirming compatibility with certain low-temperature BEOL steps while highlighting the need for further engineering to achieve high-temperature stability. We have added this analysis to the manuscript.

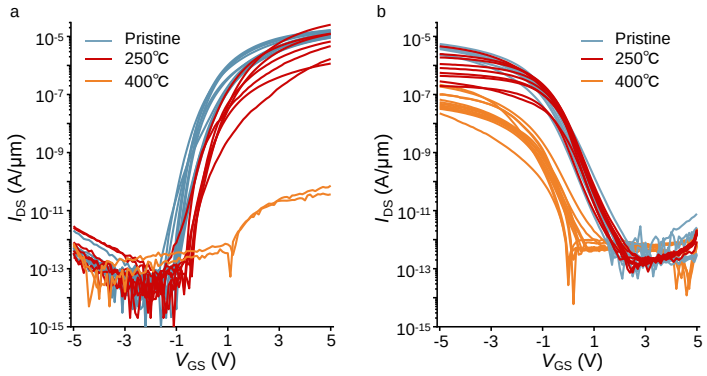

Fig. R7. Thermal stability of the doping methods. a, The transfer characteristics of n-type doped WSe_2 transistors which were annealed in a tube furnace under Ar atmosphere at 250°C and 400°C for 1 hour. b. The transfer characteristics of p-type doped WSe_2 transistors which were annealed under Ar atmosphere at 250°C and 400°C.

Comment 2: In Supplementary Fig. 14, hysteresis is observed when the TMAH concentration reaches 25%. This suggests that aggressive chemical treatment might induce interface traps or surface defects. Although the authors optimized the concentration to window, the physical origin of this hysteresis is not thoroughly discussed. The authors are encouraged to compare the interface trap density (Dit) of pristine and processed devices to quantitatively verify the surface integrity. A detailed discussion on the trade-off between doping efficiency and interface quality would provide valuable insights to the readers rather than just presenting the final optimized result.

Response to Comment 2: We sincerely thank the reviewer for this perceptive observation. Upon re-evaluation, we identified an error in the original version of the figure, which contributed to the misinterpretation of hysteresis at 25 wt% TMAH concentration. We have now corrected and redrawn the relevant data. Fig. R8a presents the transfer characteristics of both pristine and p-type doped WSe_2 transistors treated with 25 wt% TMAH, showing no significant hysteresis compared to the

control devices. To further investigate interface quality, we performed capacitance-voltage (C–V) measurements on both pristine and doped devices. As shown in Figs. R8b and R8c, the doped devices exhibit lower frequency dispersion and sharper C–V curves, indicating a reduction in interface trap density (D_{it}) after doping. This suggests that, under optimized conditions, the TMAH treatment may actually passivates certain native defects rather than introduce new traps. Nonetheless, we acknowledge that at high doping concentrations (e.g., 25 wt%), increased device-to-device variability is observed, likely due to non-uniform adsorption or local surface perturbations.

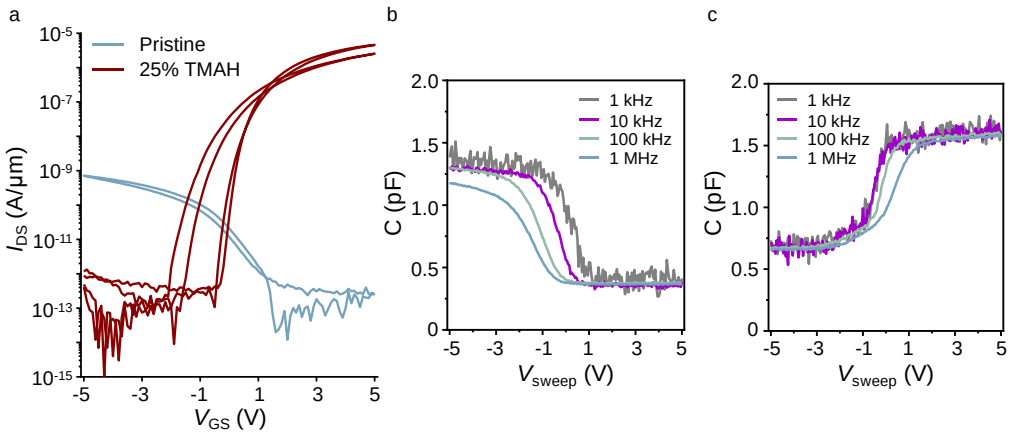

Fig. R8. a, Transfer characteristics of pristine WSe_2 and p-type doped WSe_2 transistors treated by 25 wt% TMAH solution. b, CV curves of pristine p-type device. c, CV curves of n-type doped device.

Comment 3: The mechanism of n-type doping through TMAH treatment requires further clarification regarding its effect on the pre-existing p-doping. Since the entire WSe_2 channel is initially p-doped, the n-type regions must undergo a significant polarity inversion. While the DFT calculations in Supplementary Fig. 7 provide insights into the electronic states of $N(CH_3)_4$ groups, the manuscript does not explicitly discuss whether the TMAH treatment physically removes the p-type dopants or if the electron-donating effect of the $N(CH_3)_4$ groups simply overwhelm

the previous carrier concentration. A clearer experimental or theoretical explanation of this mechanism would add significant depth to the discussion of the homogeneous integration process.

Response to Comment 3: We appreciate the reviewer's insightful comments, which are a valuable scientific question. To clarify the polarity inversion process, we have performed additional density functional theory (DFT) calculations to model the coexistence of p-type and n-type dopants on monolayer WSe_2. The results, presented in Fig. R9, show that the $N(CH_3)_4$ group exhibits a strong electron-donating character, introducing donor states near the conduction band minimum. Even in the presence of pre-existing p-type dopants, the charge transfer from $N(CH_3)_4$ is sufficient to compensate and ultimately invert the dominant carrier type, leading to effective n-type conduction. The differential charge density plots (Fig. R9a) and density of states (DOS) analysis (Fig. R9b) confirm that the $N(CH_3)_4$-induced states dominate the near-Fermi-level electronic structure, enabling robust electron accumulation. This mechanism enables spatially selective doping without requiring physical removal of prior dopants, which is key to our mask-based patterning approach.

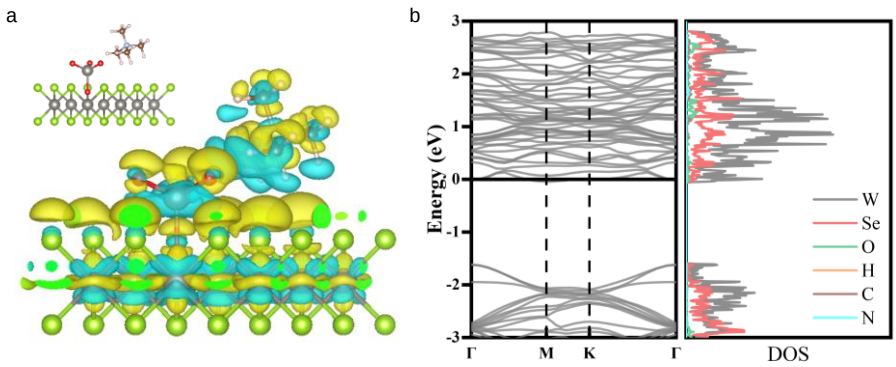

Fig. R9. DFT calculations. a, Differential charge density distributions of WSe_2 with $N(CH_3)_4$ and WO_4 group. b. DOS profile of WO_4 group adsorbed WSe_2 at Se vacancy site and $N(CH_3)_4$ group adsorbed on WSe_2. Inset presents the atomic structure of monolayer WSe_2, WO_4 group and $N(CH_3)_4$ group.

Comment 4: Figure 3f serves as a benchmark figure but lacks legibility and a transparent representation of critical performance metrics. Specifically, while the authors claim to establish new performance standards, the benchmark plot omits operation frequency or switching speed, which are fundamental to logic circuit performance. Furthermore, the current visualization in Fig. 3f makes it difficult to quantitatively assess how the reported WSe_2 CMOS compares to recent state-of-the-art literature. The authors are encouraged to improve the clarity of Figure 3f and provide a detailed comparison table in the main text, including specific values for mobility, delay, and gain at comparable supply voltages to ensure an objective evaluation of the work. Typographical errors in the figure should be revised as well.

Response to Comment 4: We appreciate the reviewer's detailed comments. We agree that a clear and quantitative benchmarking is essential for contextualizing our results within the broader field. In response, we have completely revised Fig. 3f to improve clarity, readability, and data transparency. The updated version uses a cleaner layout, consistent scaling, and corrected typographical errors, with clearly labeled data points and improved legends. Additionally, we have added a comprehensive performance comparison table (Supplementary Table 1) . While our current devices demonstrate excellent voltage gain (396 V/V) and ultra-low static power, we acknowledge that the switching speed and operating frequency are limited by relatively large parasitic resistance and capacitance, particularly associated with the long-channel design and interconnects. As such, the current work primarily validates the feasibility and uniformity of wafer-scale homogeneous integration rather than maximizing high-speed performance. We have added a candid discussion of these limitations and outlined our future directions, including contact engineering and device scaling, to reduce parasitic resistance and capacitance and enhance switching speed. This context is now clearly presented in the revised manuscript.

Comment 5: The authors utilized Au electrodes for both PMOS and NMOS devices.

Could the authors clarify the reason behind using a single metal (Au) for both cases? It would be informative to know if other contact metals have been evaluated to improve the contact resistance for the n-type region. Additionally, there is a difference in the top-gate dielectric thickness between the p-type (~30 nm) and n-type (~20 nm) regions due to the bilayer hard mask process. The manuscript would benefit from including a discussion on how this structural asymmetry was considered in the device design and threshold voltage optimization.

Response to Comment 5: We appreciate the reviewer's detailed technical inquiry. Regarding contact metal selection, we systematically evaluated alternative low-work-function metals such as In (indium) for the NMOS contacts to improve electron injection. As shown in Fig. R10, while In does yield higher on-currents due to better band alignment, it results in an excessively negative threshold voltage (V_{th}), which compromises noise margin and power efficiency in CMOS operation. In contrast, Au, despite its higher work function, provides a more balanced V_{th} for both NMOS and PMOS devices, enabling symmetric switching behavior and low-power logic operation. Moreover, using a single metal (Au) for both device types simplifies the fabrication process and reduces process complexity.

With respect to the dielectric thickness asymmetry (~30 nm for PMOS vs. ~20 nm for NMOS), this arises from the bilayer hard mask process used for selective doping. Although the thicknesses differ, we carefully engineered the doping concentrations and gate stack configurations to compensate for the resulting capacitance mismatch. As a result, both device types achieve well-matched threshold voltages and balanced current drive, which is essential for robust CMOS operation.

We again thank the reviewer for the rigorous and insightful feedback, which has greatly strengthened the scientific depth, clarity, and technical rigor of our manuscript.

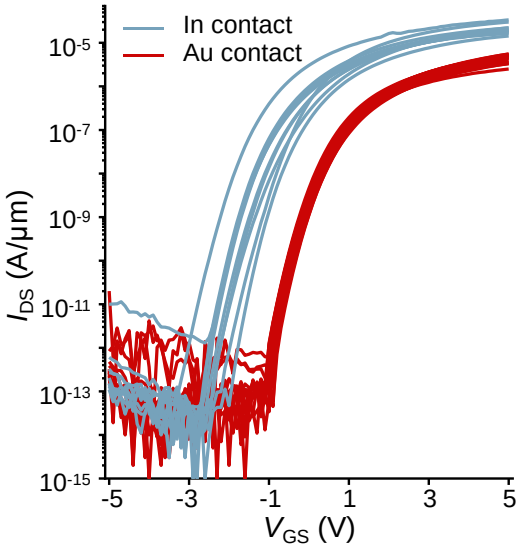

Fig. R10. Transfer characteristic curves of FETs using In and Au contacts.

Responses to Reviewer #3

General comment: This study addresses the critical bottleneck issues in the field of two-dimensional (2D) semiconductors and proposes a novel CMOS-compatible p/n-type doping strategy. It has successfully realized a wafer-scale uniform array of WSe_2 top-gate CMOS circuits. The research demonstrates prominent innovation, a clear technical route, and comprehensive experimental data. The fabricated WSe_2 CMOS inverters exhibit outstanding metrics, which rank among the leading levels in the current 2D CMOS technology. Thereby providing a crucial solution for advancing the practical application of 2D semiconductors in low-power large-scale integrated circuits. It holds significant academic value and application potential.

General response: We thank the referee for the positive evaluation and constructive comments, which have significantly enhanced the quality of our manuscript. In response to the referee's comment, we have conducted additional tests to address the raised concerns. Below, we provide detailed, point-by-point responses to each of the referee's comments, along with a summary of the changes made to the manuscript.

Comment 1: The inverter exhibits optimal performance (e.g., highest gain) at a supply voltage of 5 V and minimal power consumption at 2 V; however, the logic gates operate at a supply voltage of 3 V. The authors should clarify the rationale behind this voltage selection.

Response to Comment 1: We thank the reviewer for this thoughtful question. In this work, we focus on demonstrating the applicability of our doping strategy to long-channel devices and basic CMOS circuits, with a channel length of 10 μm, an NMOS gate dielectric thickness of 16 nm, and a PMOS dielectric thickness of 25 nm. At 5 V supply voltage, the inverter achieves maximum DC gain due to sufficient overdrive voltage. Conversely, at 2 V supply voltage, the static power consumption is

significantly reduced, enabling ultra-low-power operation. However, to balance performance, reliability, particularly to avoid potential dielectric breakdown while ensuring stable circuit operation, we selected 3 V as the operating voltage for the logic gates. This choice also accounts for non-optimized parasitic resistance and capacitance in the current device architecture.

Comment 2: The maximum operating frequency of the CMOS circuits reported in this work is 100 Hz. Can this frequency be further increased? The authors are suggested to discuss the factors that limit the switching frequency of the AND and OR gates in their revision.

Response to Comment 2: We appreciate the reviewer's insightful observation. We have conducted additional dynamic measurements to evaluate the high-frequency performance of the CMOS inverters. As shown in Fig. R11, the inverters remain functional at frequencies up to 500 Hz, demonstrating that the operational frequency can indeed be increased beyond 100 Hz. However, the current frequency limit is primarily constrained by parasitic resistance and capacitance in both the device and interconnect architecture. These parasitic resistance and capacitance arise from the non-ideal gate stack, contact resistance, and interconnect layout, which were not optimized in this proof-of-concept study. As a result, signal distortion becomes pronounced at higher frequencies, limiting the maximum switching speed.

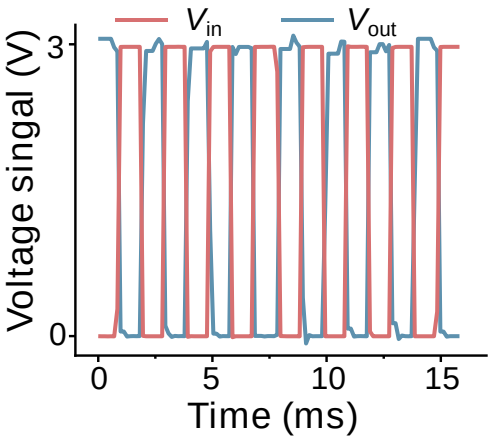

Fig. R11. Dynamic output characteristics of CMOS inverters at frequencies of 500 Hz.

Comment 3: In the device fabrication section, the function of the 2 nm SiO_2 seeding layer should be clearly explained.

Response to Comment 3: We thank the reviewer for highlighting this important point. Due to the absence of dangling bonds on the surface of two-dimensional semiconductors, conventional atomic layer deposition (ALD) techniques struggle to nucleate dielectric films directly on two-dimensional film. To overcome this challenge, we introduced a 2 nm SiO_2 seeding layer, which serves critical function: it provides nucleation sites for subsequent ALD growth of high-quality gate dielectrics. This enables reliable dielectric integration in CMOS fabrication.

Comment 4: Given the excellent transistor and logic-gate performance and yield, the absence of larger-scale circuit demonstrations requires clarification. The authors should discuss the main challenges currently hindering the realization of large-scale integrated circuits based on this platform.

Response to Comment 4: We appreciate the reviewer's insightful comments. While our current work demonstrates fundamental logic circuit units, such as inverters,

NAND, and NOR gates, we acknowledge that more complex, large-scale integrated circuits have not yet been implemented. The primary challenge lies in the lack of process-compatible circuit design and layout tools tailored for 2D material-based fabrication. Additionally, scaling up requires precise control over interconnect parasitic, device matching, and yield across thousands of transistors—challenges that are currently being addressed in our follow-up research. We are actively developing design automation frameworks and process integration schemes to enable large-scale 2D ICs.

Comment 5: The thickness of the monolayer WSe_2 should be indicated in Supplementary Figure 1 for clarity.

Response to Comment 5: We thank the reviewer for this valuable suggestion. To improve clarity, we have updated Supplementary Fig. 1 to include atomic force microscopy (AFM) data clearly showing the thickness of the monolayer WSe_2 flake. As shown in Fig. R12, the measured step height is approximately 0.8 nm, consistent with the expected thickness of a single WSe_2 layer. This information has been added to the figure caption and main text to enhance data transparency. We have modified Supplementary Fig. 1 to make the characterization results clearer.

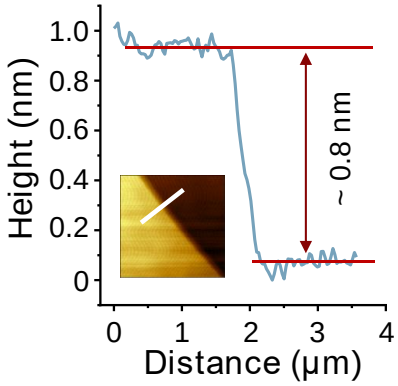

Fig. R12. AFM test result of monolayer WSe_2 film with measured thickness of ~ 0.8 nm.

Comment 6: The notation "WO_4" is potentially misleading. Since tungsten has a valence state of +6, it would be more accurate to use "$(WO_4)^{2-}$" to avoid misunderstanding.

Response to Comment 6: We appreciate the reviewer's detailed observations, which have significantly enhanced the quality of our manuscript. Since the WO_4 moiety can exist in either charged or neutral states, to prevent any confusion regarding its charge state, we have referred to WO_4 as a 'group' throughout the text.

Comment 7: Several minor grammatical and typographical issues should be corrected. For example, in line 32, "IC" should be revised to "ICs," and in line 75, "a positive" should be capitalized to "A positive" at the beginning of the sentence.

Response to Comment 7: We are grateful to the reviewer for carefully proofreading our manuscript. We have thoroughly reviewed the entire text to correct all grammatical, typographical, and formatting errors. Specifically, "IC" has been updated to "ICs" (line 32) to reflect plural usage, and "a positive" has been capitalized to "A positive" at the beginning of the sentence (line 75).

Responses to Reviewer #1

General comment: The authors' responses and the revised manuscript have been carefully evaluated. Although efforts have been made to provide additional data, clarify statements, and address part of the concerns raised, leading to an overall improvement in manuscript quality, the scalability of the doping strategy and the variability it introduces still require further clarification to ensure that the central contribution of this work is clearly defined.

General response: We sincerely appreciate the recognition of our advances in wafer-scale monolayer WSe_2 CMOS integration, including the demonstration of high-performance inverters, complex logic functionality, and ultra-low power operation.

Comment 1: According to Figure R2, no pronounced dependence on doping concentration or doping time is observed. The transfer curves under different doping conditions largely overlap. While the doping effect is clearly significant compared with the pristine state, the comparison among different doping conditions does not appear to demonstrate effective carrier concentration modulation. The authors need to clarify whether this behavior arises from saturation of the doping effect under the selected conditions or from other underlying mechanisms. If saturation occurs, the doping dose should be reduced (e.g., lower concentration or shorter doping time) to explore the controllable regime. In other words, if the effective doping level cannot be precisely tuned, the limitations of this approach could become significant.

Response to Comment 1: We appreciate the reviewer's constructive comments. The tunability of doping concentration is indeed a critical parameter for the doping process. To address this concern, we have performed additional experiments demonstrating that the doping level in our method can be precisely controlled.

The experimental results are presented in the following Fig. 1. When the concentration of the doping solution is decreased from 0.5% to 0.1%, a distinct positive shift in the threshold voltage is observed, indicating a decrease in the effective doping level. Additionally, to investigate the effect of treatment time, we applied the 0.1% solution and shortened the doping time to 20 s. Under this condition, the threshold voltage shifts even further positively, and the maximum current simultaneously decreases, which verifies that a shorter treatment time leads to a lower effective doping level.

The above results demonstrate that this doping technique is capable of precisely modulating the doping level, laying a foundation for its application. We have incorporated these new experimental results and the discussion of this trade-off into the revised Supplementary Fig. 15b and manuscript section highlighted in yellow.

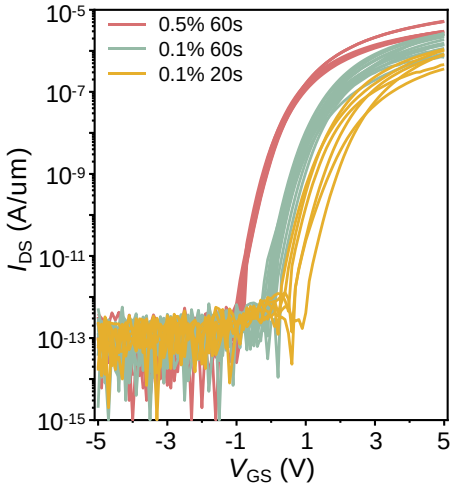

Fig. 1. Effective modulation of the doping level via reduced concentration and shortened treatment time. Transfer characteristics of WSe_2 transistors treated with low concentration solution and short doping duration.

Comment 2: In Figure R4, I note that the pristine maximum current (ID,max) of the 200 nm channel-length devices increases compared with long-channel pristine devices (as shown in Fig. R2 and Fig. 1h), from approximately 10^{-9} A/μm to 10^{-7} A/μm. However, after doping, the maximum current does not improve relative to the results shown in Fig. R2 and Fig. 3a,b; instead, a slight decrease is observed for both p- and n-doped devices. This behavior may reflect scaling-induced limitations during device scaling, and the authors should clarify this point. Furthermore, scaling of channel width should also be experimentally investigated to elucidate potential limitations of the doping strategy. If pronounced scaling-related constraints are observed, they should be explicitly discussed in the manuscript.

Response to Comment 2: The increase in pristine ID,max for the 200 nm devices aligns with standard scaling behavior. However, the slight decrease in doped current density is attributed to fabrication-induced artifacts in short-channel devices, such as increased contact resistance, edge damage, and so on, which imposed constraints on the overall device performance, rather than inherent limitations of the doping strategy. These factors likely obscured the expected doping benefits.

To further address the reviewer's concern regarding the scaling behavior of our doping strategy, we conducted supplementary experiments by varying the channel width from 30 μm down to 0.5 μm (including 5 μm). As illustrated in the updated Fig. 2, no pronounced width-scaling constraints were observed. The current density remained highly consistent across different channel widths, demonstrating the robustness of our doping approach.

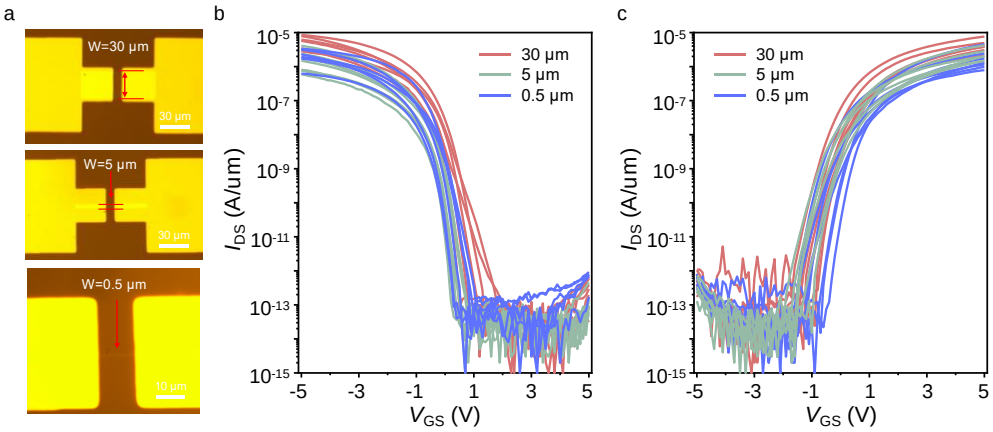

Fig. 2. Channel width scaling of the doped devices with a fixed channel length of 10 μm.
a, Optical micrographs of devices with channel widths of 30 μm, 5 μm, and 0.5 μm. b, c, Transfer characteristics of p-type (b) and n-type (c) doped devices corresponding to the widths in (a).

Comment 3: The authors mention that a 25% dopant concentration leads to degraded device variation. It is strongly recommended that additional experiments be conducted to clarify the direct relationship between doping concentration and variability degradation, so that the trade-off between doping strength and device uniformity can be quantitatively understood.

Response to Comment 3: We sincerely appreciate the reviewer's constructive suggestion. Understanding the trade-off between doping strength and device uniformity is indeed crucial for practical applications. To clarify the direct relationship between doping concentration and variability degradation, we have conducted additional experiments, specifically focusing on treatments with higher concentrations of TMAH solutions.

As shown in Fig. 3a, the transfer characteristics of transistors treated with different doping solution concentrations are presented. Fig. 3b extracts and compares the V_{th} under these different treatment conditions. The results clearly reveal that when the TMAH concentration exceeds 10%, the variability in V_{th} significantly increases as the doping concentration rises.

Based on this finding, combined with our previous experimental results, we strategically selected a lower concentration (e.g., 1%) for the doping process in our study. This choice effectively balances the doping efficiency with device uniformity, ensuring that the treated devices maintain excellent consistency without suffering from variability degradation. We have incorporated these new experimental results and the discussion of this trade-off into the revised Supplementary Fig. 15c, d and manuscript section highlighted in yellow.

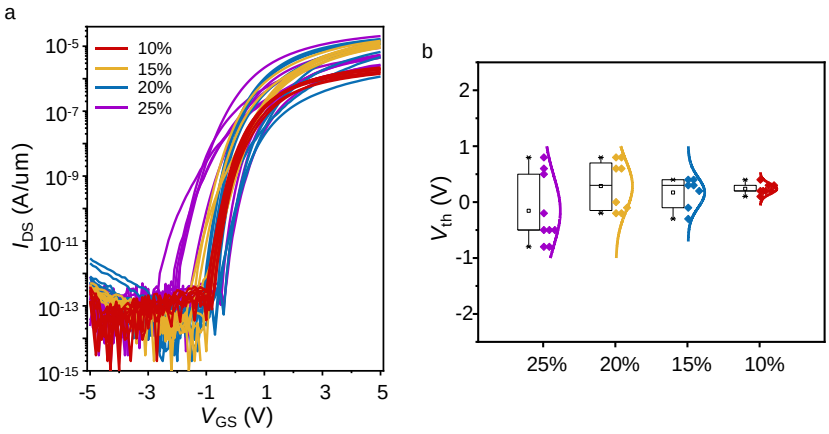

Fig. 3. Fig. 3. Impact of high-concentration TMAH treatment on device variability. a, Transfer characteristics of WSe_2 transistors treated with TMAH solutions ranging from 10 to 25 wt%. b, Statistical distribution of the V_{th} extracted from (a), presented as box plots with corresponding Gaussian fits.

Responses to Reviewer #2

General comment: The authors have made considerable efforts to address the concerns raised during the first round of review, including performing additional experiments and providing additional responses. However, after a careful evaluation of the revised manuscript and the accompanying response letter, I find that several critical issues remain unresolved. Specifically, the fundamental novelty of the doping strategy remains limited, the underlying physical mechanisms are not adequately explained in the revised text, and there are significant performance limitations regarding the operating frequency that contradict the claims of scalability. Furthermore, significant discrepancies exist between the claims made in the rebuttal and the actual content of the revised manuscript. Given the lack of thorough physical analysis and these critical inconsistencies, I believe this work is not suitable for publication in Nature Communications.

General response: We would like to express our deepest gratitude for your continued engagement with our manuscript, and fully respect your rigorous standards for Nature Communications.

First and foremost, we sincerely apologize for the "significant discrepancies" you noted between our rebuttal letter and the revised manuscript. We have carefully re-examined our previous response, and indeed identified several inconsistencies between the reply and the manuscript. We sincerely apologize for this oversight and appreciate your pointing it out. This gave the false impression that we were making claims in the rebuttal that were not supported by the paper. And several strategies are proposed to address the thermal stability and operating frequency bottleneck. We have incorporated these discussion into the revised manuscript section highlighted in blue.

Comment: The core mechanism relies on surface charge transfer doping using WO_4 and $N(CH_3)_4$ functional groups. While presented as a novel breakthrough, adsorption-based doping is a conventional approach in 2D materials research. The manuscript lacks new fundamental physics, charge transport mechanisms, mechanistic explanations for this surface chemistry application. Regarding thermal instability, the authors acknowledge a device failure at 400°C in the rebuttal and state the necessity of "further engineering". However, the revised manuscript merely reports this experimental failure without offering any meaningful discussions, physical analysis, or specific engineering strategies to overcome this limitation. Furthermore, the authors concede in the rebuttal that the limited operating frequency (100 to 500 Hz) is primarily constrained by unoptimized parasitic resistance and capacitance. Relying on long-channel devices with such critical frequency bottlenecks demonstrates that this platform lacks sufficient switching speeds and is not yet ready for realistic large-scale

logic applications.

Response to Comment: We deeply appreciate the reviewer's critical and insightful comments, which have driven us to reflect more profoundly on the scope and limitations of our work. We acknowledge the reviewer's concerns regarding the thermal instability, and the frequency bottlenecks. Below, we address each point systematically:

1. Regarding the novelty and fundamental mechanisms:
We fully agree that adsorption-based doping is a known concept in 2D materials. The primary novelty of this work does not lie in discovering a new physical phenomenon, but rather in proposing a controllable, and dual-mode (p/n) doping strategy utilizing the specific synergistic effect of WO_4 and $N(CH_3)_4$ functional groups. These newly discovered dopants provide a new research perspective for peers to identify more suitable candidates, thereby advancing the development of doping research area in 2D semiconductors.

2. Regarding thermal instability and physical analysis:
We thank the reviewer for the rigorous evaluation, which has inspired a deeper investigation into this issue. We acknowledge that simply reporting the thermal failure at 400°C is inadequate. Consequently, we propose several physically grounded engineering strategies to overcome this limitation and enhance the thermal stability of the doping process, which have been incorporated into the revised manuscript section highlighted in blue:
Enhancing Chemical Adsorption Energy via Defect Engineering: The thermal desorption of dopants is fundamentally limited by the adsorption energy. By introducing controlled Se vacancies on the WSe_2 surface via mild plasma treatment prior to doping, this treatment will provide stronger anchoring sites for the dopants. This shifts the interaction from weak physisorption to stronger chemisorption, thereby raising the activation energy barrier for thermal desorption.

Thermodynamic Optimization of the Doping Solution: Modulate the pH of the solution directly influences the chemical equilibrium. A higher concentration of functional groups in the solution can drive the surface reaction forward more completely, leading to a more robust and densely packed dopants layer that is inherently more resistant to thermal degradation.

Kinetic Suppression via stable Encapsulation: Compared to conventional SiO_2 dielectrics, encapsulating the channel with hexagonal boron nitride (h-BN) or Si_3N_4 provides an additional physical confinement barrier. This effectively suppresses the kinetic processes of dopants diffusion and desorption during thermal annealing.

3. Regarding operating frequency and realistic application limitations:
We have carefully re-examined our previous response, and indeed identified several

inconsistencies between the reply and the manuscript. We sincerely apologize for this oversight and appreciate your pointing it out. We completely concur with the reviewer's assessment. The 100–500 Hz operating frequency is indeed a critical bottleneck, primarily dictated by the large parasitic resistance and capacitance (RC delay) inherent in our current long-channel device architecture (L=10 μm). We admit that this specific platform, in its current long-channel form, is not ready for large-scale high-speed logic applications. To overcome this limitation and achieve high-frequency operation in future work, we propose the following strategies, which have also been incorporated into the revised manuscript section highlighted in blue:
Device Channel Scaling: This is the most critical step. Reduce the channel length (L) using more advanced high-resolution lithography, which will linearly decrease the channel resistance and simultaneously reduce the gate capacitance.

Parasitic Capacitance Reduction: Adopt a self-aligned gate architecture to minimize the overlap capacitance between the gate and source/drain electrodes, thereby reducing the RC time constant.

Contact Engineering: Optimize the metal-semiconductor interface to lower contact resistance will be prioritized to facilitate faster carrier injection, improve the on-state current.

Responses to Reviewer #3

General comment: The authors have addressed all my comments. I recommend acceptance.

General response: We sincerely thank the reviewer for the positive recommendation and for taking the time to evaluate our revised manuscript. We are very glad to know that our revisions have fully addressed your concerns.