Supplementary Information for

Realization of the Bienenstock-Cooper-Munro rule in a single memristor

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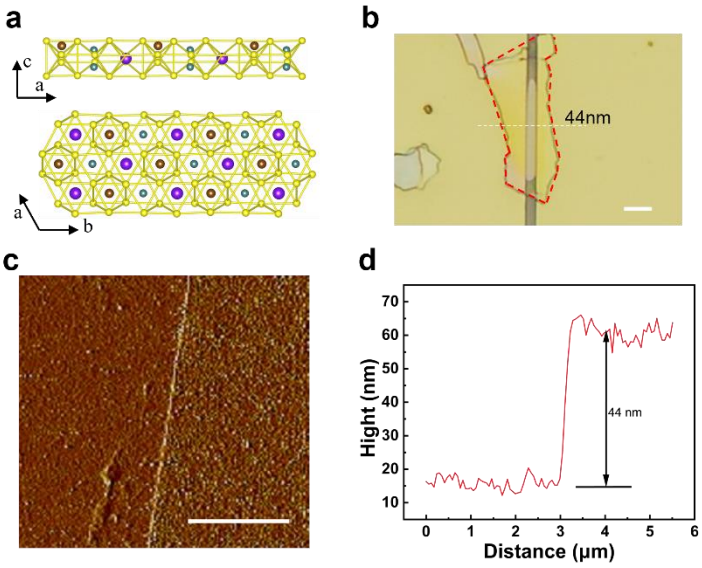
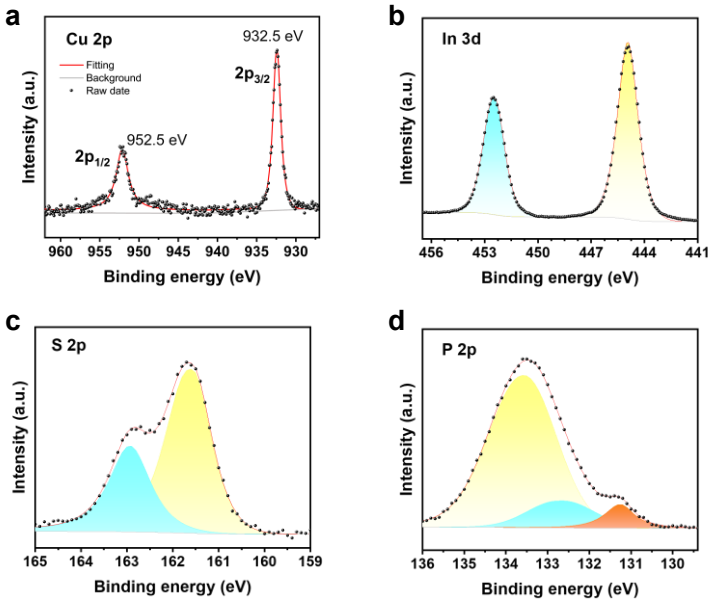
This PDF file includes:

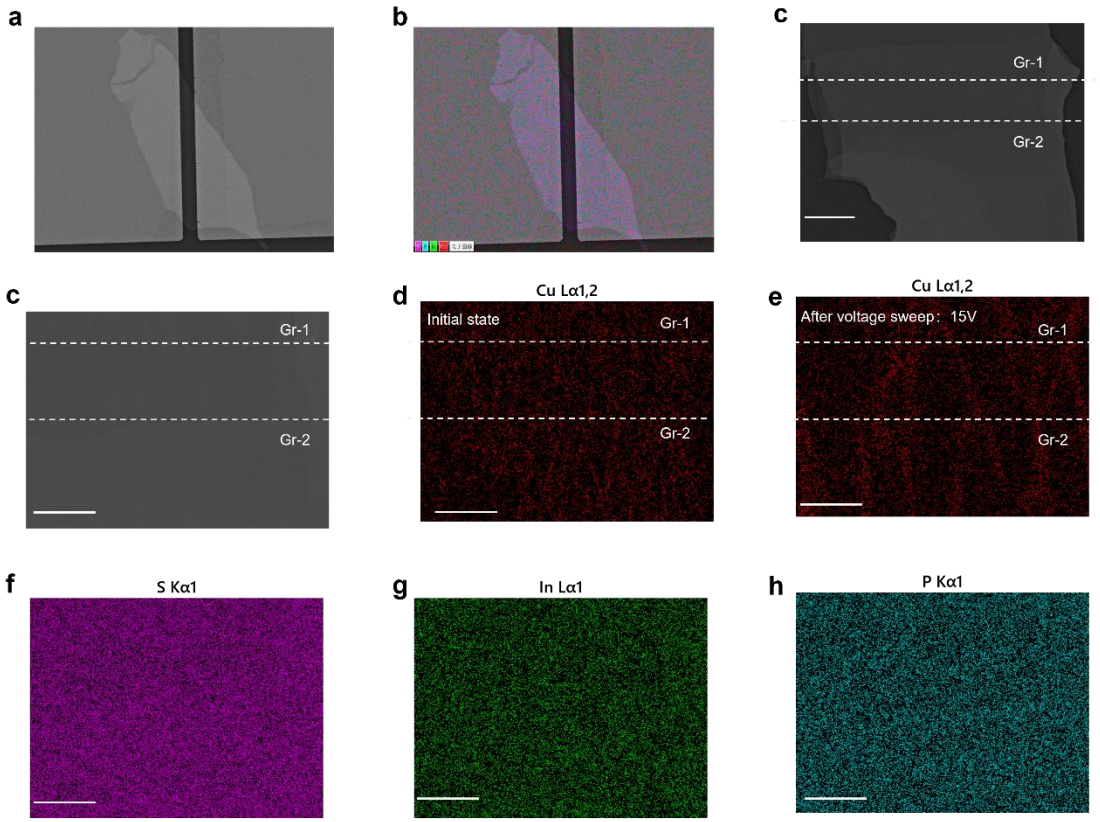
Supplementary Figures



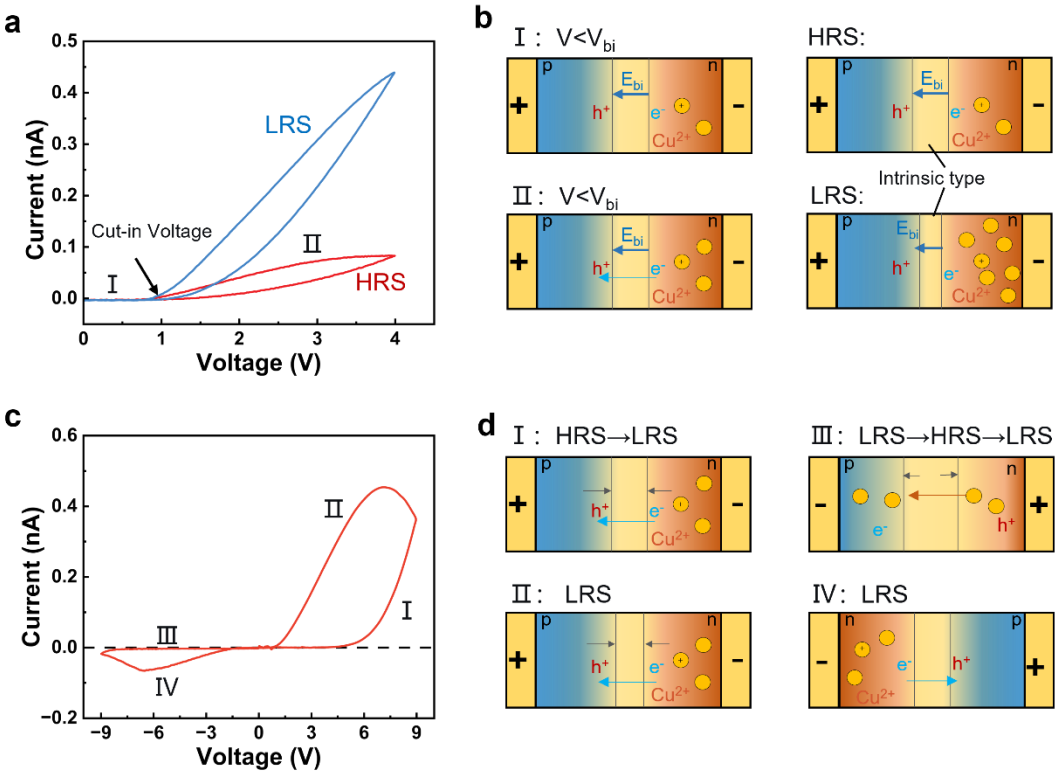
Supplementary Fig. 1 Structure and morphology of the CIPS device. **a** Crystal structure of CIPS. **b** Optical micrograph of CIPS device fabricated via the dry-transfer method, Scale bars: 10μm. **c-d** Surface morphology and thickness (44 nm) characterized by AFM, Scale bars: 3μm.



Supplementary Fig. 2 XPS characterization of CIPS film. **a** High-resolution S 2p spectrum. **b** High-resolution P 2p spectrum. **c** High-resolution Cu 2p spectrum. **d** High-resolution In 3d spectrum. All spectra confirm the presence of S, P, Cu, and In in the CIPS film.

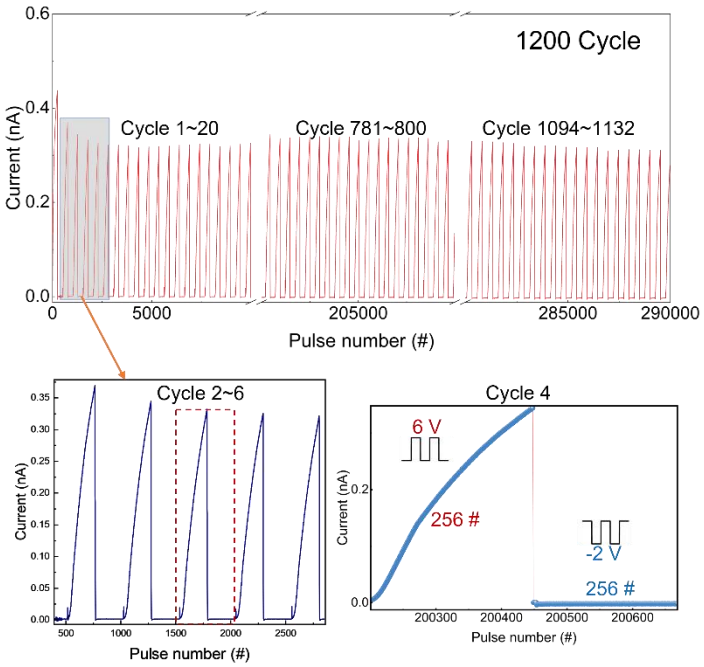


Supplementary Fig. 3 Structural and elemental characterization of CIPS devices. **a** SEM image of an Au/CIPS/Au device, with the CIPS layer located on top of the electrodes, Scale bars: 10μm. **b** EDS elemental maps of the same area, showing the spatial distribution of constituent elements; in this configuration, ion migration cannot be effectively characterized because the conductive channel lies beneath the CIPS layer, Scale bars: 10μm. **c** SEM image of the channel region in a fresh Au/Gr/CIPS/Gr/Au device, where the CIPS layer is placed under the graphene electrodes to expose the channel on the upper surface for ion-migration characterization; the graphene layers are barely distinguishable due to their low SEM contrast, Scale bars: 10μm. **d–e** Evolution of Cu distribution before and after homojunction formation, revealing pronounced Cu aggregation following a 15 V voltage sweep, consistent with previous reports, Scale bars: 2.5 μm.[1, 2, 3] **f–h** Elemental maps of In, P, and S, showing uniform distributions throughout the entire process, Scale bars: 2.5μm.

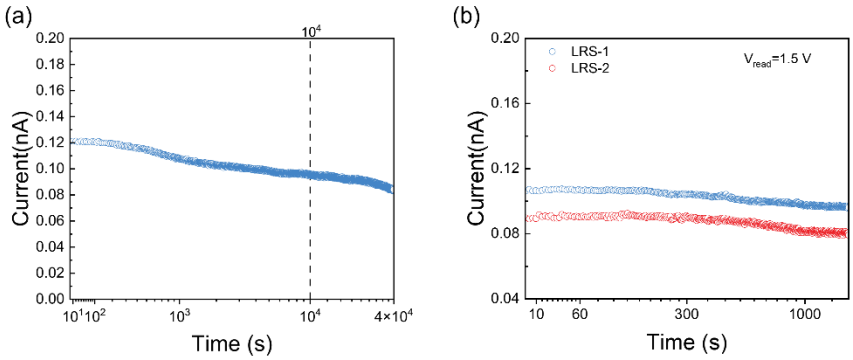


Supplementary Fig. 4 Resistive switching and homojunction behavior in CIPS devices. **a** I–V characteristics under consecutive unidirectional voltage sweeps, showing distinct LRS and HRS conductance with a clear forward cut-in voltage indicative of p–n junction formation. **b** Schematic of the conduction and resistive switching mechanisms in the CIPS memristor. **c** Homojunction switching I–V curve divided into four characteristic stages. **d** Schematics of the homojunction evolution at each stage, highlighting Cu^{+} migration-induced modulation of junction properties.

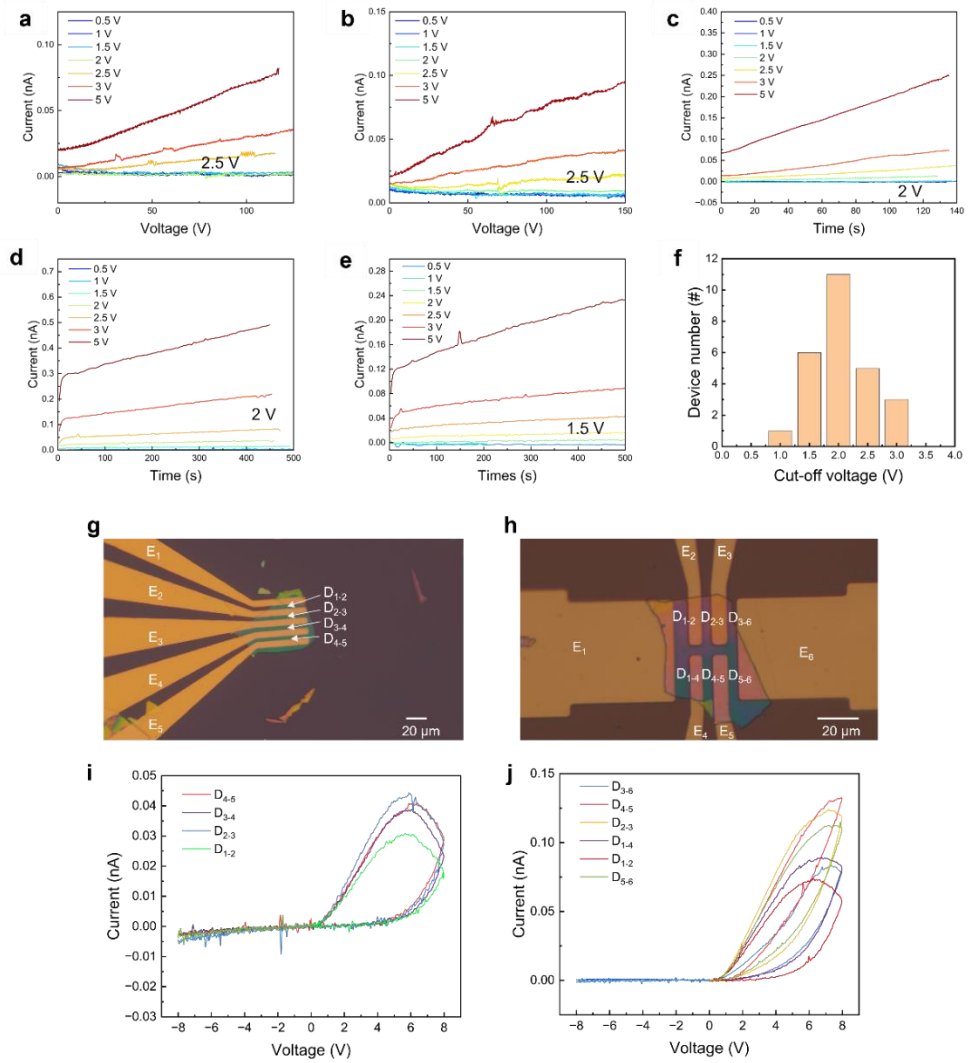
Supplementary Fig. 4 Resistive switching and homojunction formation in the CIPS device



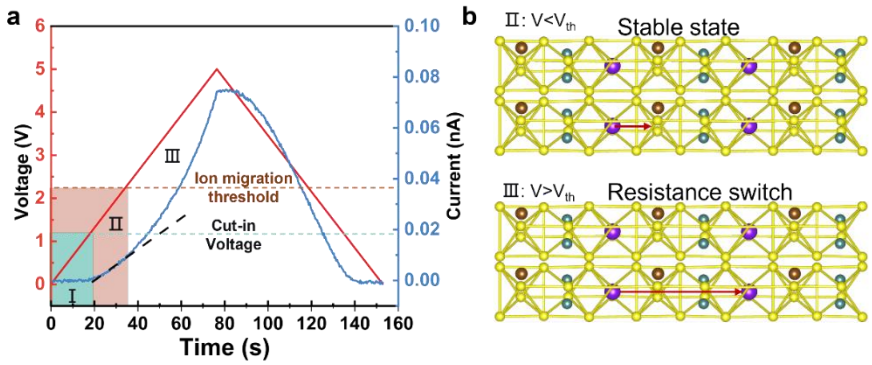
Supplementary Fig. 5 Reversible switching stability of the CIPS memristor over 1200 cycles. Conductance modulation by alternating pulse trains of 256 positive pulses (6 V, 1 s) for potentiation and 256 negative pulses (−2 V, 1 s) for depression, with each set corresponding to one cycle. The device exhibits stable, reversible switching over 1200 consecutive cycles (~300,000 individual pulses) without observable performance degradation. A detailed view of selected cycles is shown in the inset.



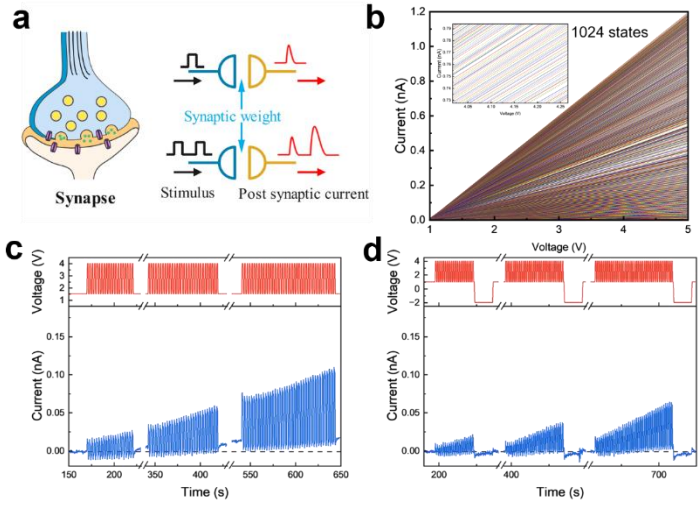
Supplementary Fig. 6 Retention characteristics of the CIPS device in the LRS. **a** LRS programmed by a 15 V voltage sweep and continuously read at 2 V; the conductance remains stable over 40,000 s, demonstrating excellent non-volatile retention. **b** Two distinct LRS conductance states remain clearly distinguishable after 1000 s, confirming the multilevel storage capability of the device.



Supplementary Fig. 7 Resistive switching characteristics and threshold voltage statistics. **a**–**e** Resistive switching behaviour of five representative devices: **a**, **b** Devices 1 and 2 (channel width = 5 μm, thickness = 42 nm); **c** Device 3 (channel width = 5 μm, thickness = 54 nm); **d** Device 4 (channel width = 4 μm, thickness = 52 nm); **e** Device 5 (channel width = 3 μm, thickness = 52 nm). **f** Statistical distribution of threshold voltages across 26 devices (channel width = 5 μm). **g**, **i** Optical microscope image and basic I–V characteristics of a 1×4 device array. **h**, **j** Optical microscope image and basic I–V characteristics of a 2×3 device array.

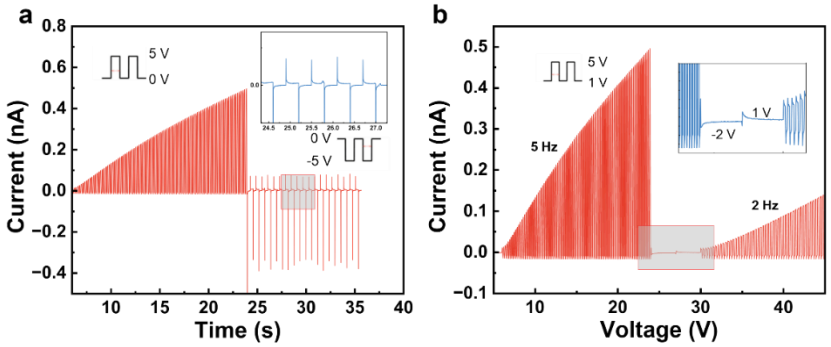


Supplementary Fig. 8 Ion migration threshold and mechanism in the CIPS device. **a** I–V sweep (0 → 5 → 0 V) showing three characteristic regions: near-zero current below the cut-in voltage, linear current between the cut-in and migration threshold voltages indicating a stable conductance state, and marked conductance increase above the migration threshold; the safe readout window lies between the cut-in and threshold voltages. **b** Schematic of the ion migration mechanism: below the threshold, Cu^{+} ions remain confined within S octahedral cages, ensuring device stability; above the threshold, long-range ion migration occurs, enabling conductance modulation.

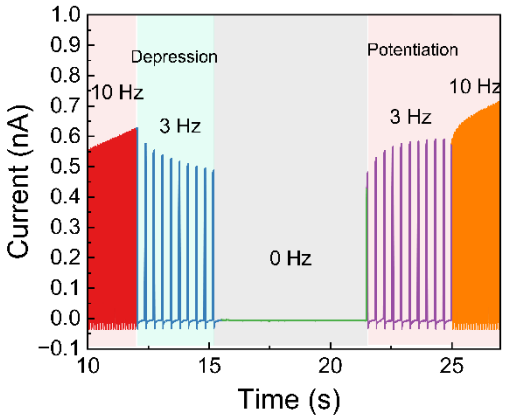


Supplementary Fig. 9 Synaptic behavior of the CIPS memristor. **a** Schematic of a biological synapse and its weight-modulation process. **b** Multi-level conductance modulation under pulsed stimulation (1–5 V, 1 Hz, 500 ms), achieving 1024 stable, nearly linear conductance states, each programmed and read with 5 V pulses. **c** Continuous programming under repeated pulse trains (1.5–4 V, 0.5 Hz,

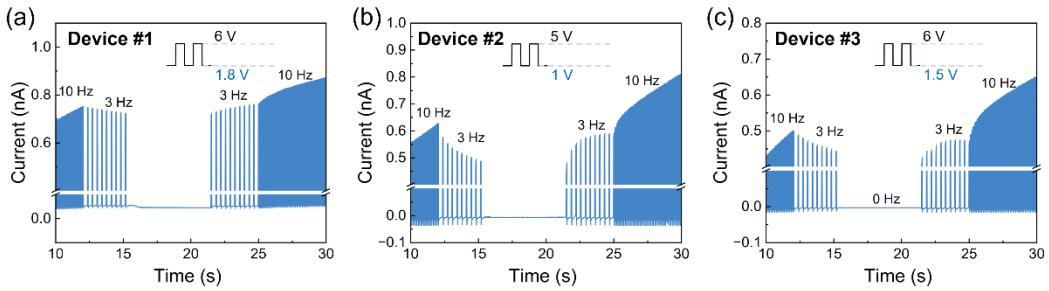
1000 ms) with 20, 30, and 40 pulses applied sequentially at 100 s intervals, showing cumulative conductance enhancement. **d** Demonstration of conductance-state erasability by a −2 V reset bias after pulsed programming.



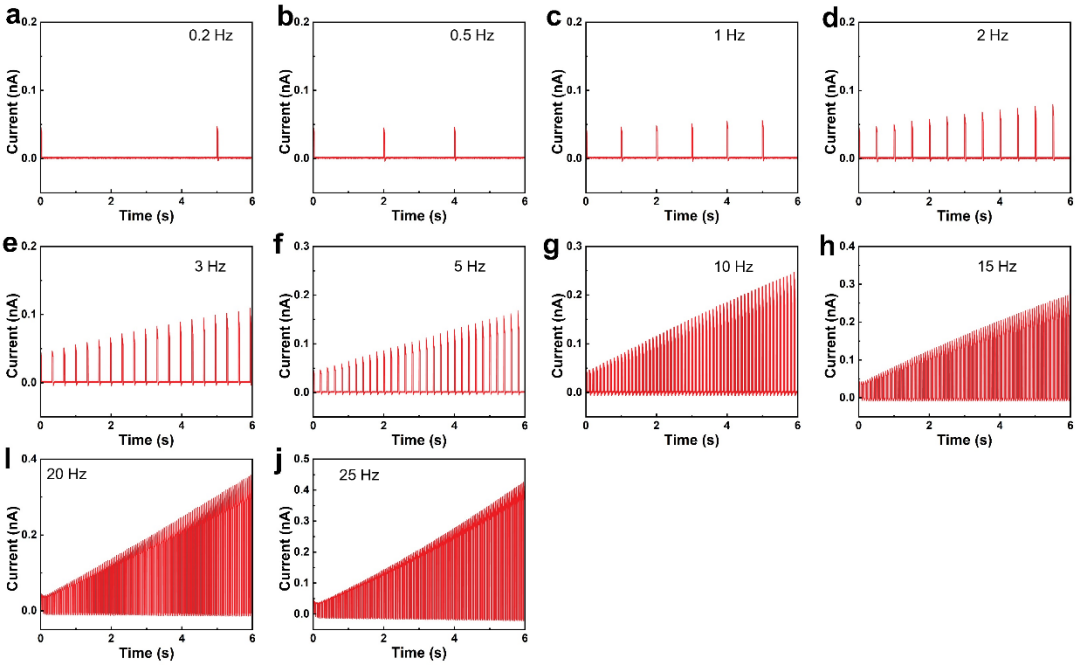
Supplementary Fig. 10 Asymmetric potentiation and depression in the CIPS memristor. **a** Conductance evolution under consecutive positive (5 V, 1 Hz, 500 ms) and negative (−5 V, 1 Hz, 500 ms) pulse trains; positive pulses induce clear potentiation, while negative-pulse depression is suppressed by the rectifying p–n homojunction. **b** Rapid conductance erasure under a −2 V bias in the LRS, confirming efficient and asymmetric modulation.



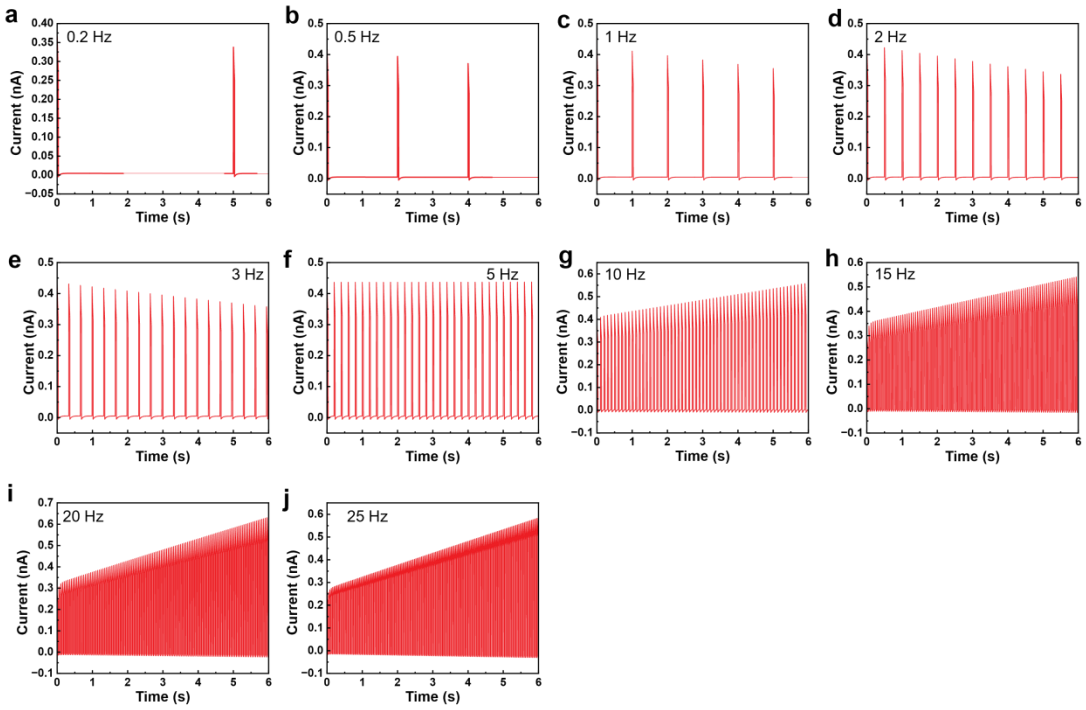
Supplementary Fig. 11 Device response to continuous pulse trains at 10, 3, 0, 3 and 10 Hz (1–5 V, 50 ms). The response to 3 Hz stimuli shifts between potentiation and depression depending on prior activation history. When the 2 Hz pulses were replaced with a constant 1 V bias (0 Hz), the device conductance remained stable.



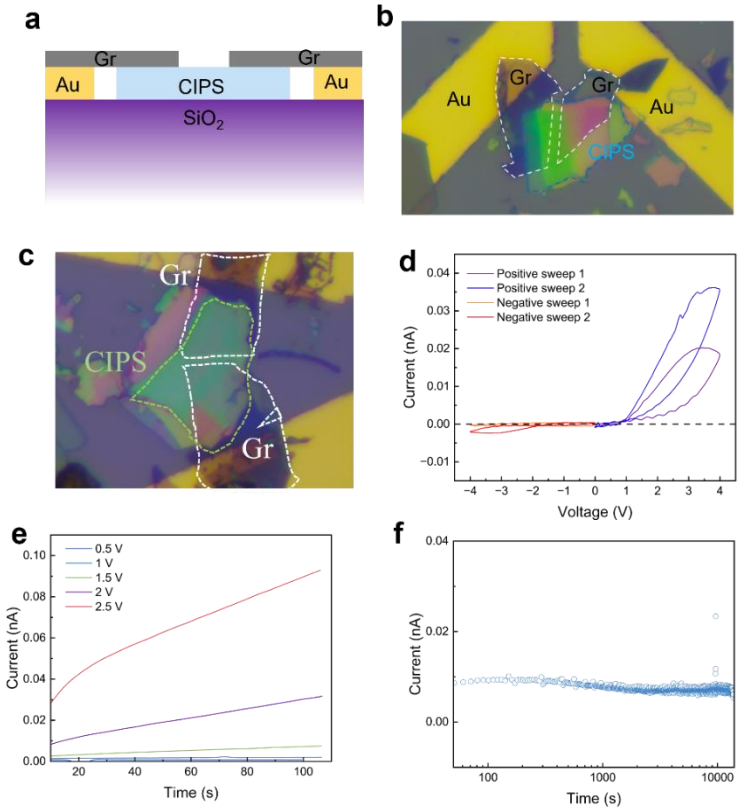
Supplementary Fig. 12 BCM rule under continuous pulse trains at 10, 3, 0, 3 and 10 Hz (pulse width 50 ms). **a** Device 1 (threshold ~2.5 V): low level 1.8 V, high level 6 V. **b** Device 2 (threshold ~1.5 V): low level 1 V, high level 5 V. **c** Device 3 (threshold ~2 V): low level 1.5 V, high level 6 V.



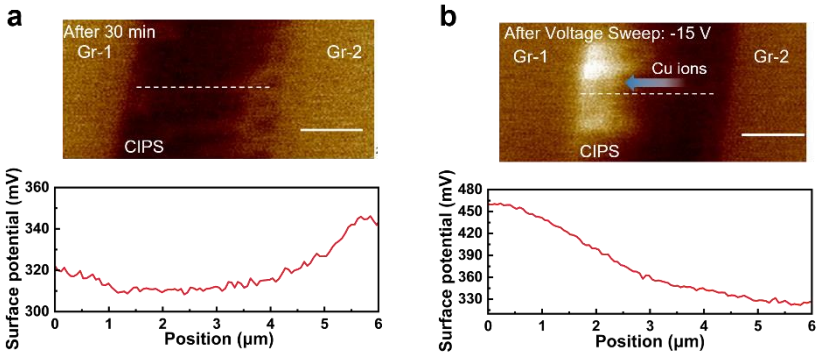
Supplementary Fig. 13 SRDP characterization of CIPS memristors. Devices were fully reset by a −2 V pulse, pre-stimulated for 20 s with a 0 Hz spike train, and then tested with spike trains at 0.2–25 Hz (pulse width 30 ms, 5 V high level, 1 V low level). Relative conductance change $\Delta G = (G_{5s} - G_{0s})/G_{0s}$ was evaluated at 5 s. **a–j** Conductance variation under test frequencies of 0.2, 0.5, 1, 2, 3, 5, 10, 15, 20, and 25 Hz, respectively, following the 0 Hz pre-stimulation (initial state).



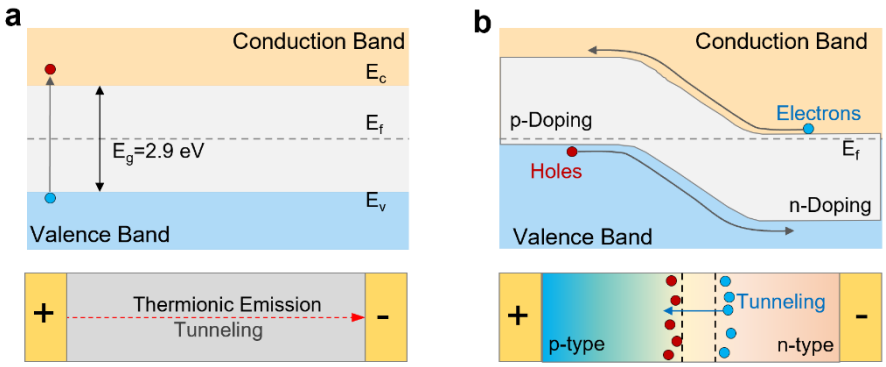
Supplementary Fig. 14 SRDP of CIPS memristors after 25 Hz pre-stimulation. Devices were fully reset and pre-stimulated with a 25 Hz spike train (20 s, pulse width 30 ms, 5 V high, 1 V low). Relative conductance change $\Delta G = (G_{5s} - G_{0s})/G_{0s}$ was evaluated at 5 s. **a–j** Conductance variation under test frequencies of 0.2, 0.5, 1, 2, 3, 5, 10, 15, 20, and 25 Hz, respectively.



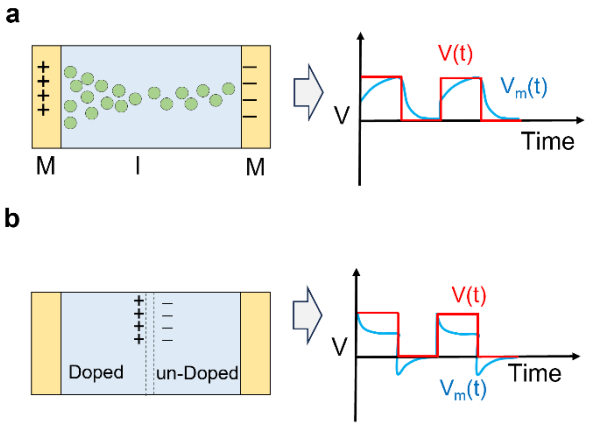
Supplementary Fig. 15 Device structure for SEM and KPFM characterization. **a** Schematic illustration of the Au/Gr/CIPS/Gr/Au device, with the conductive channel placed on the top surface to facilitate surface-sensitive measurements. **b** Optical microscopy image of a fabricated device, showing a channel width of 6 μm. **c** Optical microscopy image of another device, showing a channel width of 5 μm. **d** I–V curve of the Au/Gr/CIPS/Gr/Au structure. **e** Voltage bias test of the same structure. **f** Retention test of the Au/Gr/CIPS/Gr/Au structure.



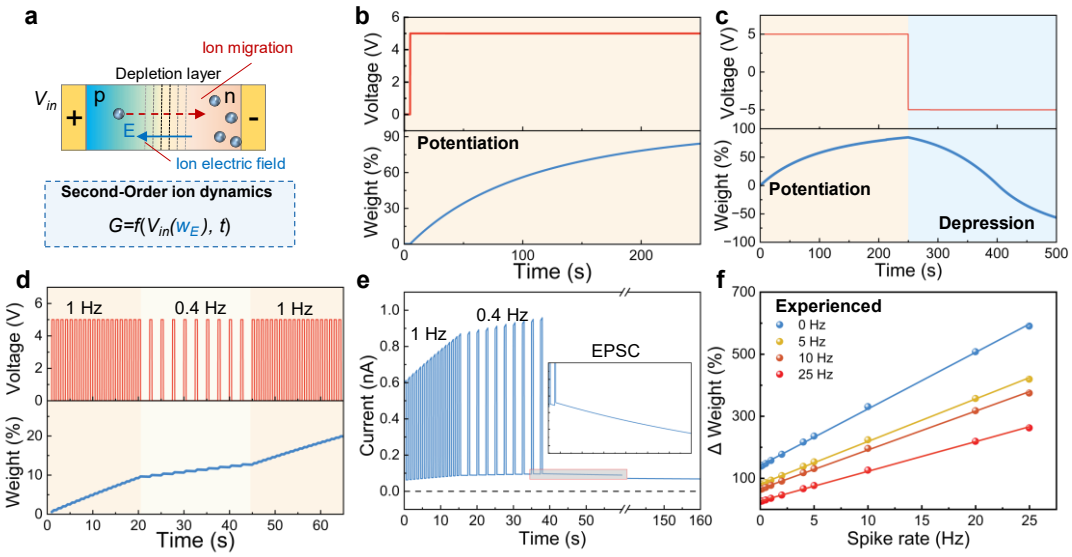
Supplementary Fig. 16 KPFM characterization of the CIPS device. **a** Potential map acquired after 30 min of relaxation, Scale bars: 3μm. **b** Potential map after a subsequent −15 V voltage sweep, revealing the evolution of surface potential associated with ion redistribution, Scale bars: 3μm.



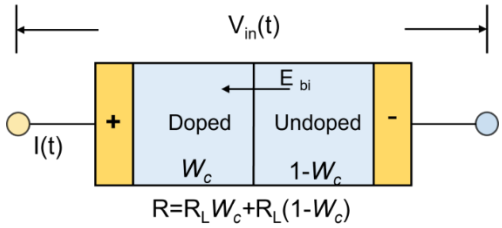
Supplementary Fig. 17 Band diagrams and conduction mechanisms of the CIPS memristor. **a** Pristine state: CIPS acts as a wide-bandgap (~2.9 eV) semiconductor, with conduction dominated by thermionic emission and tunneling. **b** After Cu^+ migration: a p–n homojunction forms, and a wide-bandgap intrinsic region persists due to the Cu^+ concentration gradient, allowing electron tunneling to sustain current flow.



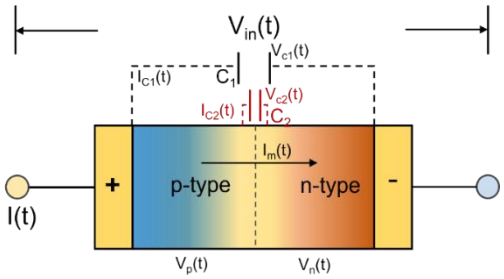
Supplementary Fig. 18 Parasitic capacitance in CIPS memristors versus classical parasitic capacitance. **a** In conventional memristors, parasitic capacitances at metal–insulator interfaces are electrically equivalent to capacitors in parallel with the device; their charging and discharging mainly smooth the applied pulses and cannot induce conductance suppression. **b** In CIPS memristors, the parasitic capacitance originates from the internal p–n homojunction as a depletion-layer capacitance, generating transient reverse-voltage impulses between spikes that enable frequency-dependent depression. The interfacial parasitic capacitance is several orders of magnitude smaller than the junction capacitance and can be safely neglected.



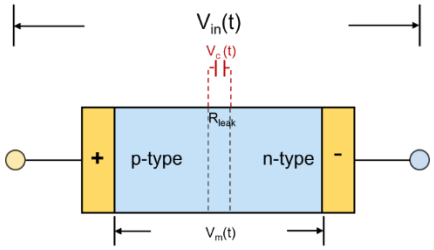
Supplementary Fig. 19 Ion dynamics modeling and simulation of the CIPS memristor. **a** Schematic and dynamic model of a second-order memristor based on CIPS. **b** Simulated conductance enhancement under a 5 V DC bias, with conductance normalized as synaptic weight. **c** Simulated conductance potentiation and depression under bidirectional DC voltage sweeps. **d** Simulated conductance response to pulse stimuli at different frequencies. **e** Implementation of the BCM rule using the CIPS ion dynamics model, demonstrating sliding threshold behavior under varied historical pulse stimuli.



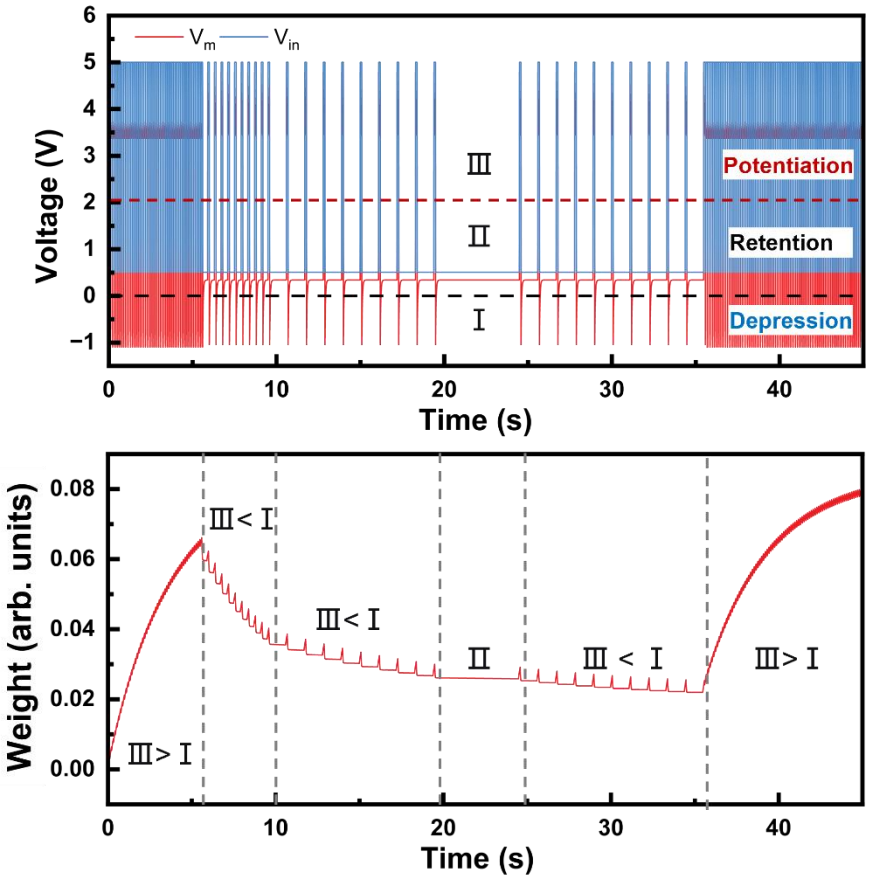
Supplementary Fig. 20 Memristor model based on second-order ion dynamics. The model describes resistive switching via coupled ionic dynamics with two state variables: Wi(t), the normalized Cu^+ migration extent (0–1) that directly determines conductance, and Ei(t), a slowly evolving built-in electric field that provides negative feedback and history dependence. The dynamical system was solved numerically in MATLAB using a time-stepping method with a step size of 0.001 s, and initial conditions were set to experimentally measured as-fabricated values.



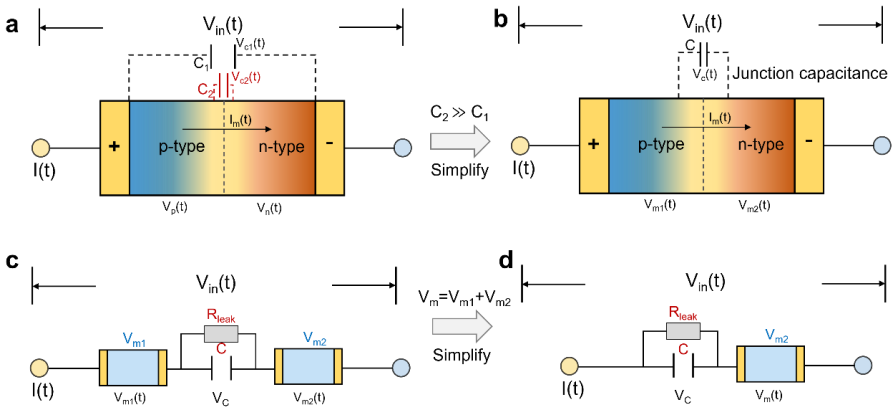
Supplementary Fig. 21 Voltage redistribution effect induced by parasitic capacitance in the CIPS memristor. Parasitic capacitance in CIPS arises from two sources: interfacial capacitance (C_1) at the metal–semiconductor contact and junction capacitance (C_2) across the p–n homojunction. C_1 behaves as a series capacitor, while C_2 is intrinsic to the device. Under pulsed stimulation, voltage redistribution across these capacitances modulates ionic migration, leading to frequency-dependent conductance modulation.



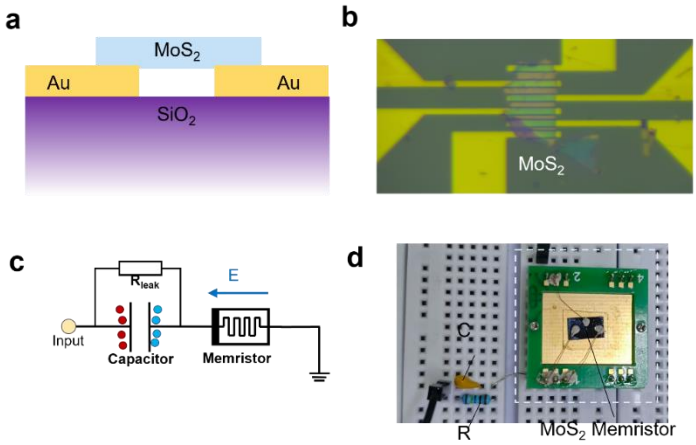
Supplementary Fig. 22 Parasitic capacitance model of the CIPS memristor. The device is modeled as a memristor in series with a junction capacitance (the dominant parasitic element arising from the internal homojunction), while the much smaller interfacial capacitance is neglected. Under pulse stimulation, the capacitor voltage evolves dynamically, determining the effective voltage across the memristor that drives ionic migration. An iterative time-stepping simulation updates the capacitor and memristor voltages at each step, and the resulting M–RC model reproduces the transient charge–discharge behavior and frequency-dependent conductance modulation, capturing the enhanced depression effect observed experimentally.



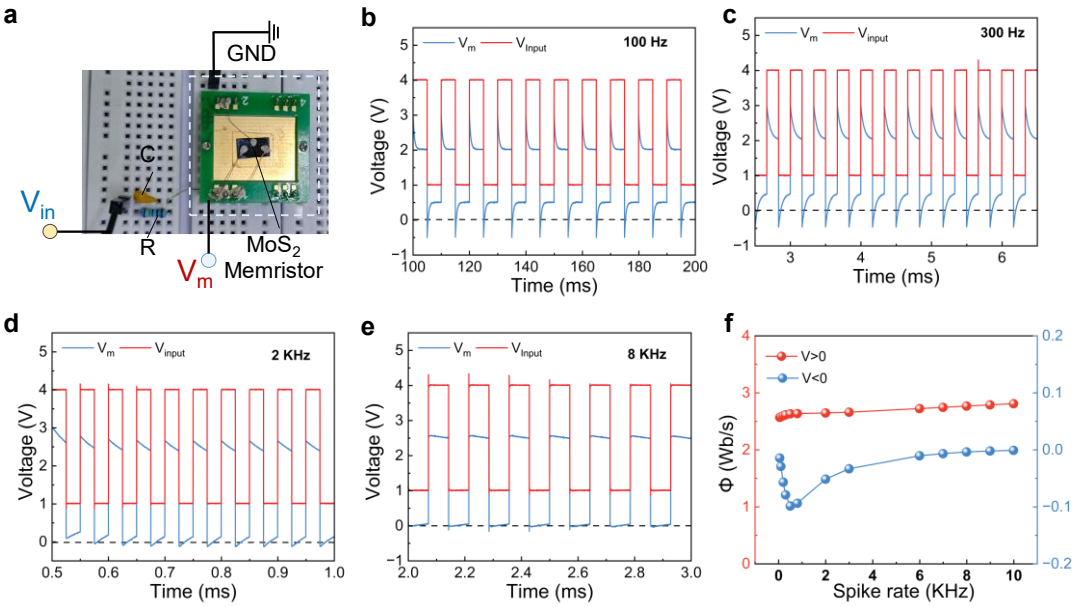
Supplementary Fig. 23 Frequency-dependent mechanism of CIPS devices (simulation) Simulations combining the second-order ion-dynamics model with the junction parasitic capacitance illustrate the device response under varying pulse frequencies. The upper panel shows the input spike trains and the corresponding mixed voltage waveforms across the memristor after redistribution due to the junction capacitance. Based on the ion migration threshold, a voltage of 2 V was defined as the threshold, below which ion migration is minimal. The lower panel depicts the real-time normalized conductance evolution under the mixed pulses. At high frequencies, potentiation dominates over suppression, resulting in an increase in conductance, whereas at low frequencies, suppression prevails. In the absence of input pulses, the conductance remains stable. The simulated conductance dynamics also reproduce the EDE observed experimentally.



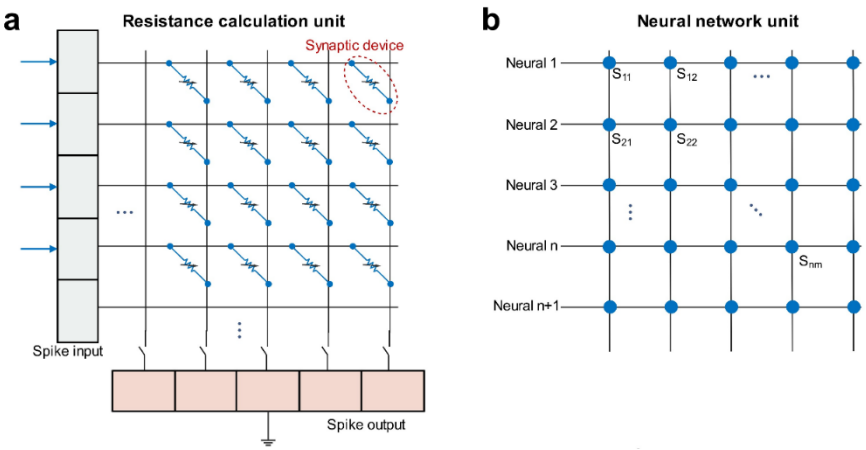
Supplementary Fig. 24 CIPS memristor and MRC equivalent circuit. **a–b** Schematic illustration of parasitic capacitances in the CIPS device; the interfacial parasitic capacitance is negligible compared with the junction capacitance and is omitted. **c–d** Equivalent circuit representation; owing to the structural symmetry of the device, the system simplifies to a memristor–resistor–capacitor (MRC) circuit.



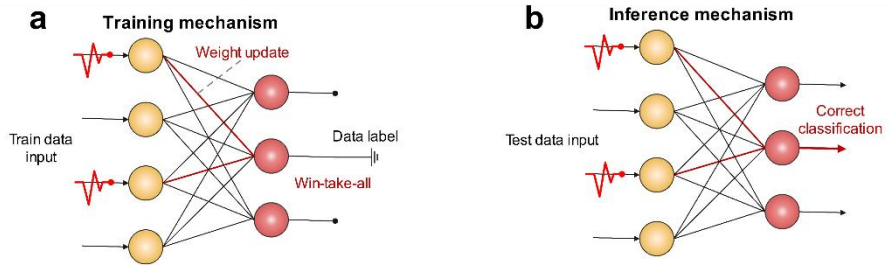
Supplementary Fig. 25 Equivalent circuit based on the MoS_2 memristor. **a** Schematic of the MoS_2 memristor device structure. **b** Optical microscopy image of the MoS_2 memristor. **c** Schematic diagram of the MRC (memristor–resistor–capacitor) circuit. **d** Experimental MRC circuit constructed with a MoS_2 memristor, incorporating a 1 MΩ resistor and a 37 pF capacitor.



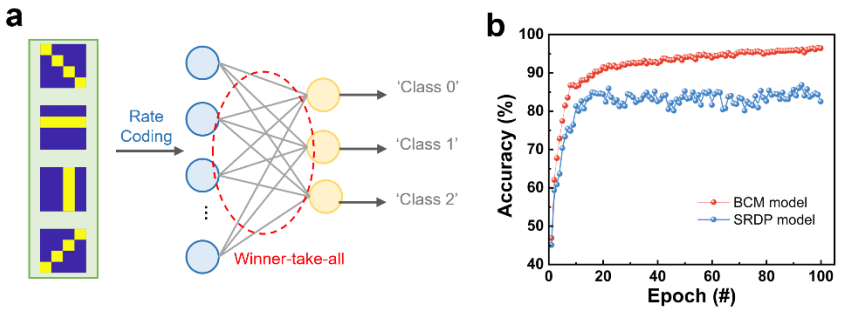
Supplementary Fig. 26 Voltage redistribution effect of MRC circuits based on MoS_2 memristors. **a** Schematic of the junction capacitance in CIPS and the equivalent MRC circuit. **b–e** Filtering outcomes under pulse stimuli at 100 Hz, 300 Hz, 2 kHz, and 8 kHz. **f** Statistics of forward and backward rectification as a function of pulse frequency.



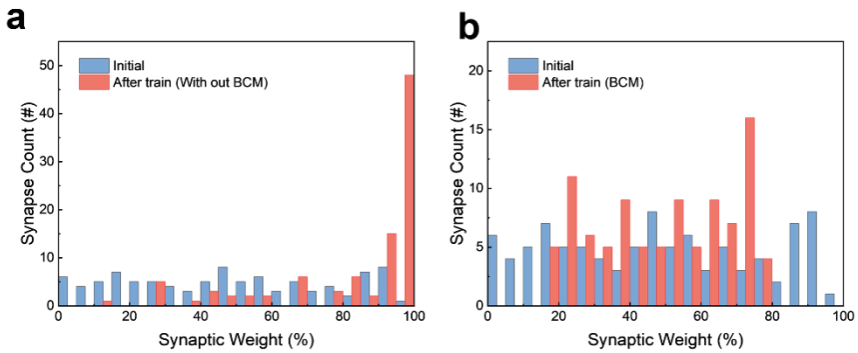
Supplementary Fig. 27 Schematic diagram of the memristor array–based circuit. **a** Crossbar array with horizontal input lines delivering spike signals as presynaptic neurons, and transistor-based switches at the outputs acting as postsynaptic neurons; conductance modulation occurs only when both are simultaneously activated, mimicking synaptic plasticity. **b** Basic neural network unit where each synapse performs weighted summation of presynaptic signals and forwards the result to the next neuron layer.



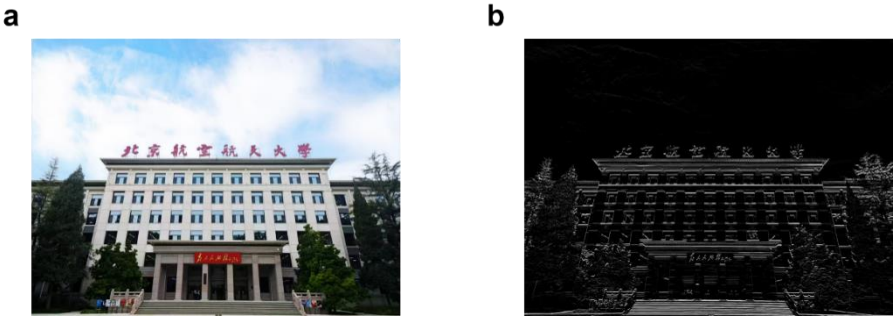
Supplementary Fig. 28 Training and inference process based on the winner-take-all rule. **a** Training phase: image data of dimension (m,n) are encoded as $m \times n$ spike trains with frequencies 0–15 Hz (pulse width 50 ms, duration 3 s); the output terminal corresponding to the correct label is grounded while others float, strengthening synaptic connections to the correct neuron. **b** Inference phase: test data are encoded identically with spike amplitudes below the modulation threshold; all outputs measure response currents, and the terminal with the highest current is selected as the predicted label.



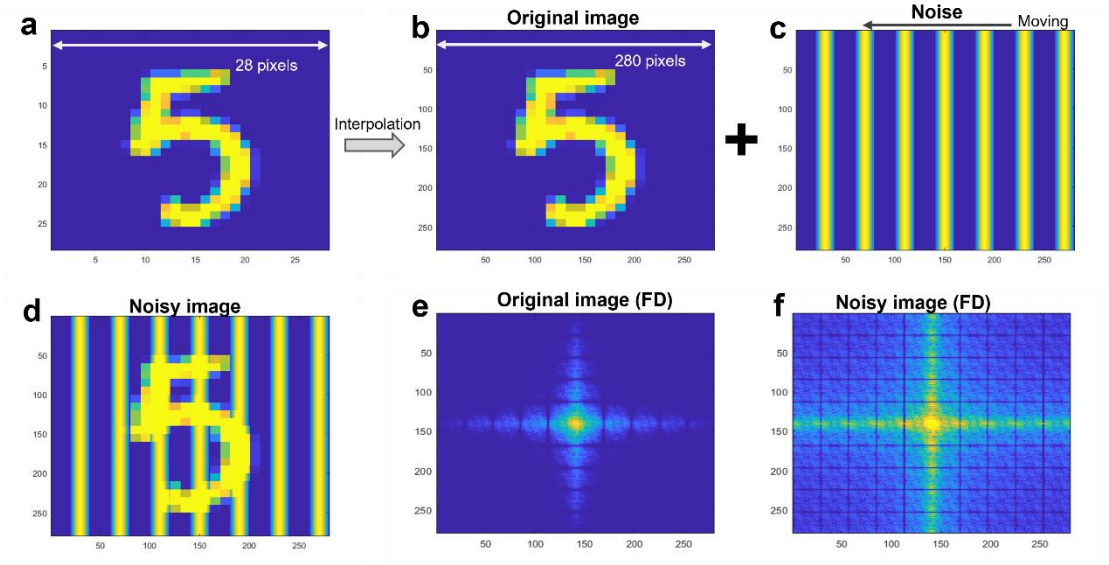
Supplementary Fig. 29 Simulation of orientation selectivity using a spike-rate-based BCM model. **a** A custom dataset of 1000 images (4×4 pixels, three orientation categories) is encoded into spike trains and processed by a single-layer classifier; the monotonic SRDP model follows first-order ion dynamics, while the BCM rule introduces a homeostatic threshold. **b** Classification accuracy during training: the monotonic SRDP model fails to converge, whereas the BCM rule exhibits stable and progressive accuracy improvement.



Supplementary Fig. 30 Weight evolution of the neural network before and after training. **a** Synaptic weight distribution under the SRDP rule at the initial state and after 100 epochs, with random initial weights and 10% Gaussian input noise; severe weight saturation is observed after training. **b** Weight distribution under the BCM rule with identical training conditions, remaining uniform and demonstrating improved stability and self-regulation of synaptic plasticity.



Supplementary Fig. 31 High-pass filtering based on the physical reservoir using the BCM rule. **a** Original image. **b** Image processed by the reservoir: input transformed to the frequency domain, filtered, and reconstructed to the spatial domain, demonstrating edge enhancement and the high-pass filtering capability of the BCM-based physical reservoir.



Supplementary Fig. 32 Construction of the striped-noise dataset based on MNIST. **a** Original MNIST image (28 × 28 pixels).[4] **b** Image up-sampled to 280 × 280 pixels by nearest-neighbor interpolation. **c** Randomly generated movable striped noise patterns. **d** Noisy video frame created by superimposing striped noise onto the original image. **e** Frequency-domain representation of the original image via FFT, showing feature information concentrated in the low-frequency region. **f** Frequency-domain image of a noisy video frame, with noise components distributed mainly in the high-frequency region.

Supplementary Tables

Supplementary Table 1 Simulation parameters of ion dynamics for CIPS memristor

Parameters	Values
Normalized state variable	[-1,1]
μ_+ ($V>V_{th}$)	0.00001/Vs
μ_0 ($0<V<V_{th}$)	0.000002/Vs
μ_- ($V<0$)	0.00005/Vs
k	0.000005/Vs
HRS	$1\times10^{11}\Omega$
LRS	$1\times10^{9}\Omega$
L	1μm
α	1
β	1
γ	1

Supplementary Table 2 Simulation parameters of the parasitic capacitor effect

Parameters	values
C	1×10^{-10} F
R_m	1×10^{9}~$1\times10^{11}\Omega$
R_{leak}	$5\times10^{10}\Omega$

Supplementary Notes

Supplementary Note 1. Mechanism of CIPS memristors and parasitic homojunctions

Supplementary Figure 4 provides a detailed illustration of the resistive switching behavior and the formation–reconfiguration mechanism of the homojunction in CIPS devices. As shown in Supplementary Fig. 4a, the electrical response of CIPS can be divided into two distinct regimes. In region I (below the cut-in voltage), the current remains nearly zero, indicating the presence of a depletion barrier. In region II, the device exhibits a typical memristive hysteresis loop. The schematic in Supplementary Fig. 4b depicts the origin of the cut-in voltage: once a p–n homojunction forms, electrons and holes diffuse toward the n- and p-type regions, respectively, establishing an internal built-in electric field. Significant current conduction occurs only when the applied voltage exceeds this built-in potential.

Due to the Cu^+ concentration gradient, a wide-bandgap intrinsic region inevitably exists within the p–n junction, serving as the main transport barrier and contributing to the high device resistance (on the order of 10^{10} Ω) even under forward bias. During the transition from HRS to LRS, the increased local doping concentration narrows this intrinsic region, enhancing carrier tunneling and resulting in a gradual increase in conductance. This process likely underpins the intrinsic RS behavior of CIPS memristors.

To elucidate the formation and reconfiguration of the homojunction, Supplementary Fig. 4c presents a full bidirectional I–V sweep, which can be divided into four stages, as illustrated in Supplementary Fig. 4d. In Stage I (0 → 9 V), Cu^+ ions drift toward the right electrode, forming a p–n homojunction and progressively increasing conductance. In Stage II (9 → 0 V), ion migration ceases, and the device remains in the forward-biased p–n LRS state. In Stage III (0 → −9 V), the reverse bias first suppresses current, restoring the device to HRS, and subsequently drives Cu^+ ions toward the left electrode, forming an n–p homojunction and a new forward LRS. Finally, in Stage IV (−9 → 0

V), ion migration slows down, stabilizing the n–p configuration.

Within the framework of memristor systems, the rectifying behavior induced by the CIPS homojunction can be regarded as a parasitic effect that significantly influences the overall RS dynamics. The built-in electric field formed in the junction not only affects charge transport but also introduces frequency-dependent inhibitory dynamics. Thus, while the homojunction complicates the conventional RS process, it also provides the physical foundation for the emergence of the frequency-dependent depression effect (EDE) and the spontaneous realization of the BCM learning rule in CIPS memristors.

Supplementary Note 2 Parasitic Capacitance in CIPS Memristors

To quantitatively evaluate the parasitic capacitance in the CIPS memristor, single-pulse stimulation was employed, and the transient discharge response was analyzed. Specifically, a voltage pulse (typically 2-15 V, 3,000 ms) was applied to the device, and the subsequent current spike observed during the voltage fall (discharge) phase was recorded. The effective parasitic capacitance C_p was then estimated by integrating the area under the discharge current transient according to:

$$C_p = \frac{1}{V}\int I(t)dt$$

where V is the voltage step amplitude, and $I(t)$ is the transient current. This method captures both the interfacial capacitance at the metal–semiconductor contact (C_1) and the junction capacitance arising from the p–n homojunction (C_2), which are difficult to isolate under standard DC measurement conditions. This pulse-based integration approach provides a straightforward and effective means to probe capacitive contributions in memristor systems without requiring impedance spectroscopy. It directly reflects the capacitive charge–discharge dynamics that occurs during device operation and can be applied under realistic pulsed conditions relevant to neuromorphic applications.

Using the above method, the capacitance of the CIPS device was extracted under

various voltage conditions. A linear relationship was observed between the integrated charge and the applied voltage (Q-U), confirming the presence of a stable capacitive element in the CIPS device. From the relation C = Q/U, the estimated capacitance is approximately 12.1 pF. In contrast, the capacitance estimated using a parallel-plate model—assuming a device width of 20 μm, thickness of 40 nm, channel width of 5 μm, and a dielectric constant of approximately 300 for CIPS—yields a value of 0.21 fF.[5]

$$C = \varepsilon\varepsilon_0 \frac{S}{d}$$

his is considerably smaller than the 12.1 pF obtained from electrical measurements, with a discrepancy of about four orders of magnitude. (Detailed calculation steps are provided in the Supporting Information.) Such a pronounced difference suggests that the capacitance in CIPS originates from a mechanism distinct from conventional interfacial capacitance.

Supplementary References

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