nature portfolio

Peer Review File

Realization of the Bienenstock-Cooper-Munro rule in a Single Memristor

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Parts of this Peer Review File have been redacted as indicated to remove third-party material.

This file contains all reviewer reports in order by version, followed by all author rebuttals in order by version.

Version 0:

Reviewer comments:

Reviewer #1

(Remarks to the Author)
This manuscript reports a two-terminal $CuInP_2S_6$ (CIPS) memristor that is claimed to realize the Bienenstock–Cooper–Munro (BCM) rule under natural spike-rate coding for the first time. This is not true. Similar reports already exist for oxide materials, perovskite materials, two-dimensional materials, and other nanomaterials based memristor, and the literature has demonstrated BCM functionality and even device arrays in all of these material systems, like John et al., Adv. Electron. Mater. 2024, 2400612; Sci. Adv. 8, eade0072 (2022); Nature Communications (2022) 13:5585; Nature Communications (2020) 11:1510; Adv. Mater. 2024, 36, 2404160; Adv. Funct. Mater. 2024, 34, 2314660; Adv. Funct. Mater. 2022, 32, 2108440. There are many other references related to this research topic and the author may could find them. Considering the novelty of this work, this reviewer cannot recommend this work at this stage. Moreover, there are several technical issues should be addressed.
(1) How do the authors define “complete” BCM? which specific features or operations are mandatory, differ from other reported works? Under this definition, why do previous BCM-like two-terminal implementations not qualify as “complete”?
(2) Many previous memristive BCM demonstrations also use natural spike-rate coding. In what precise sense is your “natural spike-rate coding” different from conventional rate coding reported?
(3) As for the quantitative justification of the large junction capacitance, the extracted capacitance is said to be “substantially larger” than a parallel-plate estimate. Please provide the actual parallel-plate value (with the assumed effective area and thickness) and the ratio between measured and estimated capacitance.
(4) Can authors provide device-to-device statistics for this capacitance to demonstrate reproducibility?
(5) The authors attribute the large capacitance to minority-carrier accumulation (diffusion capacitance) in the p–n homojunction. Have the authors performed frequency-dependent C(f) C(f) measurements to distinguish diffusion capacitance from interfacial capacitance? and any systematic C–V or C–F data in both the LRS and HRS states?
(6) The manuscript states that approximately 2 V is the threshold for Cu^+ migration. a) Is this threshold consistent across different flake thicknesses and device batches? What is the error range? Could the authors provide a simple Arrhenius-type fitting or comparison to show that this threshold corresponds to an energy barrier consistent with the reported ionic migration barrier of CIPS in the literature?
(7) As for the formula (3), the value GL and GH representing the initial and saturated conductance of the device, are from single device or obtained by fitting which specific experimental curves? Are they extracted from a single device or averaged over multiple devices? How does device-to-device variability affect the BCM curves? Do the authors have error bars or statistical information to show this?
(8) The authors use a MoS_2 memristor plus an external RC network to reproduce the experiments and verify the generality of the strategy. a) Besides MoS_2, have you also verified this approach on other types of memristors (for example, oxide-based devices or PCM)? b) How are the parameters of the external RC chosen to match the intrinsic time scales of the device? If they are not well matched, how would the EDE regime change?
(9) Junction-capacitance-driven EDE may be affected by process variations and parasitic parameters in practical chip fabrication: a) Have you evaluated the impact of process variations in Cj and Rleak on the stability of the BCM curves? b) If the junction capacitance of each cell in an array differs by a factor of 2–3 or more, can stable performance still be achieved through array-level training?

(Remarks on code availability)

Reviewer #2

(Remarks to the Author)
In this manuscript, Huang et al., used CuInP2S6-based two-terminal memristor to emulate spike-rate dependent synaptic plasticity, especially the BCM rule. The authors demonstrated that the synaptic plasticity of the memristor was affected by the history of previously applied pulses. The authors assumed this effect was due to negative capacitive feedback current formed by the p-n homojunction in the CIPS layer. The authors also demonstrated physical reservoir computing based on the CIPS memristor model developed in this work. Although this work shows the possibility of emulating BCM rule, one of the most accurate models explaining biological synapse, there is a significant gap between the authors' claim and their experimental results. Furthermore, the experimental data in the figures cannot support that this CIPS-based memristor follows the BCM rule and shows enhanced depression effect. The reviewer suggests the following comments.

1.In Figure 2g, the authors mentioned retention characteristics of the CIPS memristor when a read voltage lower than the threshold is applied during the retention period. However, in Supplementary Figure 8c, there is no change in electrical current after 100 s of interval, which contradics with Figure 2g. The reviewer asks the author for further clarification.

2. In Figure 3d, the authors showed that the direction of conductance change is affected by the previous spike rate by comparing the current change when applying a 3 Hz pulse after applying two different spike trains. The reviewer wonders, based on the EDE explanation, when a 2 Hz spike train is applied (green colored), the device should show depression since lower spike rates of pulses were applied compared to the previous spikes (3 Hz). However, in Fig. 3d, devices shows potentiation while applying a slower spike train of 2 Hz. The reviewer thinks this figure is critical for verifying the CIPS device's emulation of the BCM rule, but the reviewer cannot be fully persuaded. The reviewer asks the author for an explanation for this.

3. In Figure 3f, the authors showed a sliding threshold, similar to the BCM rule, demonstrating that the threshold frequency, determining potentiation or depression behavior of the CIPS memristor is affected by the presynaptic spike frequency. Based on the BCM rule, the threshold should increase proportionally to the historical spike rate. However, in Figure 3f, the threshold spike rate of the memristor with historical spike rates of 5 Hz and 10 Hz looks identical. The reviewer suggests that the authors provide more quantitative and systematic analysis for the emulation of the BCM rule in the CIPS memristor. Furthermore, based on the figure caption, experienced stimulation at 25 Hz should also be presented in Figure 3f, but it's missing.

4. The reviewer requests to authors provide more statistical results, especially the EDE verification shown in Figure 3. In the current figure, it looks like the results were obtained from a single device, so showing reproducibility would further enhance the manuscript.

5. Based on the KPFM measurement, the surface potential of the CIPS memristor in LRS shows linearly incrase as a function of lateral distance, indicating ion distribution due to the external electrical field. The review thinks this KPFM image contradicts the authors' explanation shown in Fig. 4f, which requires a distinct depletion region in the middle. Could this capacitive current originate from the interfacial electrical double layer (EDL) formed between the CIPS layer and the left or right contact electrode?

6. In the manuscript, the authors mentioned the CIPS memristor can be operated in two distinctive modes: non-volatile memory arrays for the readout layer and dynamic modes for the physical reservoir. The reviewer thinks the experimental verification of the CIPS' dynamic modes for the physical reservoir is lacking in the current manuscript. Based on Fig. 2g, 3b, and Supplementary Figure 6, 8, the CIPS memristor showed long-term potentiation behavior, not dynamic memristive behavior, which requires that devices should return to the HRS state quickly. The reviewer suggests that the authors provide experimental demonstration showing CIPS memristor can behave like a dynamical memristor to utilize it as a physical reservoir. Hence, the reviewer thinks it is not logical to use the CIPS memristor as a physical reservoir for the reservoir computing framework.

7. The detailed explanation of Fig. 5 is missing. Based on the contents in the manuscript and Supplementary Information, the reviewer thinks all data in Fig.5 were generated using simulation-based modeling of the behavior of CIPS memristor, not using physical devices. However, in the manuscript, this is not clear, which makes the reader confused. The reviewer suggests that the authors clarify this and add detailed modeling and simulation methods in the Methods section or Supplementary Information.

(Remarks on code availability)

Reviewer #3

(Remarks to the Author)
This manuscript reports the realization of the complete Bienenstock-Cooper-Munro (BCM) synaptic plasticity rule in a single

two-terminal memristor based on $CuInP_2S_6$ (CIPS). The BCM rule, a biologically inspired model, incorporates spike-rate-dependent plasticity with potentiation at high spike rates, depression at low rates, a sliding frequency threshold modulated by activity history (for homeostatic regulation), and an enhanced depression effect (EDE) at very low rates to prevent unchecked weight decay. The authors leverage the intrinsic properties of the CIPS memristor: second-order ionic dynamics (Cu^+ migration and built-in field feedback) for threshold sliding, and a junction parasitic capacitance that generates reverse voltage spikes during pulse intervals, enabling spike-rate-dependent depression and spontaneous EDE under natural spike-rate coding. No external gates, load resistors, or specialized encoding are required.

Here are some concerns:
1. Exfoliated flake is used, which limits scalability.
2. Limited endurance/reliability data: Only ~20 homojunction cycles shown; no extensive endurance tests (e.g., 10^6 pulses) or variability across devices (e.g., flake-to-flake stats). CIPS is vdW material, prone to defects/air sensitivity—how robust is it long-term?
3. Lateral structure (5 μm channel) is bulky for dense arrays; vertical stacking or integration with CMOS isn't addressed. Parasitic capacitance (~12 pF) might scale poorly or introduce crosstalk in crossbars.
4. Retention is only tested to 3600 s; claims of non-volatility need longer tests (> 10^4 s) or acceleration studies.
5. Could interfacial defects contribute to the switching?
6. EDE is pulse-induced, not spontaneous decay, but low-frequency depression (31% vs. 5% at 0 Hz) implies some volatility; reconcile with non-volatile claims?

(Remarks on code availability)

Version 1:

Reviewer comments:

Reviewer #1

(Remarks to the Author)
The authors have addressed most of the issues. However, I recently came across a published paper titled 'Polymorphic Functionalization Driven by Ion Displacement-Induced Antiferroelectric Ordering in $CuBiP_2Se_6$,' which demonstrates that the BCM rule can be enabled by antiferroelectric materials. In contrast, the implementation of the BCM rule in the current manuscript relies on ferroelectric materials. Therefore, the authors should explicitly discuss the differences between their study and this recent publication. Specifically, what are the advantages of utilizing ferroelectric materials for the BCM rule compared to antiferroelectric materials?

The addtional comments for cross-check are shown below:

1. Other Reviewer's Comment: Exfoliated flake is used, which limits scalability.
My response:
Regarding the scalability issue, exfoliated flakes are commonly used in 2D materials research. While this approach inherently limits scalability, this is a well-known challenge for the entire 2D materials community rather than a flaw to be completely resolved in a single paper. Nevertheless, to adequately address Reviewer #3's concern, it would be advisable for the authors to fabricate and demonstrate a small device array.
2. Other Reviewer's Comment: Limited endurance/reliability data: Only ~20 homojunction cycles shown; no extensive endurance tests (e.g., 10^6 pulses) or variability across devices (e.g., flake-to-flake stats). CIPS is vdW material, prone to defects/air sensitivity— how robust is it long-term?
My response:
I agree with this comment. It is understandable that 2D materials lose their advantage in scalability; however, in my opinion, for fundamental research, the adequate performance parameters of a single device should still be demonstrated.

3. Other Reviewer's Comment: Lateral structure (5 μm channel) is bulky for dense arrays; vertical stacking or integration with CMOS isn't addressed. Parasitic capacitance (~12 pF) might scale poorly or introduce crosstalk in crossbars.
My response:
While I agree that the authors should address the parasitic capacitance issue, I consider the other points raised in this comment to be beyond the scope of the current work
4. Other Reviewer's Comment: Retention is only tested to 3600 s; claims of non-volatility need longer tests (> 10^4 s) or acceleration studies.
My response:
I agree this reviewer.

5. Other Reviewer's Comment: Could interfacial defects contribute to the switching?
My response:
I agree with the reviewer. The authors should clarify this point to better explain the working mechanism.

6. Other Reviewer's Comment: EDE is pulse-induced, not spontaneous decay, but low-frequency depression (31% vs. 5% at 0 Hz) implies some volatility; reconcile with non-volatile claims?
My response:

I agree with the reviewer on this point. The authors should provide a clear explanation to address this concern.

Reviewer #2

(Remarks to the Author)
The authors properly addressed most of the Review#3's comments, but I still have some concerns.

In the revised Supplementary Figure 6, the authors provided a longer retention test to reply the Reviewer #3's comment (comment 4). However, based on the figure, the current from the memristor indeed decreases over time, and it gets worse when measured up to 4 x 104 s. The reviewer thinks this is the inherent limitation of ion-based two-terminal devices, as the ion can spontaneously diffuse back when there is no external field. A similar short retention time also can be found in other ion-based memristive devices (Onen et al., Science, 277, 2022). In the current revised version, the authors only showed two conductance states, so it might not be an issue, but this degradation can be an issue if we want to store multiple bits of information into this device. The reviewer concerns that the author overclaimed the retention behavior of their CIPS-based devices.

Another point is that the Reviewer #3 pointed out the long channel length (5 μm) of the current devices. The authors replied that this device is a prototype, and scaling the device is not in the scope. However, the reviewer thinks that since their device uses ion diffusion in the lateral direction, if the channel length gets shorter for higher scalability, the retention time will become even worse due to shorter diffusion length. Based on the author's reply to the Reviewer #3's comments, the reviewer further raises the retention issue of this CIPS memristor if the channel lengths get shorter.

Since the authors used lateral-type devices, the operating frequency is quite low (max 25 Hz) and the pulse width is quite long (minimum 30 ms). The reviewer suggests the authors provide discussion to increase the operation frequency of the devices and lower the pulse width of the devices.

Version 2:

Reviewer comments:

Reviewer #1

(Remarks to the Author)
The authors have addressed all the concerns from this reviewer.

Reviewer #2

(Remarks to the Author)
My comments have been addressed adequately.

Dear All:

We sincerely thank the editors and all reviewers for their valuable feedback. The manuscript "Realization of the Bienenstock-Cooper-Munro rule in a Single Memristor" (NCOMMS-25-099372-T) is revised. The responses to the reviewers' comments are listed as following:

Reviewer #1:

This manuscript reports a two-terminal $CuInP_2S_6$ (CIPS) memristor that is claimed to realize the Bienenstock–Cooper–Munro (BCM) rule under natural spike-rate coding for the first time. This is not true. Similar reports already exist for oxide materials, perovskite materials, two-dimensional materials, and other nanomaterials based memristor, and the literature has demonstrated BCM functionality and even device arrays in all of these material systems, like John et al., Adv. Electron. Mater. 2024, 2400612; Sci. Adv. 8, eade0072 (2022); Nature Communications (2022) 13:5585; Nature Communications (2020) 11:1510; Adv. Mater. 2024, 36, 2404160; Adv. Funct. Mater. 2024, 34, 2314660; Adv. Funct. Mater. 2022, 32, 2108440. There are many other references related to this research topic and the author may could find them. Considering the novelty of this work, this reviewer cannot recommend this work at this stage. Moreover, there are several technical issues should be addressed.

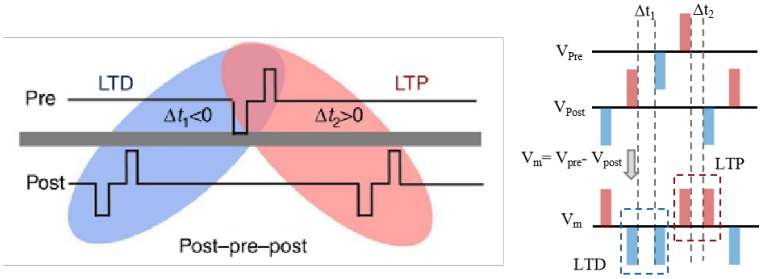
Response: We sincerely thank the reviewer's thoughtful comments and constructive criticism. We fully understand the concern regarding the novelty claim and would like to clarify the key distinctions between our work and the cited literatures. After a thorough analysis, we respectfully maintain that our claim—the first realization of the full BCM rule (including EDE) under ***natural spike-rate coding*** in a single two-terminal memristor—remains valid. The key distinction lies in the coding strategy, which we clarify below.

Coding strategies	Features	References
Spike-rate coding (SRDP)	Only threshold sliding	Adv. Funct. Mater. 2015, 25, 4290–4299 Adv. Funct. Mater. 2018, 28, 1706927 Adv. Funct. Mater. 2019, 29, 1807316 ACS Appl. Mater. Interfaces 2020, 12, 50061−50067 IEEE Transactions on Electron Devices. 2023, 12: 6301-6306
Spike-time coding (Triplet-STDP)	Threshold sliding + EDE	Nat. Commun. (2020) 11:1510; Nat. Commun. (2022) 13:5585 Sci. Adv. 8, eade0072 (2022) ACS Appl. Mater. Interfaces 2023, 15, 5456−5465 Adv. Electron. Mater. 2024, 2400612 IEEE Electron Device Letters 2025 46: 2042-2045
Spike-voltage coding (SVDP)	Threshold sliding + EDE	Adv. Funct. Mater. 2024, 34, 2314660 Adv. Mater. 2024, 36, 2404160
Additional gate coding	Threshold sliding + EDE	Adv. Funct. Mater. 2022, 32, 2108440 Nature 2023 Vol. 624:551-556
Spike-rate coding (SRDP)	Threshold sliding + EDE	This work

The original BCM rule is a model of synaptic plasticity induced by stimulation at spike-rate coding. Early memristor-based BCM implementations successfully demonstrated threshold sliding under spike-rate coding (Adv. Funct. Mater. 2015, 25, 4290; Adv. Funct. Mater. 2018, 28, 1706927; Adv. Funct. Mater. 2019, 29, 1807316; ACS Appl. Mater. Interfaces 2020, 12, 50061; IEEE Trans. Electron Devices 2023, 12, 6301). However, due to the inherent monotonic spike-rate response of conventional

memristors, the second essential feature of the BCM rule—non-monotonic EDE behavior—could not be achieved in those studies.

In 2020, Wang et al. introduced a Triplet-STDP coding scheme and, for the first time, demonstrated EDE-like behavior in WO_x memristors using carefully designed spike patterns (Nat. Commun. 2020, 11, 1510). Subsequent studies have adopted this encoding strategy to mimic EDE in various memristor systems (Nat. Commun. 2022, 13, 5585; Sci. Adv. 2022, 8, eade0072; ACS Appl. Mater. Interfaces 2023, 15, 5456; Adv. Electron. Mater. 2024, 2400612; IEEE Electron Device Lett. 2025, 46, 2042). However, this approach presents several critical limitations:



The triplet-STDP coding (a redefined spike-rate coding)

1. **Deviation from biological spike-rate coding**: Triplet-STDP redefines "spike-rate" based on the time intervals of specially designed spike triplets. This encoding scheme does not correspond to the continuous spike-rate stimulation that defines natural rate coding in biological systems.
2. **Lack of non-volatility**: According to the original BCM theory (Nat. Rev. Neurosci. 2012, 13, 798), EDE requires synaptic weights to remain stable in the absence of input (0 Hz). Triplet-STDP-based demonstrations do not satisfy this criterion, as they only consider isolated spike triplets and do not account for device behavior under continuous stimulation or idle periods.
3. **Practical applicability in SNNs**: Current spiking neural network (SNN) systems primarily rely on temporal coding or natural rate coding (spike count per unit time). Triplet-STDP, voltage coding, or additional gate control are not directly compatible with standard SNN architectures and would introduce prohibitive circuit complexity—especially at the array level.

In contrast, our CIPS memristor achieves both threshold sliding and EDE under natural

spike-rate coding without any external encoding circuitry. The device inherently generates a reverse voltage spike via its parasitic junction capacitance, which introduces a spike-rate-dependent depression that saturates at high frequencies. This mechanism enables: potentiation at high frequencies; depression at low frequencies; stable conductance at 0 Hz. It fully complies with the EDE behavior as defined in the BCM framework. Moreover, this intrinsic strategy is directly compatible with SNN rate-coding schemes, offering a hardware-efficient and biologically plausible solution.

We acknowledge that our initial wording in the introduction may have been understated, potentially leading to the misunderstanding that we were dismissing all prior work. We have now revised the introduction to more clearly articulate the distinction between natural spike-rate coding and Triplet-STDP-based approaches, and to properly contextualize our contribution within the existing literature.

We thank the reviewer for pushing us to refine our novelty claim and for helping us strengthen the manuscript. We hope this clarification addresses the concern.

(1) How do the authors define “complete” BCM? which specific features or operations are mandatory, differ from other reported works? Under this definition, why do previous BCM-like two-terminal implementations not qualify as “complete”?

Response: We thank the reviewer for raising this important question, and we will clarify this definition below. In our manuscript, the definition follows that widely adopted in the literature (Nat. Commun. 2020, 11, 1510; Adv. Funct. Mater. 2024, 34, 2314660; Adv. Funct. Mater. 2022, 32, 2108440), namely, a complete BCM rule must exhibit two essential features:

(1) Threshold sliding—the frequency threshold for potentiation/depression adapts based on prior activity.

(2) Non-monotonic EDE behavior—depression strengthens at intermediate frequencies but weakens at very low or very high frequencies, with stable conductance at zero input.

We do not claim that previous implementations are “incomplete”. Rather, we respectfully note that due to the intrinsic monotonic frequency response of conventional memristors (rooted in their flux–charge dynamics), achieving the EDE feature has remained a challenge. In prior reports, non-monotonic EDE-like behavior was typically obtained by introducing specialized encoding schemes (e.g., Triplet-STDP, Additional gate coding) that effectively redefine spike-rate, rather than by modifying the intrinsic device properties.

By contrast, our work leverages the inherent parasitic junction capacitance of the $CuInP_2S_6$ (CIPS) memristor, which generates a reverse voltage spike during pulse intervals. This built-in mechanism introduces intrinsic non-monotonicity, enabling the device to emulate the complete BCM rule—including EDE—under natural spike-rate coding, without any external encoding circuitry.

We have revised the introduction (page 3) to articulate this distinction more clearly, emphasizing both the definition of a complete BCM rule and the novelty of our intrinsic

approach. We thank the reviewer for helping us sharpen this critical point.

Location of Change: Introduction, page 3:

As illustrated in Fig. 1b, synaptic weight in the BCM rule is determined by spike rate, where high rates induce synaptic potentiation and low rates result in depression. The complete BCM rule encompasses two key features: threshold sliding and a non-monotonic enhanced depression effect (EDE). Threshold sliding refers to the dynamic modulation of the frequency threshold based on the history of neuronal activity, while EDE describes the phenomenon where depression is strongest at intermediate spike rates but weakens at low rates. Threshold sliding can be emulated by second-order memristors that involve a spontaneous relaxation process.[19-21]

(2) Many previous memristive BCM demonstrations also use natural spike-rate coding. In what precise sense is your "natural spike-rate coding" different from conventional rate coding reported?

Response: We thank the reviewer for this important question. The term "natural spike-rate coding" in our manuscript refers to conventional rate coding as defined in neuroscience—information is encoded solely by the number of spikes per unit time, with fixed pulse voltage and width.

To the best of our knowledge, no previous study has demonstrated the full BCM rule (including EDE) under this natural spike-rate coding. As summarized in Table 1, prior works that achieved EDE-like behavior (Nat. Commun. 2020, 11, 1510) relied on Triplet-STDP encoding, which redefines "spike-rate" through specially designed spike patterns (e.g., triplets with specific inter-spike intervals). Although these studies also use the term "rate coding" the underlying coding scheme is fundamentally different from spike-rate coding, as it does not correspond to continuous spike-rate stimulation and fails to satisfy the BCM requirement of stable weight at zero input (0 Hz).

To avoid ambiguity, we introduced the term "natural" to explicitly distinguish our approach from these redefined coding schemes. In the revised manuscript, we have clarified this distinction in the Introduction (page 4). We apologize for any confusion caused by our initial wording and thank the reviewer for helping us articulate the uniqueness of our work more precisely.

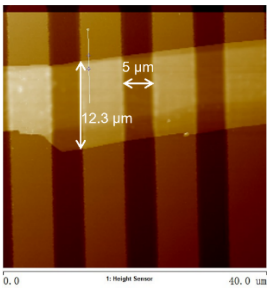
Location of Change: Introduction, page 4:

These methods inevitably increase circuit complexity and rely on external control parameters, diverging from the self-regulated nature of biological synapses. More importantly, such approaches do not rely spike-rate coding; instead, they employ non-rate-based methods such as triplet-STDP coding, gate-voltage modulation, or spike-voltage encoding, which deviate from the spike-rate coding principle common in neural systems. In principle, non-monotonic EDE behavior can be established through

the competition between two opposite monotonic processes.[27, 32]

(3) As for the quantitative justification of the large junction capacitance, the extracted capacitance is said to be "substantially larger" than a parallel-plate estimate. Please provide the actual parallel-plate value (with the assumed effective area and thickness) and the ratio between measured and estimated capacitance.

Response: We thank the reviewer for this valuable comment. Following the request, we have quantitatively compared the measured junction capacitance with the parallel-plate estimate.



As illustrated in the device structure, the CIPS flake has a width of ~10 μm, a thickness of ~40 nm, and a channel length of 5 μm. Using a dielectric constant of ε ≈ 300 for CIPS (Nano Energy 58 (2019) 596–603), the parallel-plate capacitance is calculated as:

$$C = 8.854 \times 10^{-12} \times 300 \times \frac{(10 \times 10^{-6})(40 \times 10^{-9})}{5 \times 10^{-6}} = 0.21\ fF$$

This value is approximately four orders of magnitude smaller than the capacitance extracted from pulse measurements (~12.1 pF), confirming that the observed capacitive effect cannot be attributed to a simple parallel-plate geometry and instead originates from the diffusion capacitance of the p–n homojunction formed by Cu^{+} migration.

We have included this calculation in the revised manuscript ("Junction capacitance and pulse-induced conductance depression effect" section, page 8) and provided detailed derivation steps in the Supplementary Information (Supplementary Note 2). We thank the reviewer for helping us improve the clarity and rigor of our work.

Location of Change: Introduction, page 4:

From the relation C = Q/U, the capacitance is estimated to be ~12.1 pF, substantially larger than the value (0.21 fF) predicted by a parallel-plate model of equivalent dimensions (Supplementary Note 2). This notable discrepancy indicates that the capacitance in CIPS stems from a mechanism distinct from conventional interfacial capacitance.

Location of Change: Supplementary Note 2, Supplementary Information page 4:

Using the above method, the capacitance of the CIPS device was extracted under various voltage conditions. A linear relationship was observed between the integrated charge and the applied voltage (*Q*-*U*), confirming the presence of a stable capacitive element in the CIPS device. From the relation $C = Q/U$, the estimated capacitance is approximately 12.1 pF. In contrast, the capacitance estimated using a parallel-plate model—assuming a device width of 20 μm, thickness of 40 nm, channel width of 5 μm, and a dielectric constant of approximately 300 for CIPS—yields a value of 0.21 fF.[4]

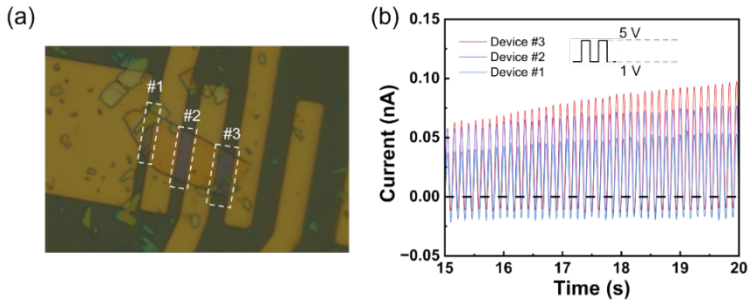
$$C = \varepsilon\varepsilon_0 \frac{S}{d}$$

his is considerably smaller than the 12.1 pF obtained from electrical measurements, with a discrepancy of about four orders of magnitude. (Detailed calculation steps are provided in the Supporting Information.) Such a pronounced difference suggests that the capacitance in CIPS originates from a mechanism distinct from conventional interfacial capacitance.

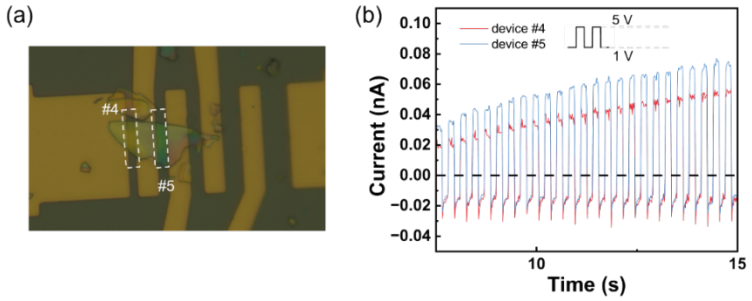
(4) Can authors provide device-to-device statistics for this capacitance to demonstrate reproducibility?

Response: We thank the reviewer for this valuable comment. To demonstrate the reproducibility of the observed capacitive behavior, we characterized seven representative devices with varying channel dimensions and flake thicknesses, and employed multiple measurement instrument to verify reproducibility.

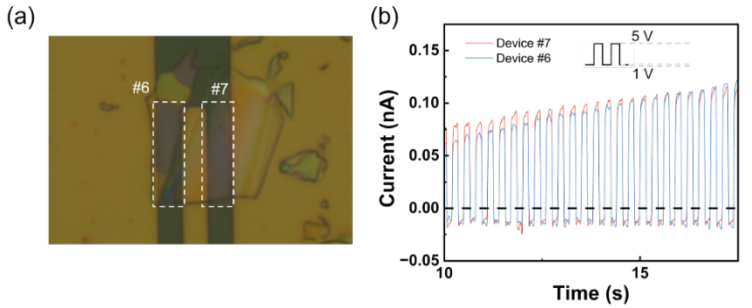
Devices #1–3: channel width = 3, 4, and 5 μm, respectively; thickness = 40 nm



Devices #4–5: channel width = 3 and 4 μm; thickness = 52 nm



Devices #6–7: channel width = 5 μm; thickness = 42 nm



All devices were subjected to pulse stimulation (high level: 5 V, low level: 1 V). As shown in the figures, every device exhibits clear charge–discharge transients during voltage switching, confirming the presence of a significant capacitance. Notably, no

clear correlation is observed between the discharge spike magnitude and channel dimensions, suggesting that the capacitance does not originate from interfacial effects but rather from the internal p–n junction, consistent with our proposed mechanism.

To rule out measurement artifacts, we tested the device using three independent instrument, each with its own probe station (During the measurement, the instrument's integration function was disabled to display the raw spikes):

(1) Semiconductor parameter analyzer (Keithley 4200)

(2) Sourcemeter (Keithley 2450)

(3) Current preamplifier + oscilloscope (Stanford Research Systems SR570, PicoScope 4000)

The capacitance was estimated by integrating the discharge current:

$$Q=\int Idt$$

$$C=UQ$$

The extracted capacitance values were 85.3 pF (Keithley 4200), 47.8 pF (Keithley 2450), and 57.9 pF (SR570). All values are of the same order of magnitude and consistent with the ~12.1 pF reported in the main text, confirming that the observed capacitance is intrinsic to the device and not an artifact of a particular measurement setup. Similar discharge spikes and reconfigurable p–n junction behavior in lateral CIPS devices have also been reported in recent studies (Device 3, 100712, 2025; ACS Nano 2023, 17, 1239–1246), further corroborating our findings.

[Figure Redacted]

(5) The authors attribute the large capacitance to minority-carrier accumulation (diffusion capacitance) in the p–n homojunction. Have the authors performed frequency-dependent C(f) C(f) measurements to distinguish diffusion capacitance from interfacial capacitance? and any systematic C–V or C–F data in both the LRS and HRS states?

Response: We thank the reviewer for this insightful comment regarding the origin of the large capacitance and the lack of frequency-dependent C-f characterization. In our CIPS memristor, standard impedance spectroscopy faces practical difficulties due to the non-ideal equivalent circuit behavior. The devices exhibit strong nonlinear resistance and significant parasitic series resistance, which severely distort the sinusoidal response under AC small-signal conditions. Our attempts to perform *C-f* measurements resulted in heavily distorted waveforms, making reliable capacitance extraction via conventional impedance analyzers infeasible. Therefore, we adopted a pulse integration method that directly captures the charge–discharge dynamics under operational pulsed conditions.

Although direct *C-f* data are not available, the attribution of the measured capacitance to minority-carrier accumulation (diffusion capacitance) in the p–n homojunction is supported by multiple converging lines of evidence:

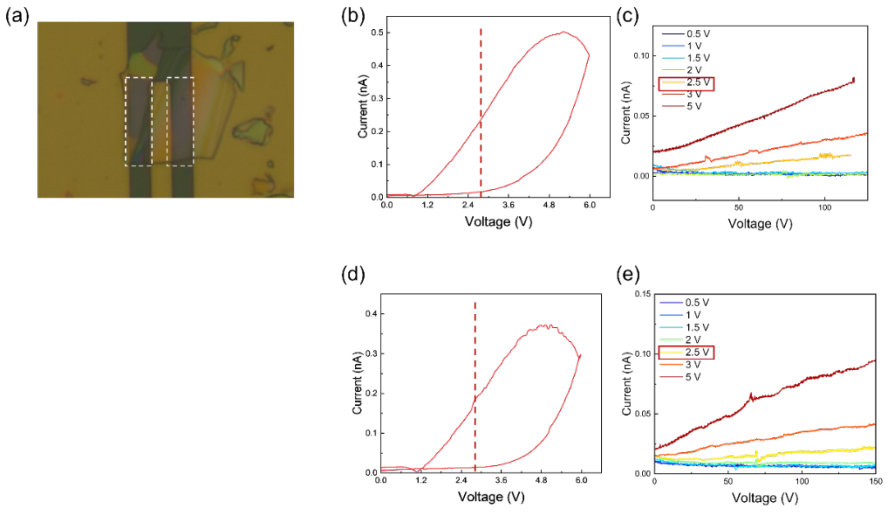
1. CIPS has been widely reported to form a reconfigurable p–n homojunction in lateral device structures (ACS Nano 2023, 17, 1239–1246; Device 3, 100712, 2025). It is a well-established principle in semiconductor physics that a p–n junction inherently possesses junction capacitance, and under forward bias, this capacitance is dominated by diffusion capacitance arising from minority-carrier storage.
2. The measured capacitance shows no correlation with channel dimensions (see response to Comment #4), ruling out dominant interfacial or geometric origins.
3. The measured capacitance (~12.1 pF) is four orders of magnitude larger than the parallel-plate estimate (~0.2 fF), far exceeding what could be explained by interfacial effects alone.

(6) The manuscript states that approximately 2 V is the threshold for Cu^+ migration. a) Is this threshold consistent across different flake thicknesses and device batches? What is the error range? Could the authors provide a simple Arrhenius-type fitting or comparison to show that this threshold corresponds to an energy barrier consistent with the reported ionic migration barrier of CIPS in the literature?

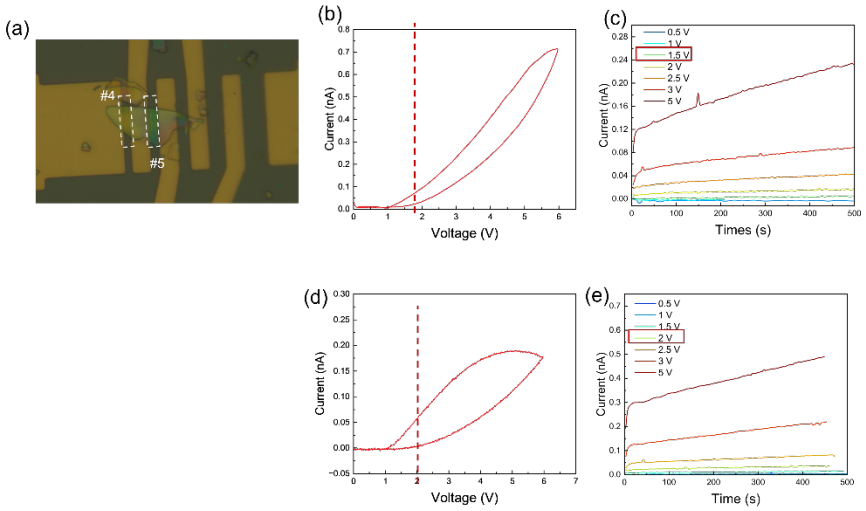
Response: We thank the reviewer for this valuable comment. To address the variability and statistical distribution of the threshold voltage for Cu^+ migration, we have characterized multiple devices with different channel dimensions and flake thicknesses, as summarized below.

The following picture show the *I*–*V* characteristics of five representative devices:

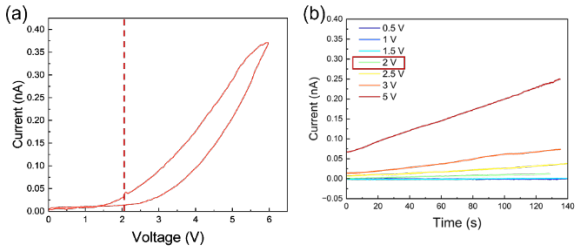
Devices 1 and 2: Fabricated on the same CIPS flake with identical channel widths (5 μm). They exhibit nearly overlapping *I*–*V* curves and the same threshold voltage (~2.5 V), demonstrating good uniformity within the same batch.



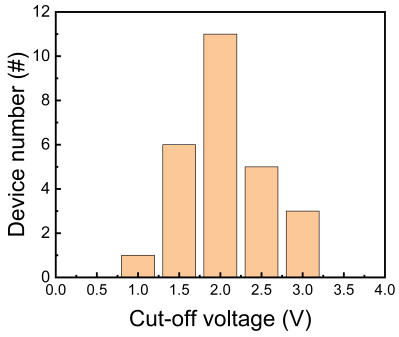
Device 3 and 4: A narrower channel (3 and 4 μm) on the same flake shows a higher current under the same bias and a lower threshold voltage (~1.5 V/2 V), indicating that the threshold is sensitive to channel width.



Device 5: With channel widths 5 μm (from a different flake), exhibit thresholds of ~2.0 V, indicating that there are differences among the various batches of devices.



Due to the poorer endurance of devices with narrower channels, which are more prone to breakdown under repeated cycling, our statistical analysis focused primarily on devices with a 5 μm channel width. These results indicate that the threshold voltage varies across devices, typically ranging from 1.5 V to 2.5 V, as summarized in the statistical distribution of 26 devices (5 μm channel width).



Influence of flake thickness

Based on our experimental observations across a thickness range of 20–80 nm, no clear

correlation between flake thickness and threshold voltage could be established. We speculate that this may be due to current crowding near the electrode interface, such that the bulk of the CIPS flake beyond a certain thickness does not contribute effectively to ion migration. This hypothesis is supported by KPFM measurements: when the electrode is placed beneath the CIPS flake, no polarization-induced potential distribution is detectable; in contrast, when the electrode is placed on top of the flake, a clear potential distribution is observed on the same side (as shown in Figs. 4d and 4e of the main text). This suggests that ion migration and the resulting field effect are confined to the region near the top electrode.

Batch-to-batch variability

We attribute the observed variability across different fabrication batches primarily to the contact quality at the CIPS/electrode interface. The mechanical exfoliation and wet-transfer processes involve polymeric films, which inevitably leave residues that can affect the interface quality. In devices prepared outside the cleanroom environment, we often observe significantly higher threshold voltages or even non-conducting behavior, further supporting this interpretation.

Regarding Arrhenius-type fitting

We agree that temperature-dependent Arrhenius analysis would provide more direct evidence linking the threshold voltage to the ionic migration barrier. However, we respectfully note that the threshold voltage observed in our CIPS memristors is not solely determined by the intrinsic migration barrier, but is also significantly influenced by interface contact quality and device history. In our experiments, the threshold voltage exhibits small fluctuations depending on prior stimulation, which limits the precision required for reliable Arrhenius fitting. Furthermore, the focus of this work is not on the detailed conduction mechanisms of CIPS—which have been extensively studied in previous reports (e.g., Adv. Mater. 2023, 35, 2302419, providing phase diagrams of ion migration under varying electric fields and temperatures). Based on literature reports, the migration barrier for Cu^{+} in CIPS is typically in the range of 0.3–

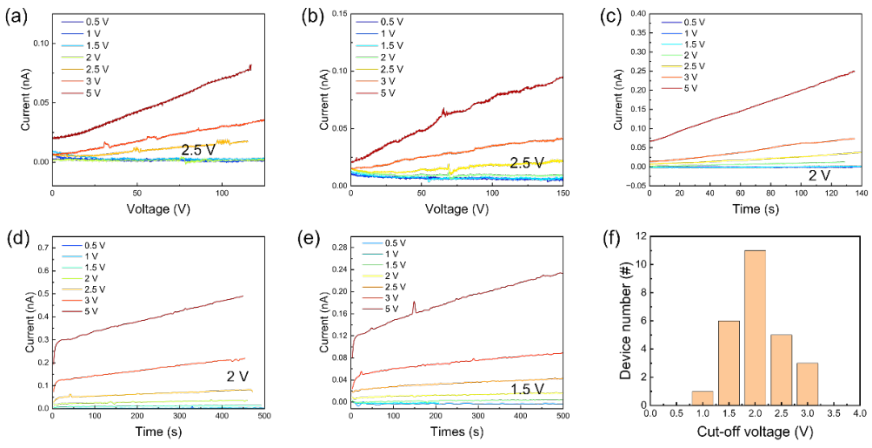
0.6 eV (Nano Energy 2019, 58, 596–603; ACS Nano 2023, 17, 1239–1246). The observed threshold voltage of ~2 V, when considered alongside these reported values, is broadly consistent with an ion-migration-based switching mechanism. We acknowledge that a quantitative comparison would require systematic temperature-dependent studies, which we plan to pursue in future work.

In the revised manuscript, we have incorporated these discussions in the "Electrical properties and synaptic behavior of the CIPS memristor" section, and added the statistical distribution of threshold voltages in Supplementary Fig. 7. We thank the reviewer for prompting us to analyze device variability more thoroughly, which has significantly strengthened the manuscript.

Location of Change: Result, page 6:

Conductance potentiation occurs only above ~2 V, indicating a threshold voltage associated with Cu^+ migration. Supplementary Fig. 7 presents the threshold voltage statistics for a subset of devices, showing that the threshold varies across devices (ranging from approximately 1.5 to 2.5 V) depending on factors such as interface contact quality. This threshold likely corresponds to the activation barrier for ion motion, which is further supported by voltage-sweep measurements (Supplementary Fig. 8).[44, 45]

Location of Change: Supplementary Figure 7, Supplementary Information page 8:



Supplementary Figure 7. Resistive switching behavior of five representative devices under constant bias and statistical distribution of threshold voltages across 26 devices.

(a, b) Devices 1 and 2: channel width = 5 μm, thickness = 42 nm.

(c) Device 3: channel width = 5 μm, thickness = 54 nm.

(d) Device 4: channel width = 4 μm, thickness = 52 nm.

(e) Device 5: channel width = 3 μm, thickness = 52 nm.

(f) Statistical distribution of threshold voltages for 26 devices (channel width = 5 μm).

(7) As for the formula (3), the value GL and GH representing the initial and saturated conductance of the device, are from single device or obtained by fitting which specific experimental curves? Are they extracted from a single device or averaged over multiple devices? How does device-to-device variability affect the BCM curves? Do the authors have error bars or statistical information to show this?

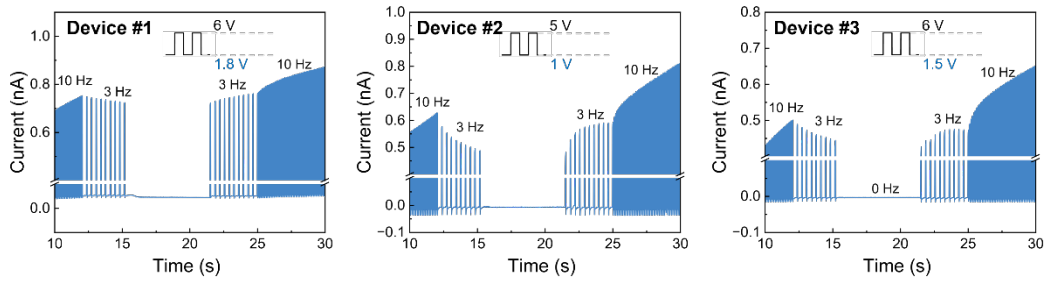
Response: We thank the reviewer for this valuable comment.

Equation (3) represents a simple linear mapping that correlates the ion migration state variable W_i with the device conductance G, a widely adopted approach in memristor modeling (Nature 2008, 453, 80–83). Here, G_L and G_H denote the initial (low-conductance) and saturated (high-conductance) states of the device, respectively, which can be directly obtained from experimental measurements. The values listed in Supplementary Table 1 were empirically selected based on statistical results from multiple devices and rounded to integers for computational convenience. It should be noted that the conclusions (particularly the realization of threshold sliding and non-monotonic EDE) of this work are determined by the relative conductance change and the competition between potentiation and depression processes, and are therefore insensitive to the exact numerical values of G_L and G_H. We have added a clarifying statement in the revised manuscript.

We fully agree that device-to-device variability is an important consideration. As is widely acknowledged in the field, the stochastic nature of mechanical exfoliation for two-dimensional materials makes perfect device uniformity challenging—a limitation the community is actively working to address. In our experiments, device-to-device variations primarily affect the operating voltage window and the frequency threshold for BCM behavior, but do not alter the overall trend or the emergence of EDE under natural spike-rate coding. As discussed in our response to Comment #6, the threshold voltage for Cu^+ migration varies across devices (typically 1.5–2.5 V), which directly influences the pulse amplitude required to induce conductance changes. Consequently, the programming voltages must be carefully calibrated for each device.

We have elaborated on this calibration process in the "Electrical properties and synaptic behavior of the CIPS memristor" section of the main text.

The figure below demonstrates the BCM rule in several representative devices. Devices with different threshold voltages require different programming pulse voltages: the low level should be set slightly below the threshold to maintain non-volatility, while the high level must be calibrated to balance the potentiation and depression processes. Although the specific pulse parameters vary from device to device, the core BCM features—threshold sliding and non-monotonic EDE—are reproducible across different devices.



It is worth noting that the CIPS memristor exhibits spontaneous conductance relaxation. To mitigate this during operation, we apply a sub-threshold DC bias (the low level of the pulse train, set to 1-2 V in this work) to suppress relaxation. Under these conditions, the reverse voltage spike generated by the junction capacitance during pulse intervals perturbs this equilibrium, enabling depression. The choice of bias voltage is therefore critical:

- An excessively high low-level bias diminishes the depression effect induced by the capacitance, compromising the low-frequency depression regime.
- An excessively low bias fails to suppress relaxation, leading to conductance decay even in the absence of input (0 Hz).

Similarly, the high-level pulse amplitude must be carefully selected to balance potentiation and depression. Due to non-ideal factors in the physical system, each device requires individual experimental calibration to determine its optimal operating voltages.

In the result and SI section, supplement relevant explanations of equation (3) in the manuscript.

Location of Change: Result page 10:

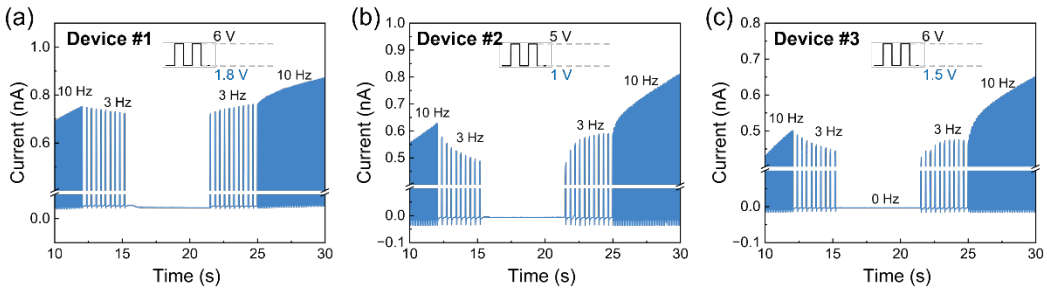
Finally, the device conductance G is functionally related to W_i by a linear mapping[51-53]:

$$G = G_L + W_i(G_H - G_L). \quad (3)$$

Location of Change: Supplementary Table 1, Supplementary Information page 20:

The values of Parameters in equation Table 1 represent the ion dynamics of CIPS memristor. The values represent typical behavior observed across multiple devices and were used consistently in all simulations to ensure comparability of results. These values were empirically selected based on measurements from multiple devices and simplified to integers for computational convenience. It should be noted that the specific numerical values do not affect the qualitative conclusions of this work, as the BCM learning dynamics are primarily governed by the relative conductance change and the competition between potentiation and depression processes, rather than the absolute conductance values.

Location of Change: Supplementary Figure. 14, Supplementary Information page 20:



Supplementary Figure 12. BCM rule of five representative devices under continuous pulse trains at 10, 3, 0, 3 and 10 Hz (50 ms).

a. Device 1 (threshold ~2.5 V): low level = 1.8 V, high level = 6 V

b. Device 2 (threshold ~2 V): low level = 1 V, high level = 5 V

c. Device 3 (threshold ~2 V): low level = 1.5 V, high level = 6 V

(8) The authors use a MoS_2 memristor plus an external RC network to reproduce the experiments and verify the generality of the strategy. a) Besides MoS_2, have you also verified this approach on other types of memristors (for example, oxide-based devices or PCM)? b) How are the parameters of the external RC chosen to match the intrinsic time scales of the device? If they are not well matched, how would the EDE regime change?

Response: We thank the reviewer for these valuable questions.

a) In addition to MoS_2, we have also validated this strategy in TiO_x- and WO_x-based memristors, with promising results. In future work, we aim to further refine this approach and explore its scalability toward array-level implementation of the BCM rule.

b) The reviewer raises an astute point: matching the RC time constant to the intrinsic dynamics of the memristor is indeed the most critical challenge in this proof-of-concept demonstration. Specifically, three conditions must be satisfied:

1. **Time-scale matching**: The inflection point of the integrated negative discharge spike as a function of frequency is governed by the RC time constant ($\tau=RC$). To observe the transition from increasing to saturated/decreasing depression—i.e., the EDE regime—the inter-spike interval in the pulse train must be on the same order of magnitude as τ. If the time constants are poorly matched, the necessary non-monotonic EDE behavior cannot be resolved.
2. **Voltage division**: To ensure that a significant portion of the input voltage drops across the memristor during the discharge transient, the series resistance RR should be comparable to the memristor's own resistance R_mRm. If RR is too small or too large, the capacitive discharge spike becomes too weak to effectively modulate the device.
3. **Switching speed compatibility**: The range of pulse frequencies used in the experiment must be compatible with the intrinsic resistance switching speed of the memristor. If the pulses are too fast (high frequency), the device may not have sufficient time to respond; if too slow (low frequency), relaxation effects may dominate.

When applying this strategy to oxide-based memristors (e.g., TiO_x, WO_x), we encountered an additional practical constraint: their relatively low equivalent resistance (on the order of $10^5\ \Omega$) necessitates the use of large capacitances (in the μF range) to satisfy the conditions above. This requirement poses challenges for integration and scalability—an issue we are actively addressing in ongoing work.

Theoretical framework.

To provide a rigorous understanding of these matching requirements, we developed a simplified circuit model for the CIPS device (Supplementary Fig. 20). In this equivalent circuit, the memristor is connected in series with a non-ideal capacitor (with parallel leakage resistance R_l). The voltage across the memristor, V_m, is governed by:

$$\frac{dV_m}{dt} = \frac{V_{in}(t)}{R_l C} - \frac{R_l + R_m}{R_l R_m C} V_m$$

Under steady-state DC conditions, the capacitor acts as an open circuit, and the voltage division is simply:

$$V_m = \frac{R_m}{R_l + R_m} V_{in}(t)$$

During transients, the capacitor charges or discharges, temporarily altering V_m. Upon a low-to-high transition, rapid charging produces a positive voltage spike driving potentiation; upon a high-to-low transition, discharging generates a negative voltage spike driving depression. The capacitor voltage dynamics follow:

$$\frac{dV_c}{dt} = \frac{V_{in} - V_c}{R_m C} - \frac{V_c}{R_l C}$$

Under natural spike-rate coding (fixed pulse width and amplitude), each spike produces identical positive and negative transients. The integrated area of the positive spikes increases linearly with frequency, leading to monotonic potentiation. At low frequencies, the capacitor fully discharges between pulses, so the integrated negative spike area also increases linearly. However, as frequency increases (inter-spike interval decreases), the capacitor cannot fully discharge, causing the integrated negative spike area to saturate and eventually decrease. The competition between this saturating depression and linear potentiation gives rise to the non-monotonic EDE behavior characteristic of the BCM rule.

(9) Junction-capacitance-driven EDE may be affected by process variations and parasitic parameters in practical chip fabrication: a) Have you evaluated the impact of process variations in Cj and Rleak on the stability of the BCM curves? b) If the junction capacitance of each cell in an array differs by a factor of 2–3 or more, can stable performance still be achieved through array-level training?

Response: We thank the reviewer for these insightful and professionally relevant questions, which are indeed critical for assessing the practical feasibility of our approach.

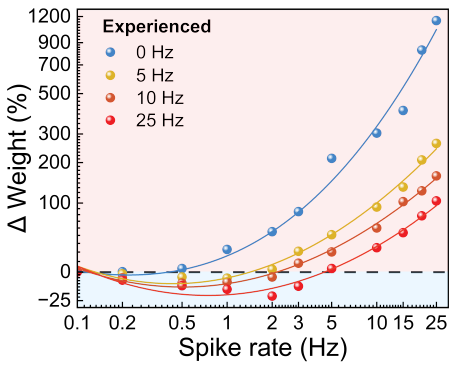
a) We have evaluated the influence of RC parameter variations through the theoretical framework presented in our response to Comment #8. Variations in capacitance and leakage resistance can significantly affect the operating frequency range of the BCM rule, with the characteristic frequency scaling approximately as $\theta \approx 1/RC$. This variability inevitably increases the complexity of coding, as a single fixed pulse frequency cannot optimally address all devices in a large-scale array. However, as demonstrated in our model, the qualitative features of the BCM rule—threshold sliding and non-monotonic EDE—remain preserved across a reasonable range of parameter variations, even though the absolute frequency threshold may shift.

b) The primary goal of this work is to demonstrate a proof-of-concept prototype for realizing the BCM rule in a single CIPS memristor and to elucidate the underlying mechanism. We fully acknowledge that, due to the inherent limitations of van der Waals materials, CIPS itself is not currently suitable for large-scale array integration. However, as emphasized in the manuscript, our work provides a generalizable strategy—the equivalent circuit model—that can be implemented in more mature and uniform memristor platforms (e.g., oxide-based devices with integrated capacitors fabricated using conventional CMOS processes). In such platforms, the parameters C_j and R_{leak} can be precisely controlled through established fabrication techniques, thereby mitigating the variability concerns. We believe that by decoupling the mechanism from the specific material system, our approach offers a viable path toward scalable BCM-based neuromorphic systems.

Reviewer #2

In this manuscript, Huang et al., used CuInP2S6-based two-terminal memristor to emulate spike-rate dependent synaptic plasticity, especially the BCM rule. The authors demonstrated that the synaptic plasticity of the memristor was affected by the history of previously applied pulses. The authors assumed this effect was due to negative capacitive feedback current formed by the p-n homojunction in the CIPS layer. The authors also demonstrated physical reservoir computing based on the CIPS memristor model developed in this work. Although this work shows the possibility of emulating BCM rule, one of the most accurate models explaining biological synapse, there is a significant gap between the authors' claim and their experimental results. Furthermore, the experimental data in the figures cannot support that this CIPS-based memristor follows the BCM rule and shows enhanced depression effect. The reviewer suggests the following comments.

We thank the reviewer for these professional and insightful comments. We appreciate the opportunity to clarify the key points raised. First, we respectfully note that both hallmark features of the BCM rule—threshold sliding and the enhanced depression effect (EDE)—have been experimentally observed in our work, as demonstrated in Fig. 3f and further supported by additional data in the revised manuscript (Supplementary Figs. 11 and 12). These results confirm that the CIPS memristor indeed exhibits BCM-like plasticity under spike-rate coding.



Newly updated Figure 3f in main text

The primary novelty of our work lies in being the first demonstration of true EDE behavior under natural spike-rate coding in a single two-terminal memristor. Prior to this work, nearly all related studies achieved non-monotonic EDE-like behavior using Triplet-STDP coding, an approach introduced by Wang et al. in 2020 (Nat. Commun. 11, 1510). While innovative, this coding strategy relies on precisely timed spike triplets and effectively redefines "spike-rate" in a way that deviates from natural rate coding. Moreover, it operates in a regime approaching destructive readout and does not satisfy the BCM requirement of stable synaptic weight in the absence of input (0 Hz)—a feature essential for both biological plausibility and practical neuromorphic systems.

By contrast, our approach leverages the intrinsic junction capacitance of the CIPS memristor to generate EDE under continuous spike-rate stimulation, without any external encoding circuitry. The generality of this mechanism has been validated through both mathematical modeling and equivalent circuit experiments using other memristor types, as detailed in the manuscript.

We address each of the reviewer's specific concerns point by point below. We thank the reviewer again for helping us strengthen the clarity and rigor of our work.

1.In Figure 2g, the authors mentioned retention characteristics of the CIPS memristor when a read voltage lower than the threshold is applied during the retention period. However, in Supplementary Figure 8c, there is no change in electrical current after 100 s of interval, which contradics with Figure 2g. The reviewer asks the author for further clarification.

Response: We thank the reviewer for this comment. The observed behavior is not contradictory, but rather reflects the voltage-dependent retention characteristics of the CIPS memristor.

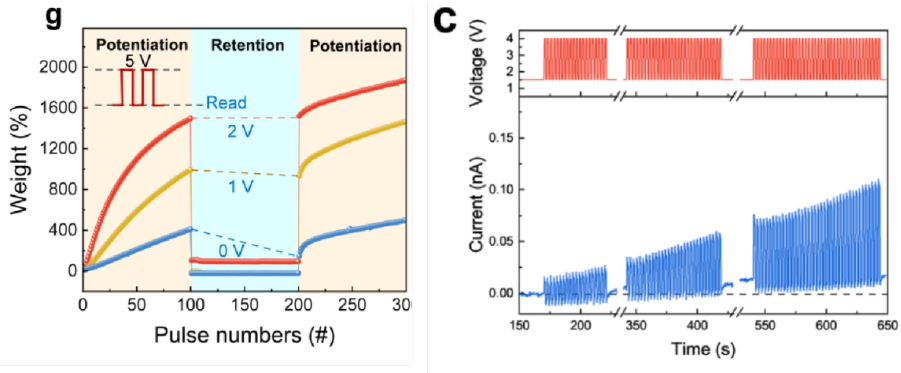


Figure 2g and Supplementary Figure 8c (revised as 9c)

As demonstrated in Figure 2g, the retention stability of the device improves significantly when a higher read voltage is applied during the retention period. Specifically, applying a read voltage closer to the threshold voltage helps stabilize the conductance state by counteracting spontaneous relaxation.

In Supplementary Figure 8c (revised as 9c), a read voltage of 1.5 V was used during the retention test (as indicated by the red curve in the figure, which represents the applied pulse voltage). This voltage is above the threshold for effective retention enhancement, consistent with the saturating trend shown in Figure 2g. Consequently, the device maintains its conductance state without observable decay over the 100 s interval, which aligns with the enhanced retention expected at this read voltage.

We have clarified this point in the revised manuscript and updated the figure caption of Supplementary Figure 9c to explicitly state the read voltage condition. We thank the reviewer for helping us improve the clarity of our presentation.

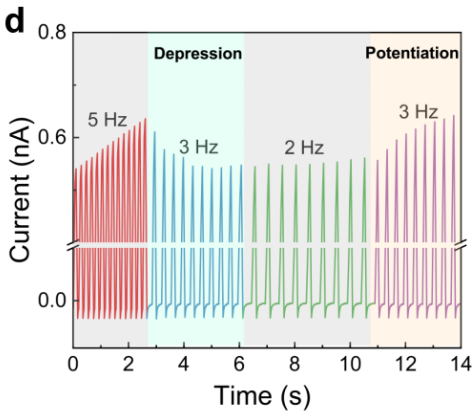
Location of Change: Supplementary Figure. 9, Supplementary Information page 10:

c. Continuous programming characteristics of the device under repeated pulsed stimulation (1.5 – 4 V, 0.5 Hz). Three pulse trains, each containing 20, 30, and 40 pulses, are applied sequentially with 100 s intervals, resulting in cumulative conductance enhancement across successive sets.

2. In Figure 3d, the authors showed that the direction of conductance change is affected by the previous spike rate by comparing the current change when applying a 3 Hz pulse after applying two different spike trains. The reviewer wonders, based on the EDE explanation, when a 2 Hz spike train is applied (green colored), the device should show depression since lower spike rates of pulses were applied compared to the previous spikes (3 Hz). However, in Fig. 3d, devices shows potentiation while applying a slower spike train of 2 Hz. The reviewer thinks this figure is critical for verifying the CIPS device's emulation of the BCM rule, but the reviewer cannot be fully persuaded. The reviewer asks the author for an explanation for this.

Response: We thank the reviewer for this insightful comment, which is very helpful. We have carefully considered the question and provide the following explanation. Corresponding revisions have been made in the manuscript to reflect this clarification.

Regarding the behavior observed in the old Figure 3d: In the original figure, the absence of conductance depression during the 2 Hz stimulation (green curve) is attributed to a boundary condition—the device had already approached its minimum conductance state. Specifically, the device was initially preset to a high conductance state by 5 Hz pulses. Subsequent 3 Hz stimulation disrupted the previous equilibrium, inducing depression. By the time the 2 Hz pulses were applied, the conductance had already reached its lower bound, limiting further depression. However, the internal ion distribution had been reconfigured during prior stimulation, causing the threshold to slide toward lower frequencies. This sliding effect is evident in the latter part of the 2 Hz pulse train, where the conductance begins to trend upward again. Finally, the reapplied 3 Hz pulses break the new equilibrium, leading to potentiation.



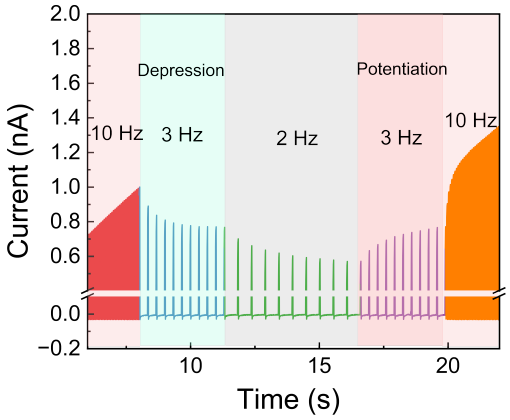
The old Figure 3d

We acknowledge that this presentation may have caused confusion. Our initial intention was to follow the conventional format used in prior BCM demonstration studies.

[Figure Redacted]

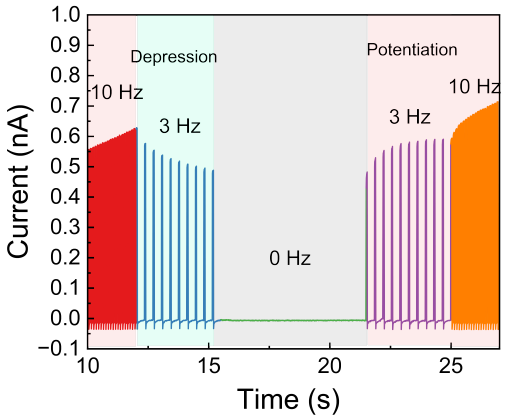
Adv. Funct. Mater. 2015, 25, 4290; Adv. Electron. Mater. 2024, 2400612; Sci. Adv. 2022, 8, eade0072; Nat. Commun. 2022, 13, 5585; Nat. Commun. 2020, 11, 1510

Upon further reflection, we agree with the reviewer that a clearer demonstration is necessary to fully validate the EDE behavior. The boundary issue can be avoided by operating the device in a higher conductance range. In the revised manuscript, we have therefore replaced Figure 3d with new data obtained using a higher-frequency preconditioning pulse train to preset the device to a higher conductance state. In the updated figure, the device now exhibits the expected conductance depression under 2 Hz stimulation, consistent with the BCM rule.



Newly updated Figure 3d in the revised main text replacing the old Figure 3d

To further strengthen the verification of EDE, we have added Supplementary Figure 11, which directly compares the response to 2 Hz stimulation (from the updated Fig. 3d) with the response to 0 Hz stimulation (i.e., constant subthreshold bias). Under 0 Hz, no conductance change is observed, confirming that the depression at 2 Hz is frequency-dependent and not merely an artifact of relaxation. This comparison conclusively demonstrates the EDE phenomenon central to the BCM rule.

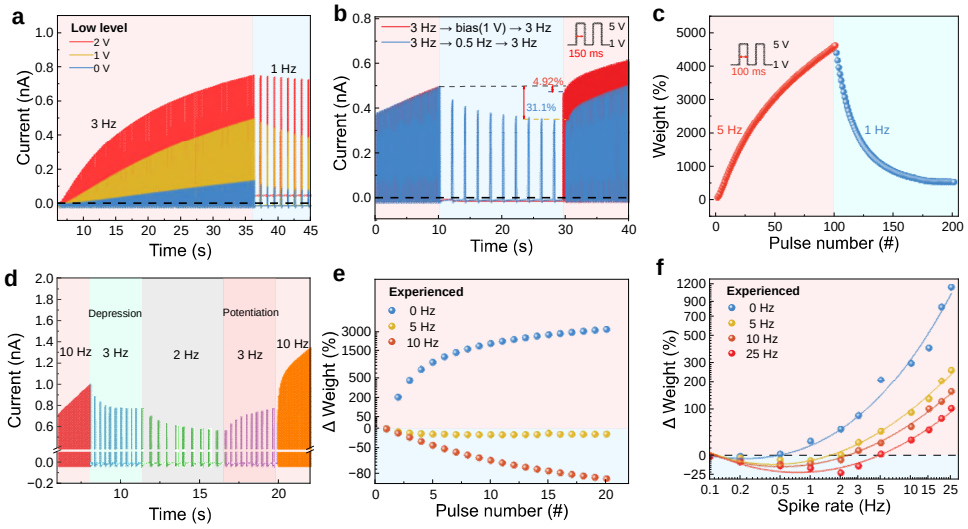


We have revised the description of Figure 3d accordingly in the manuscript. We thank the reviewer for helping us identify this ambiguity and for guiding us toward a more rigorous and convincing demonstration.

Location of Change: Result page 7:

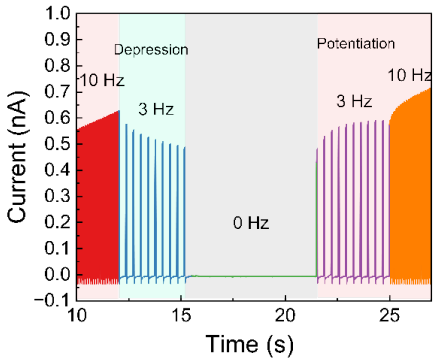
The CIPS memristor successfully emulates history-dependent plasticity, a key adaptive

feature of the BCM rule.[25, 31] To demonstrate this, we applied four pulse trains at different frequencies (1–10 Hz, 50 ms) to stimulate the CIPS memristor. The resulting conductance changes (Fig. 3d) reveals distinct frequency-specific responses: potentiation at 10 Hz, depression at 3 Hz, further depression at 2 Hz, and restored potentiation upon re-applying 3 Hz and 10 Hz. The fact that identical 3 Hz stimuli induce diametrically opposite outcomes depending solely on prior stimulation history provides direct evidence for history-dependent plasticity. Furthermore, when the 2 Hz pulses were replaced with a constant 1 V bias, the device conductance remained stable, demonstrating the EDE behavior of the CIPS memristor (Supplementary Figs. 11, and the reproducibility across multiple devices in Supplementary Fig. 12)). This feature is further supported in Fig. 3e, which shows that the rate of conductance change systematically decreases with increasing intensity of historical stimulation.



The revised fig3 in manuscript.

Location of Change: Supplementary Figure 11, Supplementary Informations page 7:



Supplementary Figure 11. Asymmetric response of the CIPS memristor under positive and negative pulse stimulation.

Device response to continuous pulse trains at 10, 3, 0, 3 and 10 Hz (1–5 V, 50 ms). The response to 3 Hz stimuli shifts between potentiation and depression depending on prior activation history. When the 2 Hz pulses were replaced with a constant 1 V bias (0 Hz), the device conductance remained stable.

3. In Figure 3f, the authors showed a sliding threshold, similar to the BCM rule, demonstrating that the threshold frequency, determining potentiation or depression behavior of the CIPS memristor is affected by the presynaptic spike frequency. Based on the BCM rule, the threshold should increase proportionally to the historical spike rate. However, in Figure 3f, the threshold spike rate of the memristor with historical spike rates of 5 Hz and 10 Hz looks identical. The reviewer suggests that the authors provide more quantitative and systematic analysis for the emulation of the BCM rule in the CIPS memristor. Furthermore, based on the figure caption, experienced stimulation at 25 Hz should also be presented in Figure 3f, but it's missing.

Response: We thank the reviewer for this thoughtful suggestion.

In the original BCM theory, the sliding threshold θ_M is defined as the time-averaged square of the postsynaptic activity:

$$\theta_M = E[y^2]$$

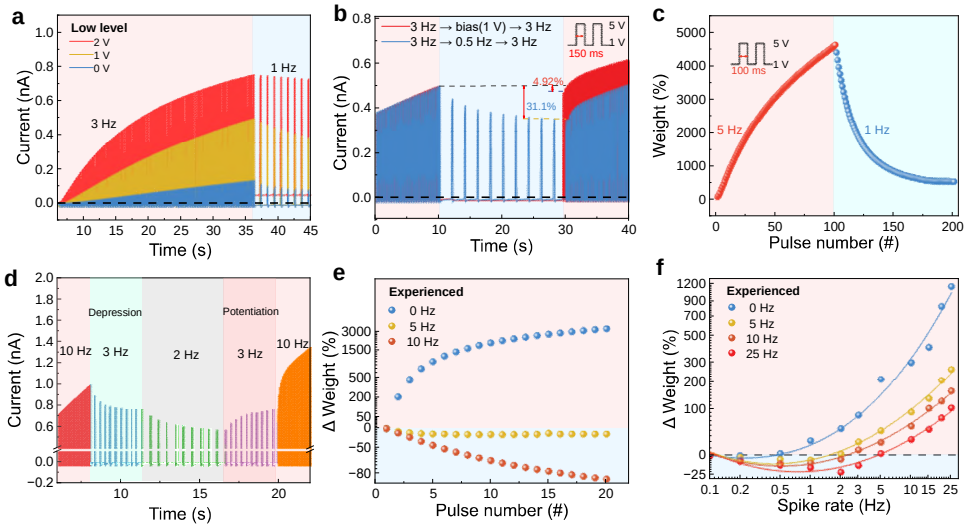
where y represents the postsynaptic firing rate. This formulation indicates that the threshold is determined by the statistics of historical postsynaptic activity, rather than being strictly proportional to the presynaptic spike rate. Therefore, while increased presynaptic activity generally shifts the threshold toward higher spike-rate, the relationship is indirect and mediated by the integrated postsynaptic response.

In our CIPS memristor, the spike-rate dependent transition between potentiation and depression qualitatively reproduces this sliding threshold behavior. Due to the nonlinear dynamics inherent to both the memristor and the parasitic capacitance, the threshold does not increase in strict proportion to the historical pulse rate.

Regarding the missing 25 Hz data in Figure 3f:

We sincerely apologize for this oversight. During manuscript preparation, the 25 Hz dataset was inadvertently moved to Figure 1d, leading to its omission from Figure 3f. In the revised manuscript, we have corrected this error and now include the 25 Hz data in Figure 3f, which provides a more complete characterization of the BCM-like

behavior in our device. We thank the reviewer for prompting us to provide a more rigorous and complete characterization of the BCM-like behavior in our device.



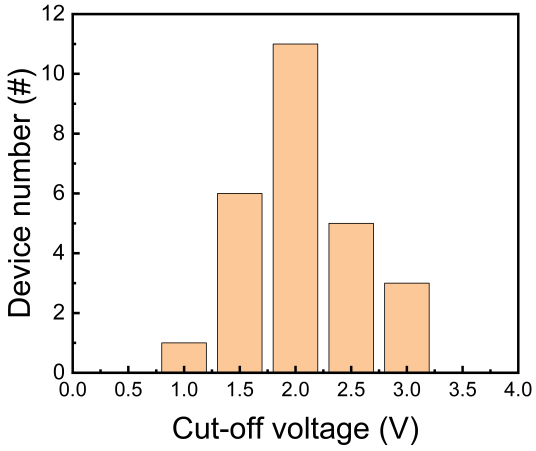
The revised fig3 in manuscript.

d. Device response to continuous pulse trains at 10, 3, 2, 3 and 10 Hz (1–5 V, 50 ms). The response to 3 Hz stimuli shifts between potentiation and depression depending on prior activation history.

4. The reviewer requests to authors provide more statistical results, especially the EDE verification shown in Figure 3. In the current figure, it looks like the results were obtained from a single device, so showing reproducibility would further enhance the manuscript.

Response: We thank the reviewer for this important suggestion. To demonstrate the reproducibility of the EDE behavior shown in Figure 3, we have performed pulse measurements on multiple representative devices and included these results in the revised manuscript.

The EDE effect in our work arises from the competition between two processes: (i) potentiation induced by the applied pulses, and (ii) depression generated by the reverse voltage spikes from the junction capacitance during pulse intervals. Due to the stochastic nature of two-dimensional material exfoliation, batch-to-batch variations lead to differences in the threshold voltage required to trigger conductance potentiation. Consequently, the high and low levels of the programming pulses must be carefully calibrated for each device to balance the potentiation and depression effects. We have provided statistical results of threshold voltages for multiple devices (with an estimated precision of ±0.5 V, as the threshold itself can fluctuate slightly depending on stimulation history).



The following figure (to be included as Supplementary Figure 12) presents the EDE verification for three representative devices with threshold voltages of approximately 1.5 V, 2 V, and 3 V. The pulse parameters used were:

- Device 1 (threshold ~2.5 V): low level = 1.8 V, high level = 6 V
- Device 2 (threshold ~1.5 V): low level = 1 V, high level = 5 V
- Device 3 (threshold ~2 V): low level = 1.5 V, high level = 6 V

All devices were stimulated with 50 ms pulses. The results consistently show:

Potentiation under 10 Hz stimulation,

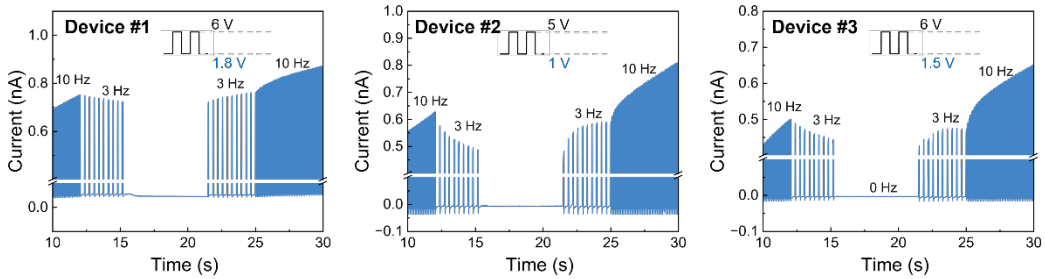
Depression after switching to 3 Hz,

Stable conductance under 0 Hz (constant low-level bias),

Repeated potentiation when 3 Hz and 10 Hz are reapplied.

The stable conductance under 0 Hz, depression at 3 Hz, and potentiation at 10 Hz collectively demonstrate the non-monotonic EDE behavior central to the BCM rule, and confirm that the effect is reproducible across devices despite variations in absolute threshold voltages.

The newly added data about the reproducibility in Supplementary Figure 12:



We fully acknowledge that device-to-device uniformity remains a key challenge for two-dimensional materials, and that the need for individual voltage calibration currently limits practical deployment. To address this, we have developed an equivalent circuit model of the CIPS memristor (presented in the main text) and validated it through simulation, which reproduces the experimental EDE behavior with good fidelity. This model provides a pathway toward implementing the BCM rule in more stable and uniform memristor platforms (e.g., oxide-based devices with integrated capacitors). In future work, we will explore the scalability of this approach to array-level integration.

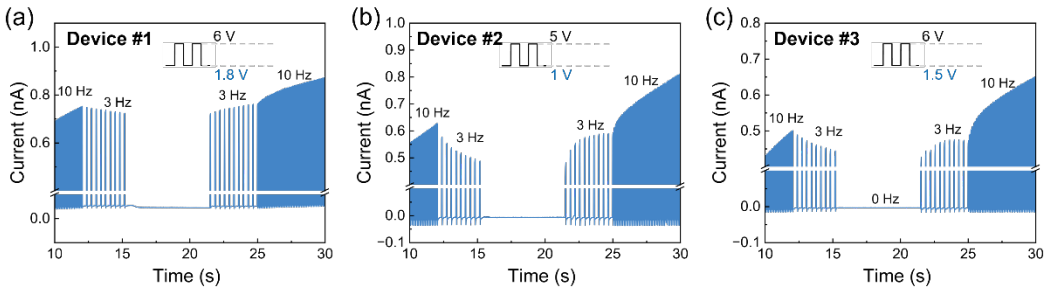
We have added the data about the reproducibility described above to the Supporting

Information (Supplementary Fig. 12) and included a corresponding discussion in the main text (Results section, page 7). We thank the reviewer for helping us strengthen the manuscript.

Location of Change: Result page 7:

Furthermore, when the 2 Hz pulses were replaced with a constant 1 V bias, the device conductance remained stable, demonstrating the EDE behavior of the CIPS memristor (Supplementary Figs. 11, and the reproducibility across multiple devices in Supplementary Fig. 12)).

Location of Change: Supplementary Figure 12, Supplementary Information page 12:



Supplementary Figure 12. BCM rule of five representative devices under continuous pulse trains at 10, 3, 0, 3 and 10 Hz (50 ms).

a. Device 1 (threshold ~2.5 V): low level = 1.8 V, high level = 6 V

b. Device 2 (threshold ~1.5 V): low level = 1 V, high level = 5 V

c. Device 3 (threshold ~2 V): low level = 1.5 V, high level = 6 V

5. Based on the KPFM measurement, the surface potential of the CIPS memristor in LRS shows linearly incrase as a function of lateral distance, indicating ion distribution due to the external electrical field. The review thinks this KPFM image contradicts the authors' explanation shown in Fig. 4f, which requires a distinct depletion region in the middle. Could this capacitive current originate from the interfacial electrical double layer (EDL) formed between the CIPS layer and the left or right contact electrode?

Response: We thank the reviewer for raising this important point. The KPFM measurement and the junction model shown in Fig. 4f are not contradictory, and we provide the following clarification.

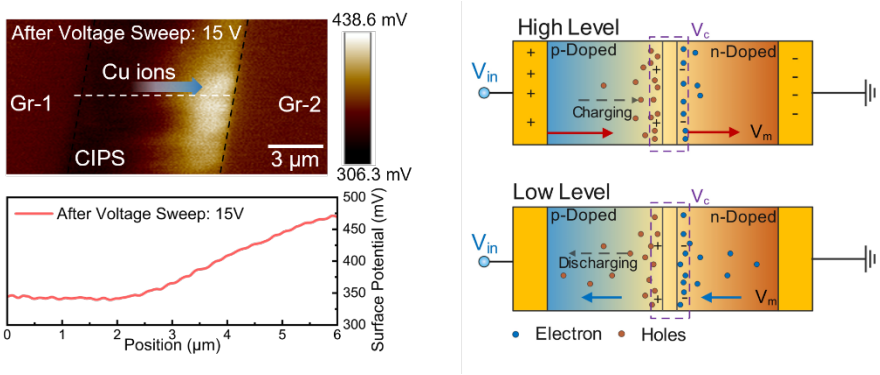


Fig. 4eand Fig. 4f

1.KPFM measurements reflect ion distribution, not carrier distribution.

The KPFM measurements presented in Fig. 4 were performed after applying a 15 V scanning voltage, with no bias applied during the KPFM measurement itself. Therefore, the observed surface potential distribution corresponds to the spatial distribution of Cu ions within the CIPS flake, rather than the distribution of free electrons and holes under operating conditions. This ion distribution is consistent with the EDS elemental mapping shown in Supplementary Fig. 3 and has been extensively reported in previous studies on CIPS-based devices, where Cu ion migration is established as the origin of resistive switching (ACS Appl. Electron. Mater. 2023, 5, 5625−5632; Materials Today 2023, 66, 9−16; ACS Nano 2023, 17, 1239−1246; Device 3, 100712, 2025).

2.The homojunction model describes carrier distribution under bias.

Fig. 4f illustrates the formation of a p–n homojunction resulting from Cu ion migration:

Cu-rich regions become n-type doped, while Cu-depleted regions become p-type doped, forming a p–n junction. This mechanism has been validated in prior work (ACS Nano 2023, 17, 1239−1246; Device 3, 100712, 2025). The depletion region depicted in Fig. 4f represents the region depleted of free carriers (electrons and holes), not a region depleted of Cu ions. This is entirely consistent with the KPFM results, which show a graded distribution of Cu ions across the channel. From such a graded distribution, one can naturally infer the existence of an intrinsic region between the Cu-enriched and Cu-depleted zones, which gives rise to the carrier depletion region under bias.

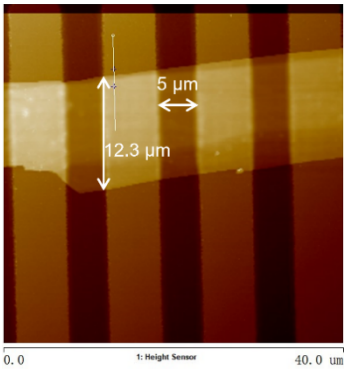
3.Regarding the possibility of an electrical double layer (EDL).

We do not exclude the possible presence of an EDL at the interfaces. However, its contribution to the measured capacitance is negligible compared to the junction capacitance. Quantitative analysis supports this conclusion:

As illustrated in the device structure, the device width and thickness are approximately 10 μm and 40 nm, respectively, with a channel width of 5 μm. Using a dielectric constant of approximately 300 for CIPS (Nano Energy 58 (2019) 596–603), the parallel-plate capacitance is estimated to be:

$$C = 8.854 \times 10^{-12} \times 300 \times \frac{(10 \times 10^{-6})(40 \times 10^{-9})}{5 \times 10^{-6}} = 0.21\ fF$$

This value is considerably smaller than the 12.1 pF obtained from *C*–*V* measurements, corresponding to a discrepancy of approximately four orders of magnitude.



Therefore, while an EDL may exist at the interfaces, the dominant capacitive contribution in our device arises from the p–n homojunction formed by Cu ion migration. We have incorporated these clarifications into the revised manuscript and

Supporting Information. We thank the reviewer for helping us articulate this distinction more clearly.

Location of Change: Result page 9:

Initially, the uniform surface potential distribution indicates no significant Cu^+ gradients (Fig. 4d). After a 15 V bias sweep, a ~120 mV potential drop emerges along the channel, signifying Cu^+ ions migrate toward the right electrode (Fig. 4e). As this measurement was performed at zero bias, this potential drop reflects the spatial distribution of migrated Cu^+ ions rather than the distribution of free carriers under operating conditions. This ion distribution is consistent with the EDS elemental mapping shown in Supplementary Fig. 3 and aligns with previous reports on CIPS-based devices.[37, 38, 41] The contact potential difference (V_{CPD}) distributions recorded after 30 min relaxation and subsequent −15 V sweep exhibit reconfigurability and nonvolatility (Supplementary Fig. 16), consistent with the RS behavior observed in electrical measurements. The resulting Cu^+ gradient establishes a built-in electric field and, based on prior studies is expected to dope the CIPS into n-type and p-type regions, forming a reconfigurable p–n homojunction (Supplementary Fig. 17). Under a forward bias, electrons injected from the n-type accumulate as minority carriers of the junction (Fig. 4f). This charge accumulation creates a diffusion capacitance that substantially exceeds conventional interfacial capacitance.[48]

6. In the manuscript, the authors mentioned the CIPS memristor can be operated in two distinctive modes: non-volatile memory arrays for the readout layer and dynamic modes for the physical reservoir. The reviewer thinks the experimental verification of the CIPS' dynamic modes for the physical reservoir is lacking in the current manuscript. Based on Fig. 2g, 3b, and Supplementary Figure 6, 8, the CIPS memristor showed long-term potentiation behavior, not dynamic memristive behavior, which requires that devices should return to the HRS state quickly. The reviewer suggests that the authors provide experimental demonstration showing CIPS memristor can behave like a dynamical memristor to utilize it as a physical reservoir. Hence, the reviewer thinks it is not logical to use the CIPS memristor as a physical reservoir for the reservoir computing framework.

Response: We thank the reviewer for this comment. We would like to clarify the definition of "dynamic memristive behavior" and explain why the CIPS memristor is well-suited for physical reservoir computing, even though its dynamics differ from the conventional decay paradigm.

In memristor, "dynamic" behavior refers to the evolution of the device state according to a set of differential equations that capture history-dependent effects. This is distinct from the simple resistance switching of static memories. The CIPS memristor is a second-order memristor governed by two coupled state variables: the ion migration front position *Wi*and the built-in electric field *Ei* (see Eqs. (1) and (2) in the main text). Its dynamics are therefore fully described by:

$$\frac{dW_i}{dt} = \mu\left(\frac{V_{in}}{L} - E_i\right)(1 - W_i)^{\alpha} - kE_i^{\beta}$$

$$\frac{dE_i}{dt} = \gamma\frac{V}{L}(W_0 - W_i)$$

These equations capture the competition between field-driven ion migration and spontaneous relaxation, giving rise to frequency-dependent plasticity, threshold sliding, and the non-monotonic EDE—all hallmarks of a truly dynamical system.

A physical reservoir must map input sequences into a high-dimensional dynamical state

space, from which a simple readout can extract features. This requires:

- Nonlinear dynamics,
- History dependence,
- The ability to project inputs into a rich repertoire of internal states.

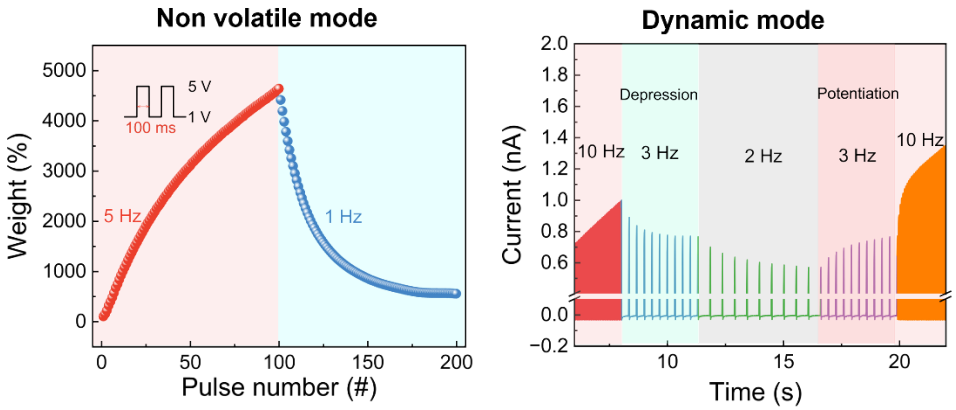
The CIPS memristor satisfies these criteria through the BCM-like plasticity it exhibits. The threshold sliding mechanism (Fig. 3f) provides a nonlinear, history-dependent response that effectively performs dimensionality reduction on spike-rate encoded inputs. Moreover, the EDE ensures that at very low input rates (including 0 Hz) the conductance remains stable, preventing unwanted drift—a feature that is actually beneficial for maintaining the reservoir's internal state integrity.

Two distinct operating modes.

We indeed envision two modes of operation for the CIPS memristor, and we agree that their experimental demonstration should be clearly distinguished:

1.Non-volatile mode: By exploiting the pronounced LTP and LTD obtained under high- and low-frequency stimulation (as in updated Figs. 2g, 3b, and Supplementary Figs. 6, 9), the device can function as a programmable synaptic weight in a conventional crossbar array. In this mode, the retention is intentionally enhanced by appropriate bias conditions (e.g., a read voltage of 1.5 V, as shown in Supplementary Fig. 9c).

2.Dynamic mode: Here we leverage the history-dependent sliding threshold and the EDE to process continuous spike trains. The conductance does not need to decay quickly to HRS; instead, the relevant dynamics are encoded in how the conductance evolves in response to the recent pulse history. Figures 3d and 3f demonstrate exactly this: the same input frequency can lead to potentiation or depression depending on the preceding activity, and the threshold frequency itself slides with past stimulation. These are precisely the properties needed for a reservoir: they provide a rich, nonlinear mapping of temporal input patterns into a high-dimensional state (the conductance value), which can then be read out by a simple linear classifier.



We are aware that many reservoir implementations rely on fast spontaneous decay (e.g., volatile memristors) to achieve a fading memory. Our approach is different—it exploits the intrinsic BCM dynamics, where memory fades through a spike-rate dependent sliding threshold rather than through simple relaxation. This is equally valid and, in fact, offers additional flexibility because the time scale of the memory can be tuned by the input statistics. We believe this represents a novel class of physical reservoir that has not been reported previously.

We hope this clarification addresses the reviewer's concern and demonstrates that the CIPS memristor, with its BCM-type dynamics, is indeed a legitimate and promising candidate for physical reservoir computing.

7. The detailed explanation of Fig. 5 is missing. Based on the contents in the manuscript and Supplementary Information, the reviewer thinks all data in Fig.5 were generated using simulation-based modeling of the behavior of CIPS memristor, not using physical devices. However, in the manuscript, this is not clear, which makes the reader confused. The reviewer suggests that the authors clarify this and add detailed modeling and simulation methods in the Methods section or Supplementary Information.

Response: We thank the reviewer for this valuable suggestion. In response, we have added detailed simulation procedures in the Methods section, as outlined below.

Location of Change: Methods page 15:

Simulation of the behavior of CIPS memristor

The simulation and modeling of the CIPS memristor are performed by numerically solving the device dynamics equations with a time step of $\Delta t = 0.001$ s. For a given input voltage sequence, a stepwise method is applied at each iteration: first, the memristor resistance is updated according to the dynamical equations using an explicit Euler method; then, based on the updated resistance, the algebraic constraints of the circuit (capacitive/resistive voltage division) are solved to obtain the new voltage and current values, which are subsequently used for the next time step.

1)Memristor dynamics equations

$$\frac{dW_i}{dt} = \mu\left(\frac{V_{in}}{L} - E_i\right)(1 - W_i)^{\alpha} - kE_i^{\beta}$$

$$\frac{dE_i}{dt} = \gamma\frac{V}{L}(W_0 - W_i)$$

$$G = G_L + W_i(G_H - G_L)$$

2) Parasitic capacitance voltage division

$$\frac{dV_c}{dt} = \frac{V_{in} - V_c}{R_m C} - \frac{V_c}{R_{leak} C}$$

$$V_m = V_{in} - V_c$$

For the simulation of CIPS device arrays, the state variables *Wi* of each device are stored in a matrix of the same dimensions as the array (the circuit configuration and input/output scheme are described in Supplementary Figure 25). By simulating the voltage sequences applied to the array inputs and the grounding conditions at the

outputs, the conductance change of each cell under the applied voltage is computed sequentially, and the output current is read accordingly. In the CIPS-based reservoir computing framework, two operating modes of the device are utilized. In the static mode, the weights obtained from the backpropagation algorithm are mapped to conductance values based on the measured LTP/LTD curves of the device. In the dynamic mode, the output current evolution under continuous voltage inputs is computed by solving the device dynamics equations.

Reviewer #3

This manuscript reports the realization of the complete Bienenstock-Cooper-Munro (BCM) synaptic plasticity rule in a single two-terminal memristor based on $CuInP_2S_6$ (CIPS). The BCM rule, a biologically inspired model, incorporates spike-rate-dependent plasticity with potentiation at high spike rates, depression at low rates, a sliding frequency threshold modulated by activity history (for homeostatic regulation), and an enhanced depression effect (EDE) at very low rates to prevent unchecked weight decay. The authors leverage the intrinsic properties of the CIPS memristor: second-order ionic dynamics (Cu^+ migration and built-in field feedback) for threshold sliding, and a junction parasitic capacitance that generates reverse voltage spikes during pulse intervals, enabling spike-rate-dependent depression and spontaneous EDE under natural spike-rate coding. No external gates, load resistors, or specialized encoding are required.

We thank the reviewer for these professional and insightful comments. We fully agree that the reliability and scalability of the device are indeed critical considerations that warrant careful attention. These challenges, however, are common in the field of two-dimensional material devices and represent ongoing areas of active research.

The primary contribution of our work is to provide a general strategy for realizing the complete BCM rule under natural spike-rate coding—a goal that has not been achieved in previous studies. By demonstrating this mechanism in a CIPS memristor and deriving its equivalent circuit model, we offer a platform-independent approach that can, in principle, be transferred to more mature and scalable memristor technologies (e.g., oxide-based devices) through the use of an external or integrated capacitor. As shown in the mechanism analysis section and Supplementary Fig. 22, our equivalent circuit model successfully reproduces the EDE behavior, confirming that the strategy is not limited to CIPS but can be generalized to other memristive systems.

We believe that by establishing this foundational mechanism, our work will inspire and

guide subsequent research toward more reliable and scalable implementations of BCM-based neuromorphic systems. Below, we address each of the reviewer's specific concerns point by point.

1. Exfoliated flake is used, which limits scalability.

Response: We thank the reviewer for raising this important point. We fully acknowledge that the use of exfoliated flakes, as in most studies involving two-dimensional materials, currently limits the scalability of our device. However, the primary contribution of this work lies in providing a proof-of-concept demonstration of a general strategy for realizing the complete BCM rule under natural spike-rate coding. The mechanistic insights gained from this prototype—particularly the role of intrinsic junction capacitance in generating EDE—are not tied to the specific material system and can inform the design of scalable implementations using more mature technologies (e.g., oxide-based memristors with integrated capacitors).

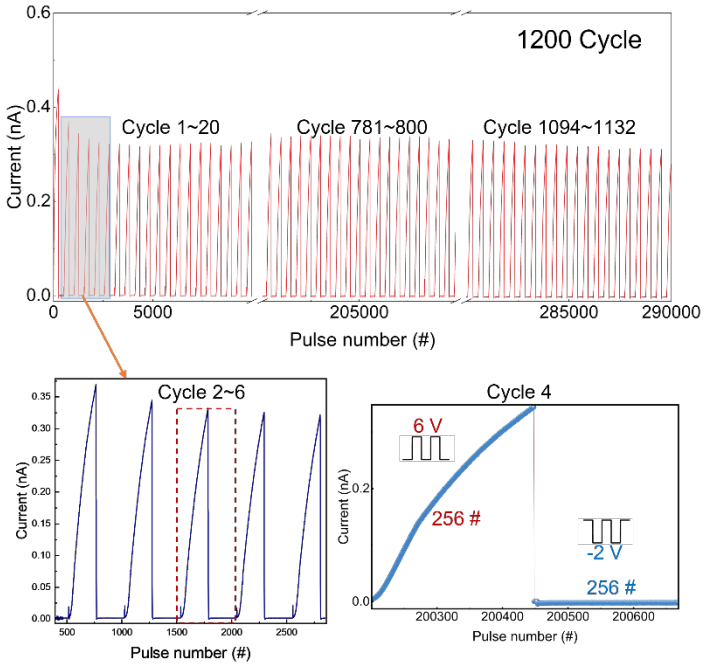
2. Limited endurance/reliability data: Only ~20 homojunction cycles shown; no extensive endurance tests (e.g., 10^6 pulses) or variability across devices (e.g., flake-to-flake stats). CIPS is vdW material, prone to defects/air sensitivity—how robust is it long-term?

Response: We thank the reviewer for these professional and insightful comments regarding device reliability and scalability. The stability and endurance of CIPS devices are actually quite excellent when properly encapsulated. Devices encapsulated with an organic thin film have been shown to remain functional for over 1 year under ambient conditions, demonstrating good long-term robustness.

To further address the reviewer's concern, we have now included additional endurance data in the revised manuscript (Supplementary Fig. 5). As shown in the figure, the device was subjected to over 3×10^5 pulses, comprising 1200 potentiation/depression cycles (each cycle consisting of 256 pulses). The device exhibits consistent switching behavior throughout the test, with good cycle-to-cycle uniformity, demonstrating that

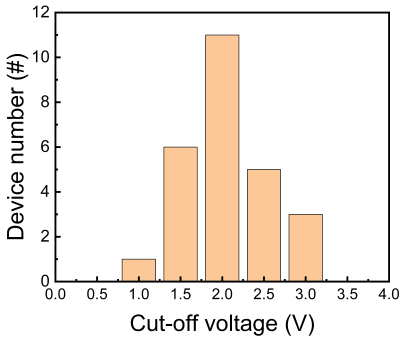
the CIPS memristor can sustain extensive operation without significant degradation.

Newly updated reversible switching in Supplementary Figure 5 to replacing the old:



We acknowledge that device-to-device uniformity remains a key challenge for two-dimensional materials, including CIPS. As summarized in our response to Reviewer #1 Comment 6, the threshold voltage for conductance switching varies across devices, typically ranging from 1.5 V to 2.5 V (based on statistics from 26 devices). This variability is primarily attributed to differences in flake quality, thickness, and interface contact conditions—factors that are common in exfoliated 2D material devices and represent an ongoing area of research. We have added this statistical distribution in Supplementary Fig. 7.

Newly added statistical distribution of threshold voltages for 26 devices:



CIPS is indeed sensitive to ambient conditions, particularly moisture and oxygen. However, as noted above, encapsulation with hBN or organic thin films has proven effective in mitigating degradation. Encapsulated devices retain their functionality for over one year, confirming that the material can be stabilized for practical applications. We have included this discussion in the revised manuscript (Device fabrication section).

We thank the reviewer for pushing us to provide a more comprehensive assessment of device reliability. These additions significantly strengthen the manuscript and provide a clearer picture of the current capabilities and limitations of CIPS-based devices.

Location of Change: Methods page 15:

Device Fabrication

Devices for electrical measurements: The electrodes were fabricated by depositing 5 nm/50 nm Cr/Au via magnetron sputtering on a Si substrate with a 300 nm SiO_2 layer (purchased from Harbin Tebo Technology). Standard photolithography and argon ion etching processes were used to pattern the electrodes, with a channel width of 5 μm between them. CIPS flakes were mechanically exfoliated from bulk crystals (purchased from SUNANO GROUP) and transferred onto the electrodes using a dry transfer technique. To prevent ambient degradation and ensure long-term stability, the devices were immediately encapsulated after fabrication with a thin PMMA or a hBN capping layer. Encapsulated devices have been shown to retain their functionality for over one year under ambient conditions.

3. Lateral structure (5 μm channel) is bulky for dense arrays; vertical stacking or integration with CMOS isn't addressed. Parasitic capacitance (~12 pF) might scale poorly or introduce crosstalk in crossbars.

Response: We thank the reviewer for raising this important point regarding scalability and integration. We fully acknowledge that the lateral structure (5 μm channel) used in this work is indeed bulky for high-density arrays, and that the integration of 2D materials with CMOS back-end-of-line processes remains an ongoing challenge in the field. Furthermore, the parasitic capacitance (~12 pF) may introduce crosstalk or scaling limitations in large crossbar arrays if not properly managed.

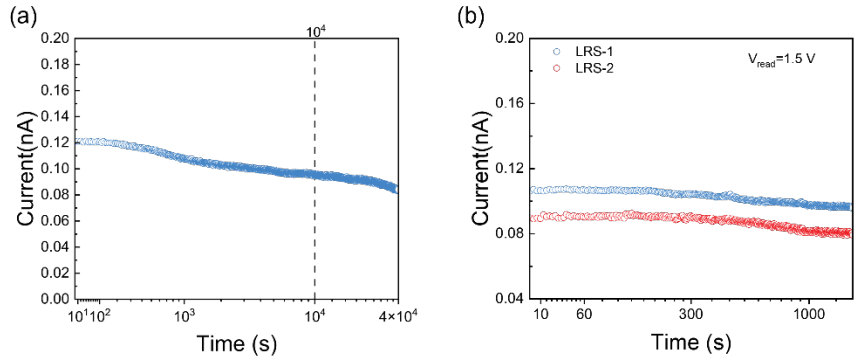
However, it is important to emphasize that the CIPS memristor presented here is a prototype device, intended to demonstrate a proof-of-concept strategy for realizing the complete BCM rule under natural spike-rate coding—a goal that has not been achieved in previous studies. The primary contribution of this work lies in the mechanistic insight and the equivalent circuit model derived from it, which together establish a general approach that can be transferred to more scalable platforms.

As demonstrated in the manuscript, the core mechanism—using a capacitor in series with a memristor to generate frequency-dependent depression—can be implemented in oxide-based memristors with integrated capacitors. Such platforms are already compatible with CMOS back-end-of-line integration and offer much better scalability and uniformity. We believe that by providing this general strategy, our work will inspire and guide subsequent research toward practical, large-scale implementations of BCM-based neuromorphic systems.

4. Retention is only tested to 3600 s; claims of non-volatility need longer tests (> 10^4 s) or acceleration studies.

Response: We thank the reviewer for this valuable suggestion. Following this recommendation, we have performed additional retention measurements extending beyond 4 × 10^4 s (~11 hours). As shown in the updated Supplementary Fig. 6, the device maintains two distinct conductance states with clear separation over the entire testing period, confirming the non-volatile nature of the CIPS memristor. These results have been incorporated into the revised manuscript. We thank the reviewer for helping us strengthen the experimental validation of device retention.

Newly updated reversible switching in Supplementary Figure 6 to replacing the old:



5. Could interfacial defects contribute to the switching?

Response: We thank the reviewer for this insightful question. While we cannot completely exclude the possibility that interfacial defects contribute to the switching behavior, multiple lines of evidence suggest that the dominant mechanism is bulk ion migration rather than interfacial effects: (i) the clear Cu^+ distribution gradient observed in KPFM and EDS mapping (Adv. Mater. 2023, 35, 2302419; Materials Today 2023 Vol. 66 Pages 9-16; ACS Nano 2023 Vol. 17 Issue 2 Pages 1239-1246; Device 3, 100712, May 16, 2025), (ii)the successful reproduction of EDE using an equivalent circuit model without invoking interfacial traps. Nevertheless, interfacial defects may play a secondary role, particularly in device variability or retention, and we have added a brief discussion of this point in the revised manuscript.

6. EDE is pulse-induced, not spontaneous decay, but low-frequency depression (31% vs. 5% at 0 Hz) implies some volatility; reconcile with non-volatile claims?

Response: We thank the reviewer for this important question. In Fig. 3b, the purpose was to compare device behavior under constant bias (0 Hz) versus low spike rate stimulation (0.5 Hz). The results show as follows:

1.Under 0 Hz (constant 1 V bias), the conductance exhibits only ~5% decay over 100 s, confirming that the device remains largely non-volatile in the absence of input.

2.Under 0.5 Hz pulse stimulation, a much stronger ~31% depression is observed, which is actively driven by the reverse voltage spikes from the junction capacitance, not by spontaneous relaxation.

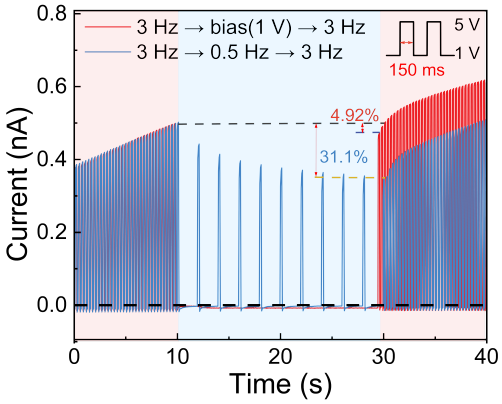


Figure 3b

This distinction is critical: EDE-driven depression is a controlled, input-dependent process, whereas spontaneous decay is an undesirable passive effect. As demonstrated in Fig. 2g, the non-volatility of the device can be further enhanced by increasing the read bias, which suppresses relaxation. Moreover, as shown in our extended retention test (Supplementary Fig. 6, >4 × 10^4 s), the two conductance states remain clearly distinguishable even after prolonged periods, confirming that the device retains its non-volatile nature despite the presence of some minimal relaxation—a feature also observed in biological synapses, where partial forgetting is physiologically plausible.

We have clarified this distinction in the revised manuscript to avoid any confusion.

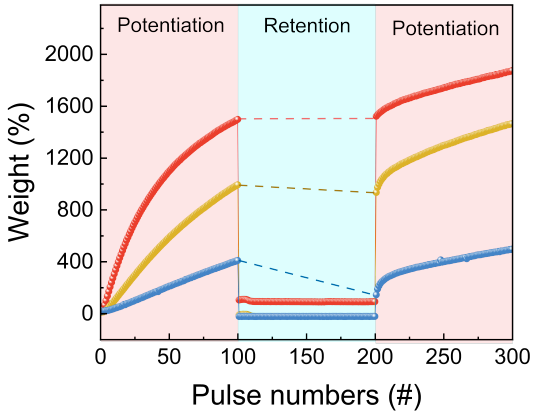

Potentiation
Retention
Potentiation
Weight (%)
2000
1600
1200
800
400
0
0
50
100
150
200
250
300
Pulse numbers (#)

Fig. 2g

Reviewer #1:

The authors have addressed most of the issues. However, I recently came across a published paper titled 'Polymorphic Functionalization Driven by Ion Displacement-Induced Antiferroelectric Ordering in $CuBiP_2Se_6$,' which demonstrates that the BCM rule can be enabled by antiferroelectric materials. In contrast, the implementation of the BCM rule in the current manuscript relies on ferroelectric materials. Therefore, the authors should explicitly discuss the differences between their study and this recent publication. Specifically, what are the advantages of utilizing ferroelectric materials for the BCM rule compared to antiferroelectric materials?

Response: We thank the reviewer for bringing the recent publication to our attention (Nat. Commun. 2025, 16, 10666). In that work, the authors utilize the antiferroelectric–ferroelectric phase transition to realize a memristor with relaxation behavior, and then implement the BCM rule via triplet-STDP encoding. However, in our opinion, the realization of the BCM rule in that study is not fundamentally linked to the antiferroelectric property. Moreover, the adopted triplet-STDP strategy is essentially the same as that reported in earlier works (e.g., Adv. Electron. Mater. 2024, 2400612). As we have already introduced triplet-STDP encoding in the Introduction section of our manuscript, we will add a citation to this recent paper there.

Regarding our work, we note that the ferroelectricity of $CuInP_2S_6$ (CIPS) originates from the off-centering of Cu ions within the lattice and is typically observed only in vertical device structures. Therefore, in our lateral-structured devices, we do not exploit the ferroelectricity of CIPS; instead, the resistive switching mechanism is based on long-range migration of Cu ions in the lateral direction. More importantly, the key enabler for realizing the BCM rule in our device is the intrinsic junction parasitic capacitance, which introduces a frequency-dependent depression. This allows the full BCM rule, including EDE, to be implemented under natural spike-rate coding without

any special encoding schemes. This demonstrates that intrinsic competing dynamics in a two-terminal device can give rise to the non-monotonic behavior required for the BCM rule. We also note that a conceptually similar phenomenon has been reported in a very recent study (Nat. Commun. 2026, 17, 3367), where introducing a voltage-dependent barrier layer also enables conductance depression under pulsed stimulation.

We thank the reviewer again for the valuable suggestion and hope the above clarification addresses the concern. We have added citations to these relevant papers in the Introduction section of the revised manuscript.

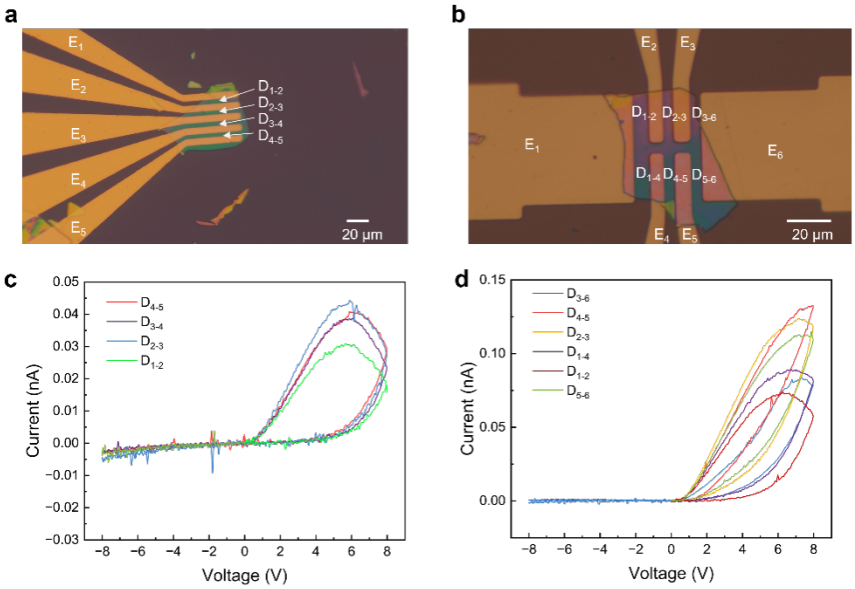
The addtional comments for cross-check are shown below:

1. Other Reviewer's Comment: Exfoliated flake is used, which limits scalability.

My response: Regarding the scalability issue, exfoliated flakes are commonly used in 2D materials research. While this approach inherently limits scalability, this is a well-known challenge for the entire 2D materials community rather than a flaw to be completely resolved in a single paper. **Nevertheless, to adequately address Reviewer #3's concern, it would be advisable for the authors to fabricate and demonstrate a small device array.**

Response: We thank Reviewer #1 for this cross-check comment. We fully acknowledge that the use of exfoliated flakes limits device scalability, a well-recognized challenge for the entire two-dimensional materials community.

To address this concern, we fabricated two small device arrays on a single flake: one 1×4 array and one 2×3 array, as shown in the figure below. The devices exhibited acceptable consistency during *I*–*V* sweeps and all showed unidirectional rectification after forming a forward p–n junction, demonstrating the feasibility of integrating multiple devices on the same flake.



Moreover, we note that CIPS intrinsically offers advantages for scalability due to its

wide bandgap, which results in negligible leakage current. It has been demonstrated that vertical crossbar arrays can be directly fabricated on CIPS without additional insulation layers, thereby avoiding crosstalk issues (Nano Lett. 2023, 23, 4524–4532). This indicates that CIPS is a promising material platform for future large-scale integration.

We hope these additional demonstrations and discussions adequately address the scalability concern raised by Reviewer #3. We thank Reviewer #1 for the constructive suggestion.

2. Other Reviewer's Comment: Limited endurance/reliability data: Only ~20 homojunction cycles shown; no extensive endurance tests (e.g., 10^6 pulses) or variability across devices (e.g., flake-to-flake stats). CIPS is vdW material, prone to defects/air sensitivity— how robust is it long-term?

My response: I agree with this comment. It is understandable that 2D materials lose their advantage in scalability; however, in my opinion, for fundamental research, the adequate performance parameters of a single device should still be demonstrated.

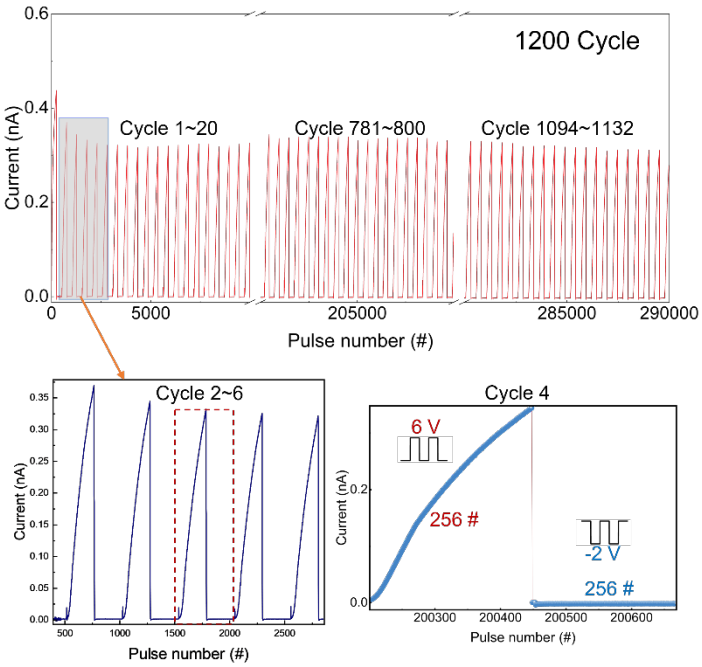
Response: We thank Reviewer #1 for this cross-check comment and fully agree that the performance parameters of a single device are indeed worth careful examination. Regarding long-term robustness, we have found that CIPS devices, when properly encapsulated, exhibit excellent stability. Devices encapsulated with an organic thin film have been shown to remain functional for over 1 year under ambient conditions, demonstrating good long-term reliability. We have added details of the encapsulation process and a discussion of device durability in the Methods section.

To further address the reviewer's concern, we have included additional endurance data in the revised manuscript (Supplementary Fig. 5). As shown in the figure, the device was subjected to over 3×10^5 pulses, undergoing 1,200 potentiation/depression cycles (each cycle consisting of 256 pulses), with no significant degradation in performance. The device exhibited consistent switching behavior throughout the test and reasonable cycle-to-cycle consistency, indicating that CIPS memristors can sustain prolonged operation without significant performance deterioration.

We also acknowledge that device-to-device uniformity remains a key challenge for two-dimensional materials, including CIPS. Based on our statistical analysis of 26 devices, the threshold voltage for conductance switching typically ranges from 1.5 V to 2.5 V. This variability is primarily attributed to differences in flake quality, thickness, and interface contact conditions—common issues in exfoliated 2D material devices. Notably, devices fabricated from the same CIPS flake generally exhibit good uniformity, as also demonstrated in previous work (Materials Today, Vol. 66, June 2023).

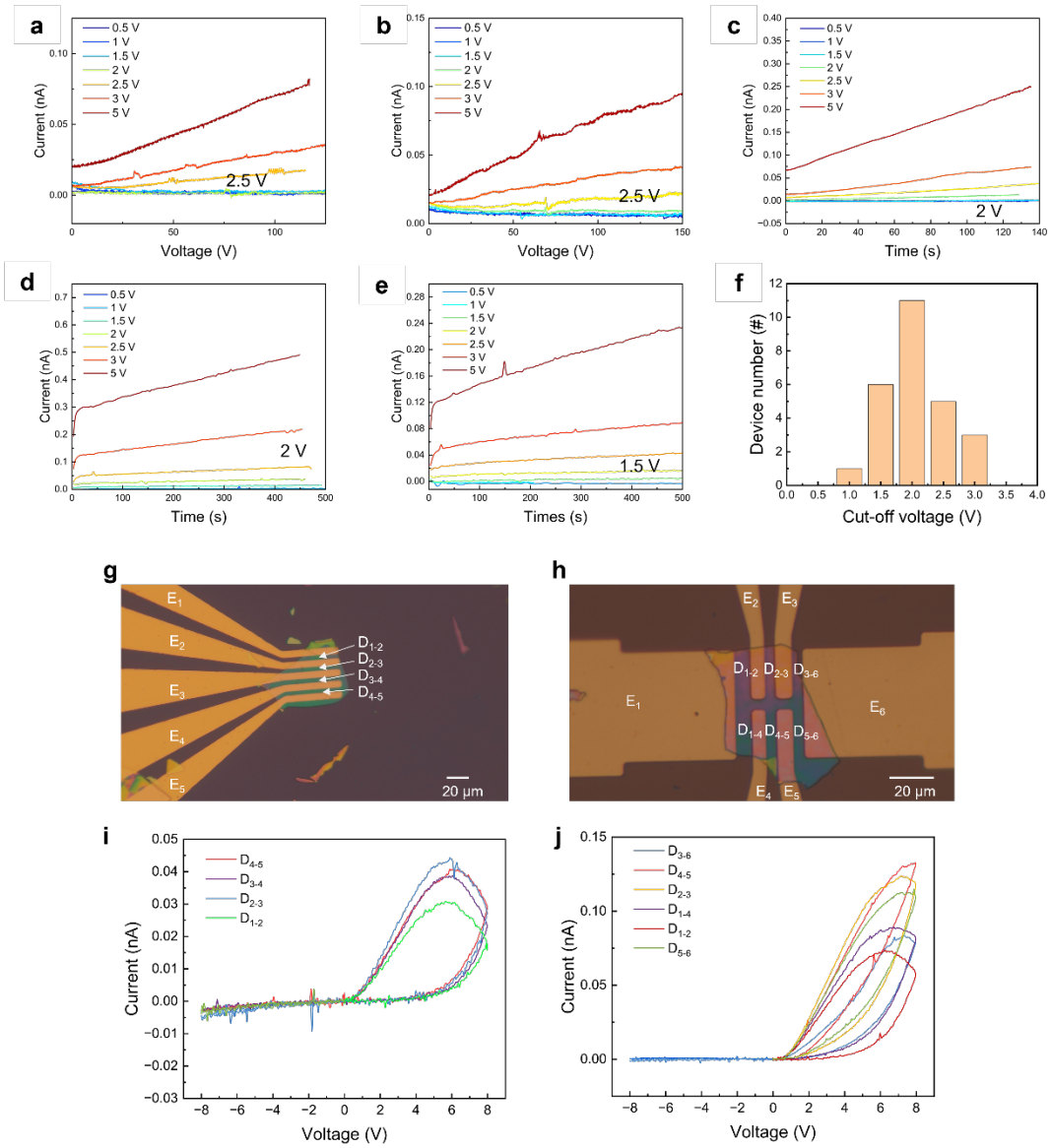
We hope these additions and clarifications adequately address the concerns raised by Reviewer #3. We thank Reviewer #1 for the constructive suggestion.

Newly updated reversible switching in Supplementary Figure 5 to replacing the old:



Supplementary Fig. 5 (The reason of the current height gradually decreases in the previous cycles in the figure is that the accumulation of historical stimuli is gradually erased.)

Newly updated device arrays in Supplementary Figure 7:



Supplementary Fig. 7

Location of Change: Methods page 15:

Device Fabrication

Devices for electrical measurements: The electrodes were fabricated by depositing 5 nm/50 nm Cr/Au via magnetron sputtering on a Si substrate with a 300 nm SiO_2 layer (purchased from Harbin Tebo Technology). Standard photolithography and argon ion etching processes were used to pattern the electrodes, with a channel width of 5 μm between them. CIPS flakes were mechanically exfoliated from bulk crystals (purchased from SUNANO GROUP) and transferred onto the electrodes using a dry transfer

technique. To prevent ambient degradation and ensure long-term stability, the devices were immediately encapsulated after fabrication with a thin PMMA or a hBN capping layer. Encapsulated devices have been shown to retain their functionality for over 1 year under ambient conditions.

3. Other Reviewer's Comment: Lateral structure (5 μm channel) is bulky for dense arrays; vertical stacking or integration with CMOS isn't addressed. Parasitic capacitance (~12 pF) might scale poorly or introduce crosstalk in crossbars.
My response: While I agree that the authors should address the parasitic capacitance issue, I consider the other points raised in this comment to be beyond the scope of the current work

Response: We thank Reviewer #1 for this constructive cross-check comment. We fully acknowledge that the lateral structure (5 μm channel) used in this work is indeed bulky for high-density arrays. However, it is important to emphasize that the CIPS memristor presented here is a prototype device, intended to demonstrate a proof-of-concept strategy for realizing the complete BCM rule under natural spike-rate coding. The primary contribution of this work lies in the mechanistic insight and the equivalent circuit model derived from it, which together establish a general approach that can be transferred to more scalable platforms.

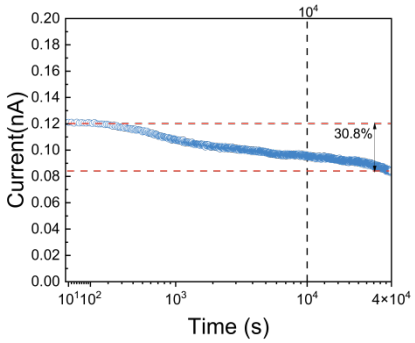
Regarding the parasitic capacitance (~12 pF), we agree that it may introduce crosstalk in large crossbar arrays if not properly managed. Nevertheless, as demonstrated in the manuscript, the core mechanism—using a capacitor in series with a memristor to generate frequency-dependent depression—can be implemented in oxide-based memristors with integrated capacitors. Such platforms are already compatible with CMOS back-end-of-line integration and offer much better scalability and uniformity. We believe that by providing this general strategy, our work will inspire and guide subsequent research toward practical, large-scale implementations of BCM-based neuromorphic systems.

We hope this clarification addresses the concerns raised by Reviewer #3. We thank Reviewer #1 again for the valuable suggestion.

4. Other Reviewer's Comment: Retention is only tested to 3600 s; claims of non-volatility need longer tests (> 10^4 s) or acceleration studies.

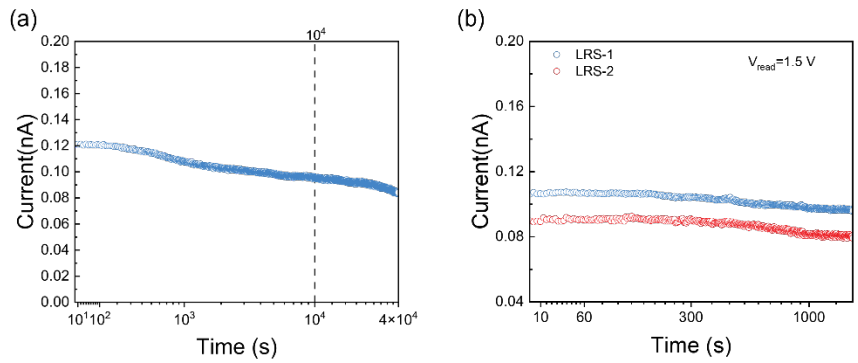
My response: I agree this reviewer.

Response: Following this suggestion, we performed additional retention measurements. The results show that after 4×10^4 s (~11 hours), the conductance decayed by approximately 30.8%. To further demonstrate that the two conductance states remain distinguishable, we characterized the retention behavior of eight devices with different initial states, all of which remained clearly distinguishable after one hour. To avoid overstatement, we have revised the description of retention in the manuscript to more objectively reflect the observed changes after 4×10^4 s.



The Conductance decay due to spontaneous ion diffusion is a common issue in ionic memristors. In our experiments, we found that applying a small bias to the CIPS device can effectively prevent spontaneous ion diffusion, resulting in longer retention (Fig. 2g). This operation is practically feasible: applying a 2 V bias when the device is idle can significantly extend the retention time. These results have been incorporated into the revised manuscript.

Newly updated retention time in Supplementary Figure 6 to replacing the old:



Location of Change: Manuscript page 6:

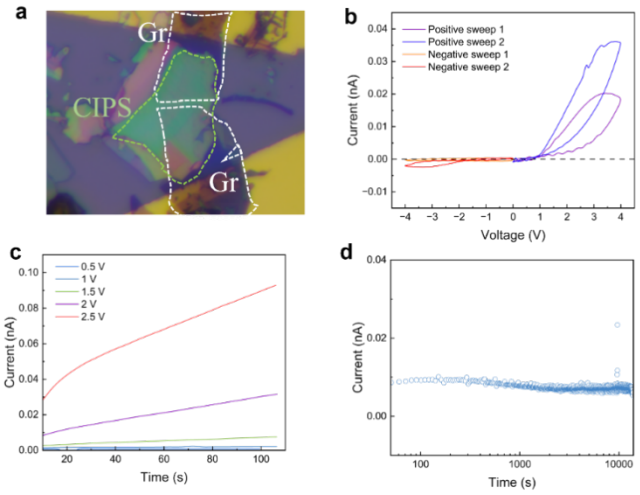
The retention measurement indicates that the LRS remains distinguishable from the HRS after at least 4 × 10^4 s, retaining approximately 70% of its initial conductance (Supplementary Fig. 6). This validates the nonvolatile nature of the resistive states and the device's suitability for neuromorphic applications where long-term information retention is essential.

5. Other Reviewer's Comment: Could interfacial defects contribute to the switching?

My response: I agree with the reviewer. The authors should clarify this point to better explain the working mechanism.

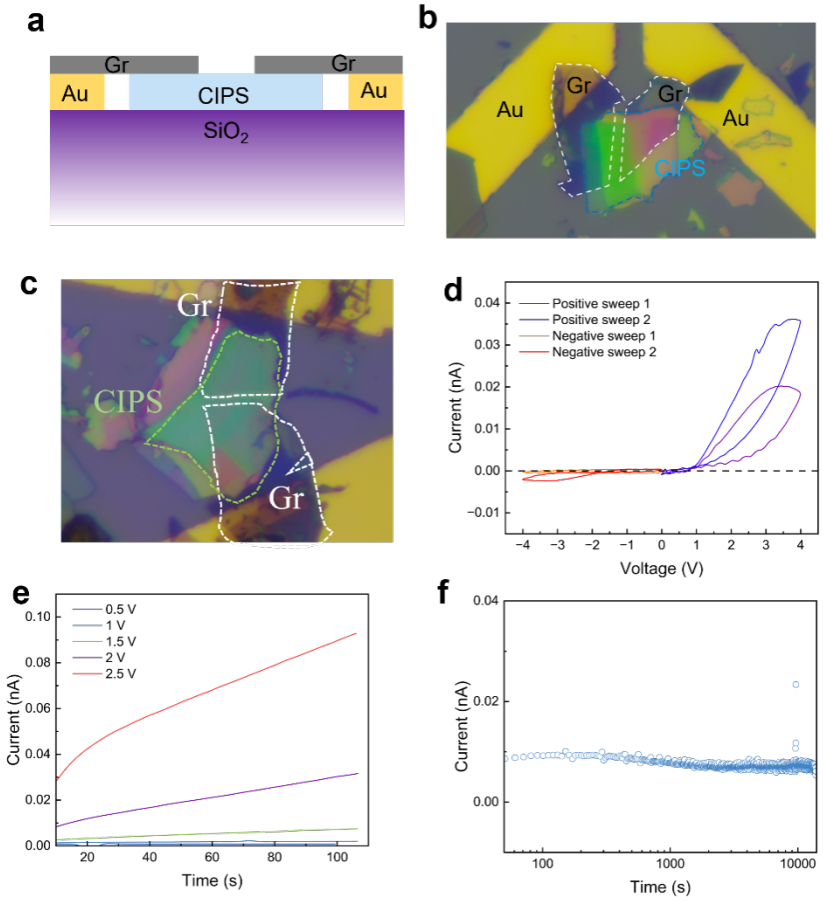
Response: We agree that the possible role of interfacial defects should be clarified to better explain the working mechanism. While we cannot completely exclude the contribution of interfacial defects, multiple lines of evidence suggest that the dominant switching mechanism is bulk ion migration rather than interfacial effects. Clear Cu^{+} distribution gradients observed by KPFM and EDS mapping, as reported in previous studies (Adv. Mater. 2023, 35, 2302419; Materials Today 2023, 66, 9–16; ACS Nano 2023, 17, 1239–1246; Device 3, 100712, 2025).

To further investigate the role of interfacial defects, we replaced the magnetron-sputtered Au electrodes with van der Waals-contacted graphene electrodes. Van der Waals contacts between 2D semiconductors and 2D semi-metallic electrodes can significantly reduce interfacial defects and lower contact resistance (npj 2D Materials and Applications, 2022, 6, 66). The resulting devices still exhibited a reconfigurable p–n junction and retained a retention time exceeding 10^4 s (results have been added as Supplementary Figure 15). This experiment indicates that the switching mechanism in CIPS devices is largely governed by ion migration, with no clear evidence of a dominant role from interfacial defects.



We have added a brief discussion of this point in the revised manuscript. We thank the reviewer for helping us strengthen the mechanistic understanding of our device.

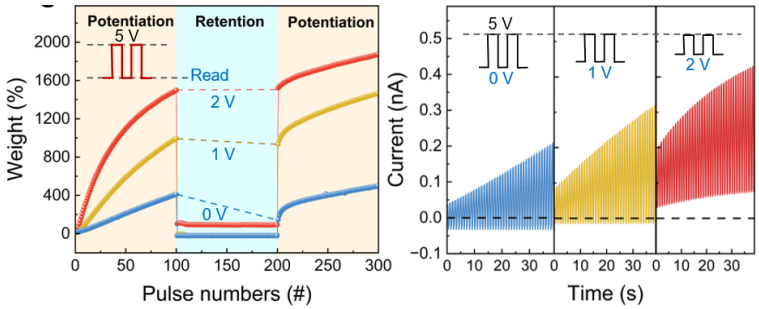
Newly updated Au/Gr/CIPS/Gr/Au structure in Supplementary Figure 15:



6. Other Reviewer's Comment: EDE is pulse-induced, not spontaneous decay, but low-frequency depression (31% vs. 5% at 0 Hz) implies some volatility; reconcile with non-volatile claims?

My response: I agree with the reviewer on this point. The authors should provide a clear explanation to address this concern.

Response: We thank the reviewer for this important comment. We fully acknowledge that, as with many ionic memristors, spontaneous ion back-diffusion in the absence of an external field is an inherent challenge that can affect non-volatility. To mitigate this, we apply a constant low-level bias (0-2 V) during device idle periods, which reduces the spontaneous decay rate without altering the conductance state (as shown in Figs. 2g–h). However, this bias also partially counteracts the depression effect generated by the junction capacitance at low frequencies. Therefore, the choice of 1 V represents a trade-off to achieve the desired EDE behavior while accepting a moderate level of spontaneous decay.



Furthermore, as demonstrated in our extended retention test (Supplementary Fig. 6, >4 × 10^4 s), the two conductance states remain clearly distinguishable even after prolonged periods, confirming that the device retains its non-volatile nature despite a certain degree of relaxation—a feature also observed in biological synapses, where partial forgetting is physiologically plausible. Moreover, the decay rate gradually decreases over time. It should be emphasized that the applied low-level bias is intended to counteract non-ideal spontaneous relaxation. If the issue of spontaneous ion diffusion could be fully resolved in the future, no additional bias would be needed, and the depression effect arising from the junction capacitance would become even more

pronounced.

We have added a discussion of this trade-off in the revised manuscript and clarified the rationale for selecting a 1 V low-level bias (see revised sentences in the manuscript, as quoted below).

Revised text in the manuscript

Location of Change: Result page 6:

As shown in Fig. 2g, by applying pulse sequences (high level: 5 V, low levels: 0, 1, 2 V), the sub-threshold voltages still significantly modulate ion migration, and the non-volatility of the device improves with increasing low-level bias.

Location of Change: Result page 7:

To compare the effects of spontaneous decay and capacitive effect, we compared the depression behavior under constant 1 V bias with that under 0.5 Hz pulsed stimulation (5 V, 150 ms), after initializing the device to the same LRS using 3 Hz pulses (Fig. 3b).

Reviewer #2:

The authors properly addressed most of the Review#3's comments, but I still have some concerns.

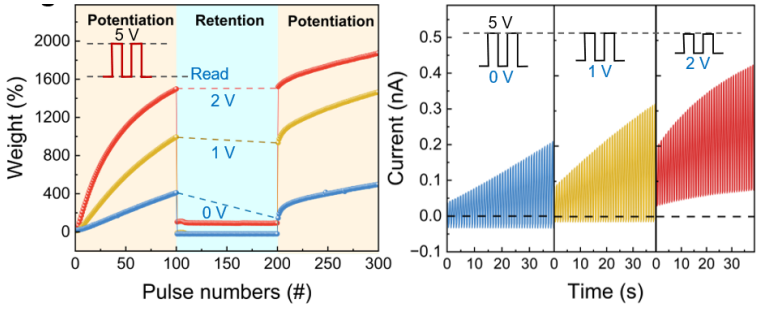
1.In the revised Supplementary Figure 6, the authors provided a longer retention test to reply the Reviewer #3's comment (comment 4). However, based on the figure, the current from the memristor indeed decreases over time, and it gets worse when measured up to 4 x 104 s. The reviewer thinks this is the inherent limitation of ion-based two-terminal devices, as the ion can spontaneously diffuse back when there is no external field. A similar short retention time also can be found in other ion-based memristive devices (Onen et al., Science, 277, 2022). In the current revised version, the authors only showed two conductance states, so it might not be an issue, but this degradation can be an issue if we want to store multiple bits of information into this device. The reviewer concerns that the author overclaimed the retention behavior of their CIPS-based devices.

Response: We thank the reviewer for the continued critical assessment. We fully agree that the gradual decrease in conductance over time, as shown in the extended retention test (Supplementary Fig. 6), reflects an inherent limitation of ion-based two-terminal devices, where spontaneous ion back-diffusion occurs in the absence of an external field. We therefore appreciate the reviewer's concern that such degradation could become more problematic for multi-bit storage applications.

To avoid overstatement, we have revised the description of retention in the manuscript to be more objective. Specifically, we now state that the LRS remains distinguishable from the HRS after at least 4×10^4 s, retaining approximately 70 % of its initial conductance (Supplementary Fig. 6). We have also emphasized that this decay can be mitigated by applying a constant low-level bias below the switching threshold (as demonstrated in Fig. 2g–h), which reduces spontaneous ion diffusion without altering the conductance state. In future work, further suppression of ion back-diffusion—for

example through improved encapsulation or material engineering—could enhance retention for multi-level applications.

We have incorporated the revised sentence into the manuscript (Results, page 6) as quoted below. We thank the reviewer for helping us present the device performance more accurately.



Figs. 2g–h

Revised text in the manuscript

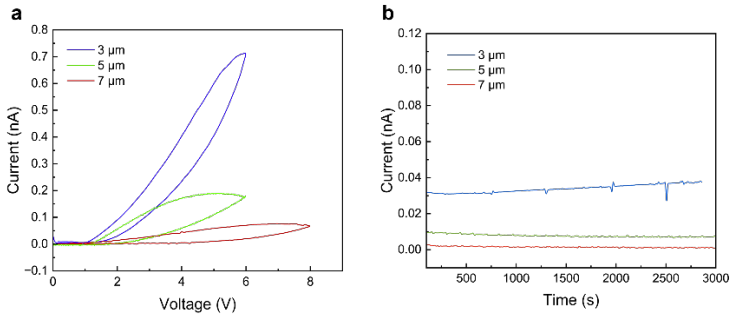
Location of Change: Result page 6:

The retention measurement indicates that the LRS remains distinguishable from the HRS after at least 4 × 10^4 s, retaining approximately 70% of its initial conductance (Supplementary Fig. 6).

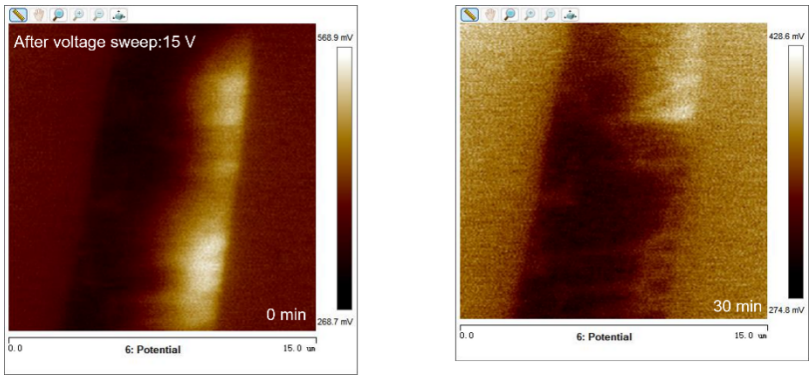
2. Another point is that the Reviewer #3 pointed out the long channel length (5 μm) of the current devices. The authors replied that this device is a prototype, and scaling the device is not in the scope. However, the reviewer thinks that since their device uses ion diffusion in the lateral direction, if the channel length gets shorter for higher scalability, the retention time will become even worse due to shorter diffusion length. Based on the author's reply to the Reviewer #3's comments, the reviewer further raises the retention issue of this CIPS memristor if the channel lengths get shorter.

Response: We thank the reviewer for raising this important issue. In our work, the 4–5 μm channel length was chosen as a practical compromise: shorter channels (3 μm) exhibited poorer endurance and were more prone to breakdown, while longer channels made the current too weak to measure reliably.

To further examine the effect of channel length on retention, we characterized devices with channel lengths of 3 μm, 5 μm, and 7 μm. Their *I*–*V* characteristics are shown in the figure below. Both the turn-on voltage and resistance increase with channel length. Devices with 5 μm and 7 μm showed no significant difference in retention over 3000 s when read at 1.5 V (a voltage below the turn-on threshold). Interestingly, the 3 μm device exhibited a faster initial decay (first 200 s) but then a gradual conductance increase. We speculate that while a shorter channel may intrinsically suffer from faster ion back-diffusion, the same read bias (1.5 V) generates a stronger electric field across the shorter channel, which helps to maintain the ion distribution and even drives further ion migration in the 3 μm device. To test this hypothesis, we set the devices to the LRS and then left them unbiased for 30 min before reading. The 3 μm device almost completely relaxed back to the HRS, whereas the 5 μm and 7 μm devices retained about 30 % of their LRS conductance. This confirms that in the absence of any bias, a shorter channel does lead to faster decay. (Since any reading pulse will drive the junction capacitance in the device to generate a suppression effect, we cannot obtain the curve of the attenuation behavior at zero bias.)



The ion diffusion process was also directly visualized by KPFM. The figure below shows the surface potential distribution after a 15 V scan and after 30 min of unbiased relaxation. A 6 μm channel device still retained a clear potential gradient after 30 min, consistent with the electrical measurements.

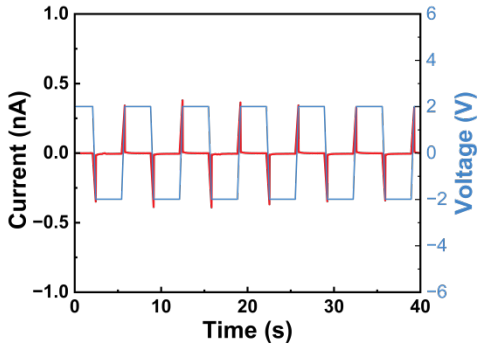


We fully agree that scalability is a major challenge for 2D materials, which we have already discussed in the manuscript and attempted to address by proposing an equivalent circuit strategy that can be transferred to more scalable memristor platforms. We acknowledge that a systematic study of channel length scaling and its impact on retention would be valuable, but such an investigation lies beyond the scope of the present work, as it would require extensive device optimization and statistical analysis. Given that we currently lack direct retention data for channels shorter than 3 μm, we have decided not to include the above discussion in the revised manuscript. We respectfully hope that the reviewer can understand this decision.

3. Since the authors used lateral-type devices, the operating frequency is quite low (max 25 Hz) and the pulse width is quite long (minimum 30 ms). The reviewer suggests the authors provide discussion to increase the operation frequency of the devices and lower the pulse width of the devices.

Response: We thank the reviewer for raising this important practical issue. We fully agree that increasing the operating frequency and reducing the pulse width are crucial for engineering applications.

In our CIPS lateral-type devices, the operating speed is limited by the intrinsic RC time constant. Based on our measurements, the device resistance is approximately $10^{10}\ \Omega$ and the junction capacitance is about 10 pF, giving an estimated RC time constant of ~0.1 s (i.e., ~10 Hz). This is why the chosen pulse width (minimum 30 ms) and frequency range (0.1–25 Hz) are appropriate for this specific device. As shown in the figure below (pulse width 3000 ms), the charge/discharge spikes are clearly visible. If the pulse width is much smaller than the RC time constant, the signal would be completely dominated by the capacitive transient and could not be properly resolved.



We acknowledge that the intrinsic material properties of CIPS limit further improvement in this specific device. However, as demonstrated in our manuscript, the proposed mechanism can be transferred to conventional memristor platforms via an equivalent circuit strategy. In our equivalent circuit experiment (Extended Data Fig. 2), using a 1 MΩ resistor and a 37 pF capacitor, the RC time constant is reduced to the order of 10^{-5} s, enabling an operating frequency range of 0.1–10 kHz. This shows that our approach is not inherently limited to low frequencies; rather, it can be adapted to

much faster memristor technologies.

We have added a discussion of this frequency limitation and the potential for improvement via the equivalent circuit strategy in the **Conclusions section** of the revised manuscript. We thank the reviewer for pushing us to address this important engineering question.

Revised text in the manuscript

Location of Change: Conclusions, page 14:

By coupling the pulse-induced potentiation and depression in the CIPS memristor, a non-monotonic EDE is achieved. Furthermore, a general dynamic framework is established in which the coupling of junction capacitance and second-order ionic dynamics fully reproduces the BCM rule. The mechanism is experimentally validated by emulating the junctional voltage-division effect with a series RC circuit, successfully reproducing the EDE behavior in conventional memristors. While the intrinsic RC time constant of the CIPS device limits its operating frequency to the order of 0–25 Hz, the equivalent circuit strategy enables much higher frequency operation (kHz range) on conventional memristor platforms. Owing to its strong biological compatibility with existing synaptic devices, this hardware-oriented strategy can be seamlessly integrated into established neuromorphic architectures. It thus provides an intrinsic solution to the long-standing stability–plasticity dilemma and opens a path toward adaptive, brain-inspired computing systems.