Supplementary Information

Wafer-Scale 2D MoS_2 Transistors with Sub-5 nm Channel Length and Subthreshold Performance Beyond the Silicon Limit

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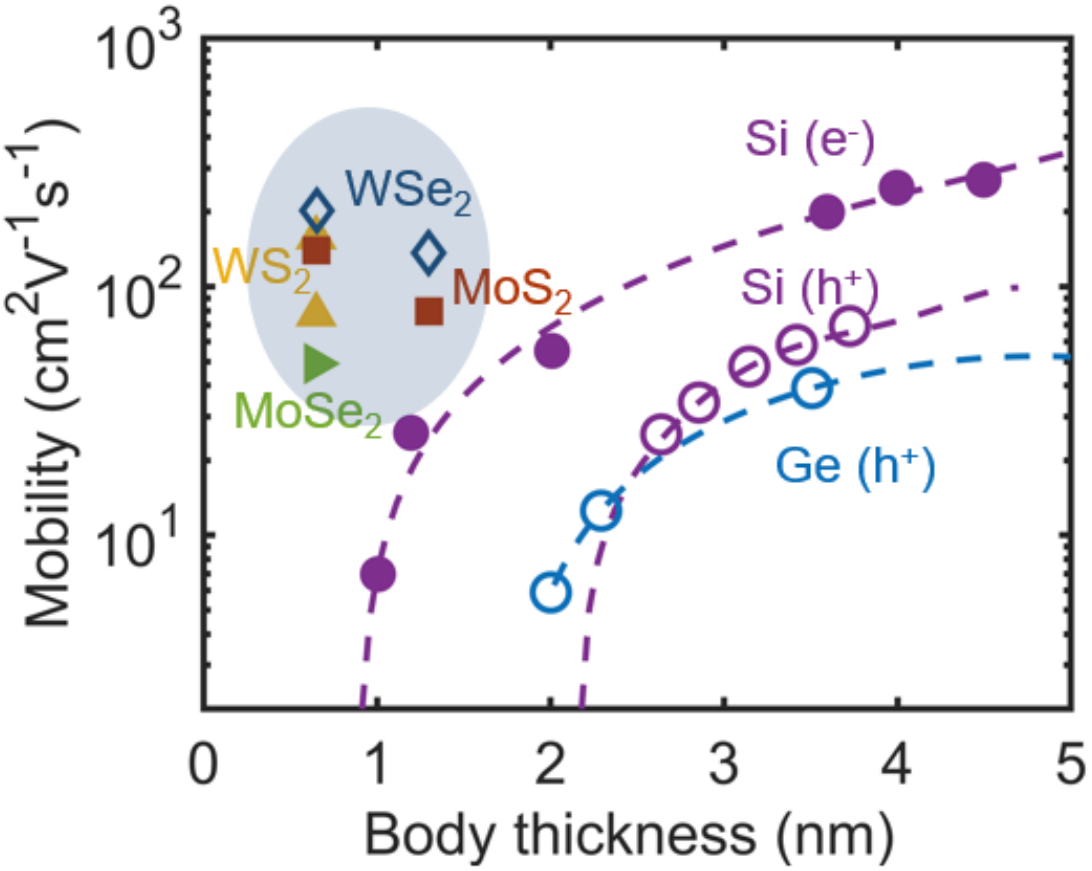
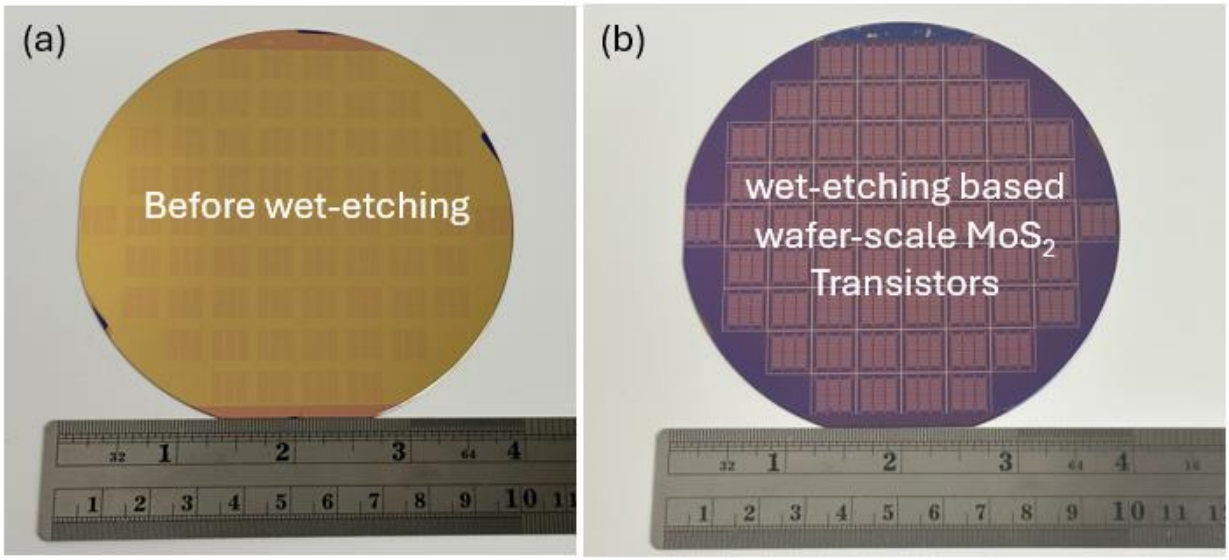
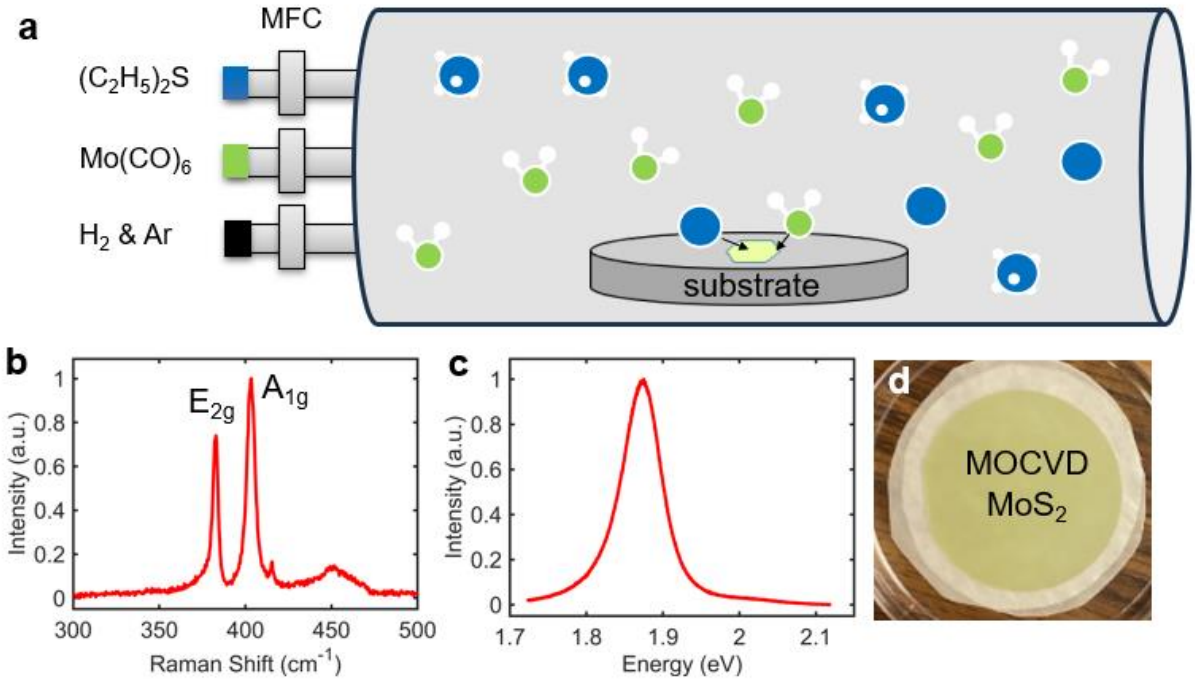


Supplementary Figure 1 Carrier mobility as a function of body thickness for various semiconductor materials. While conventional semiconductors such as silicon and germanium exhibit significant mobility degradation at reduced thickness, 2D semiconductors (e.g., MoS_2, WS_2, WSe_2 and $MoSe_2$) retain high mobility even at atomic-scale thickness, highlighting their potential for ultimate transistor scaling. Mobility data are from references[1–8].

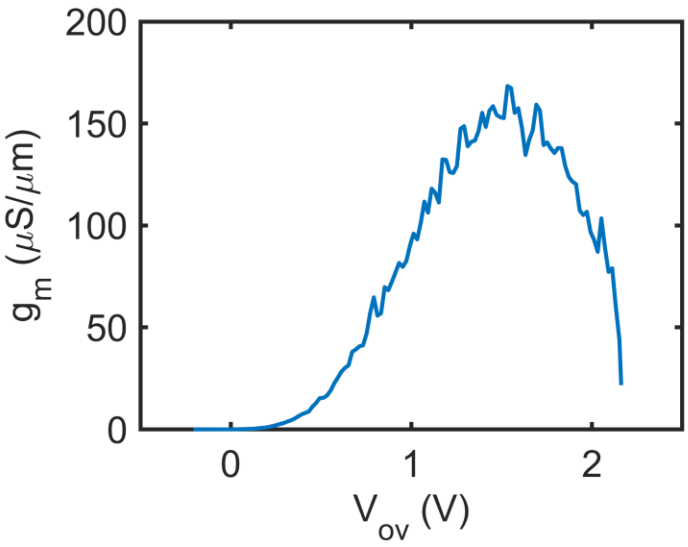
Supplementary Figure 2 Process flow for the fabrication of sub-5 nm channel arrays using a wet-etching process to remove the sacrificial oxide and metal layers. No electron-beam lithography or tape-assisted steps are required, ensuring CMOS compatibility.



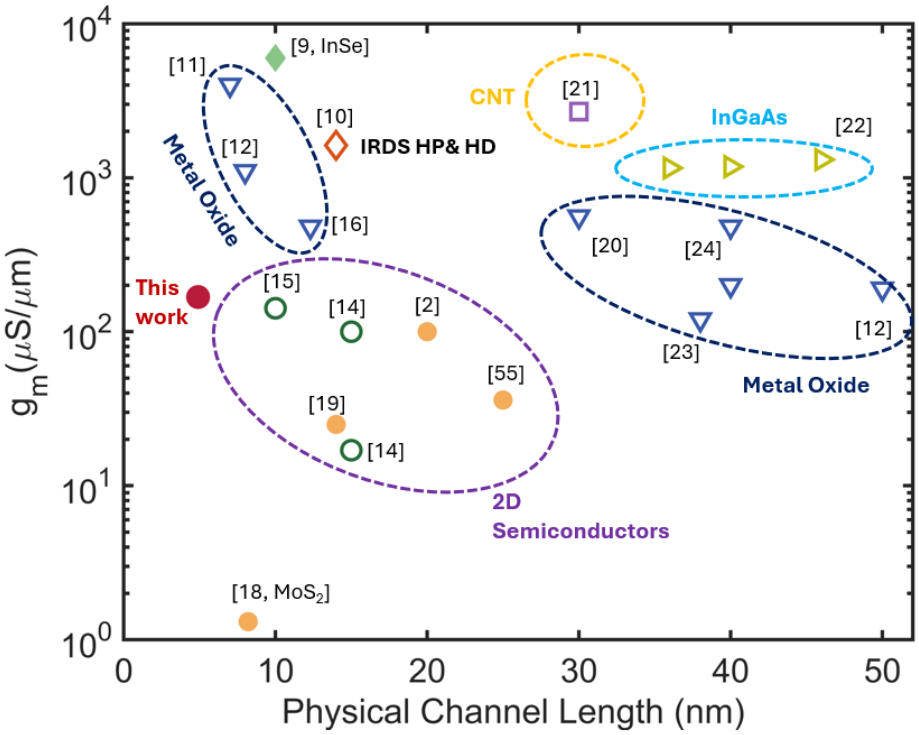
Supplementary Figure 3 Optical images of a 4-inch wafer (a) before and (b) after the CMOS-compatible wet-etch process, demonstrating wafer-scale fabrication of MoS_2 transistor arrays.



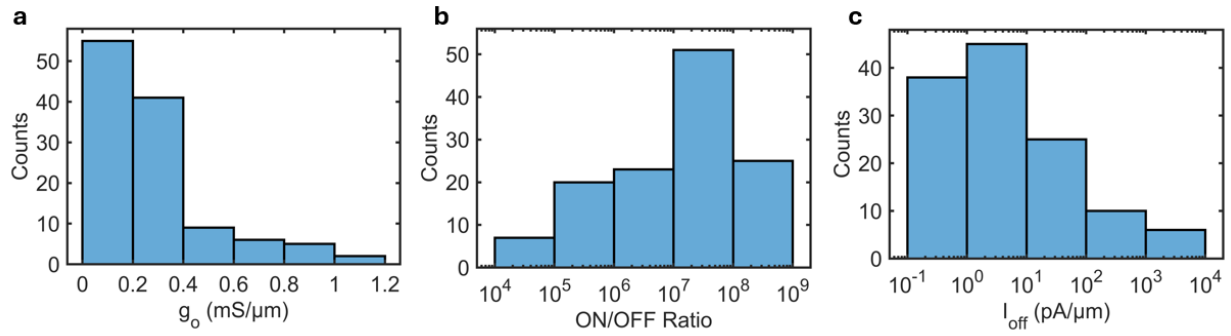
Supplementary Figure 4 MOCVD synthesis and characterization of wafer-scale monolayer MoS_2. (a) Schematic of the MOCVD synthesis setup using diethyl sulfide ($(C_2H_5)_2S$) and molybdenum hexacarbonyl ($Mo(CO)_6$) as precursors, with H_2/Ar as carrier gases. (b) Raman spectrum showing characteristic E_{2g} and A_{1g} modes of monolayer MoS_2. (c) Photoluminescence (PL) spectrum with a peak near 1.88 eV, consistent with direct bandgap emission from monolayer MoS_2. (d) Optical image of the as-synthesized wafer-scale monolayer MoS_2 film on sapphire substrate.



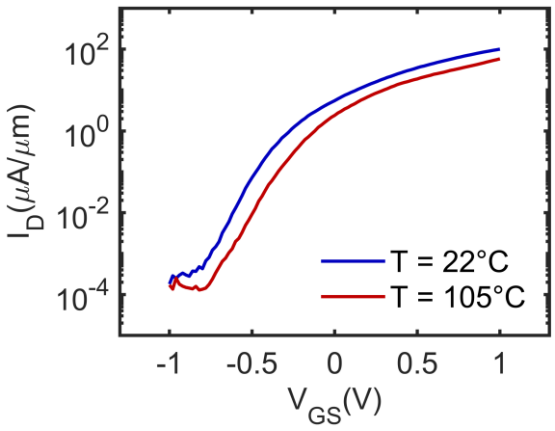
Supplementary Figure 5 Transconductance ($g_m = \partial I_D / \partial V_{GS}$) as a function of gate overdrive voltage ($V_{ov} = V_{GS} - V_{th}$) for a representative sub-5 nm MoS_2 transistor measured at $V_{DS} =$ 0.5V. The use of V_{ov}eliminates the influence of absolute threshold voltage shifts, allowing direct evaluation of the intrinsic gate-to-channel control (V_{th} = -1.1 V). The device exhibits a peak $g_m$of 168 mS/mm, demonstrating strong electrostatic coupling and high differential current drive under IRDS-consistent operating conditions.



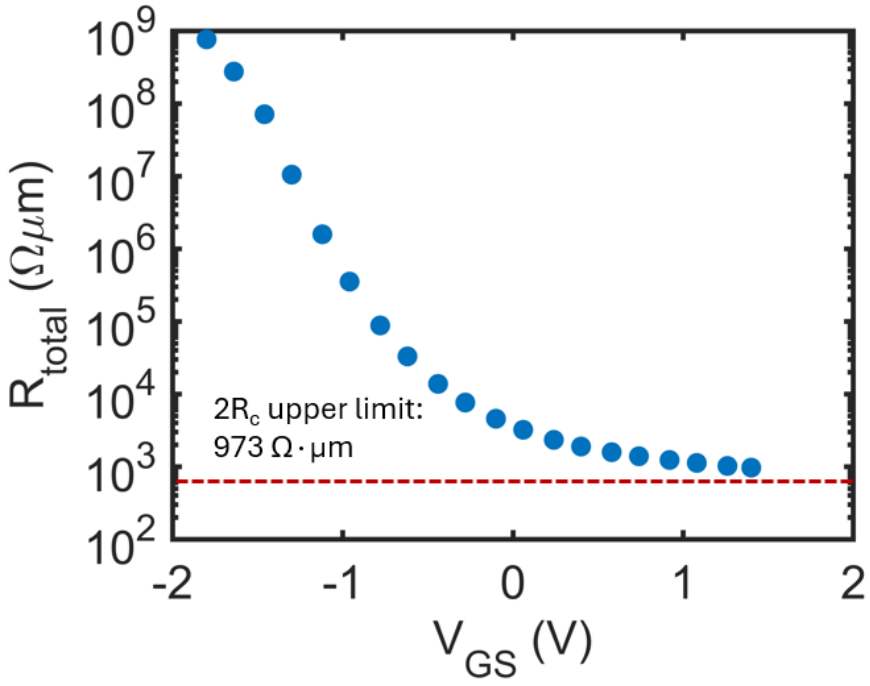
Supplementary Figure 6 Benchmarking of transconductance (g_m) *versus* physical channel length for advanced nanoscale transistors. The plot compares this work (red circle) with state-of-the-art devices based on 2D semiconductors, metal oxides(In_2O_3, IGZO), InGaAs and carbon nanotubes (CNT). The orange diamond denotes the IRDS targets. Reference: *9–24*.



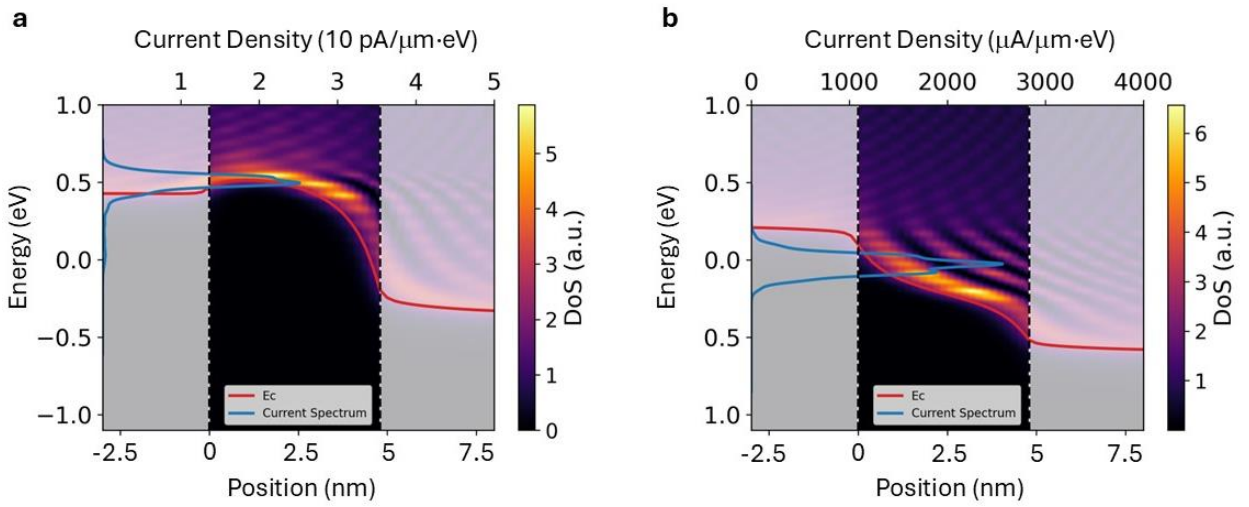
Supplementary Figure 7 Statistical distribution of key performance metrics for sub-5 nm MoS_2 MOSFETs (138 devices). Histograms of on-state conductance g_o (a), maximum current modulation ratio across full measured gate voltage range (b), and off-state leakage current I_{off} (c).



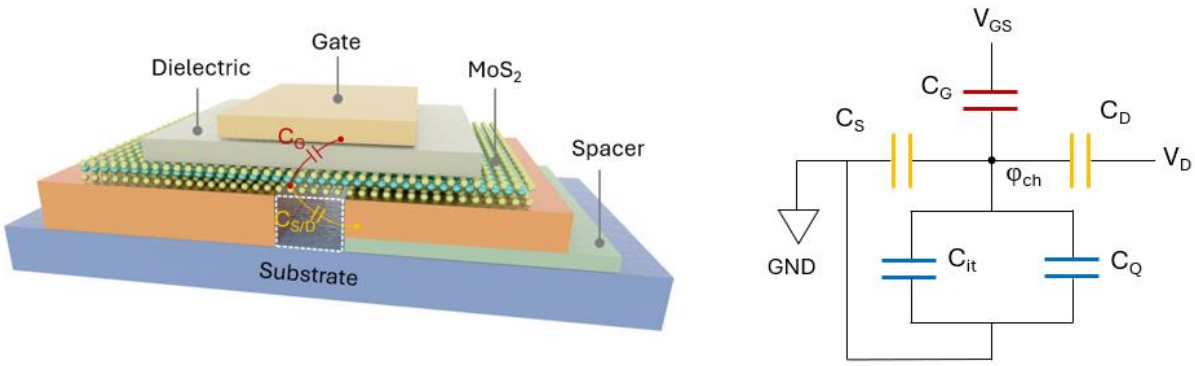
Supplementary Figure 8 Temperature-dependent transfer I-V characteristics of a representative sub-5 nm MoS_2 transistor measured at room temperature (22 °C) and at 105 °C. The device maintains stable switching behavior and similar on/off ratio across temperatures, with a positive shift in threshold voltage likely attributed to desorption of surface adsorbates.



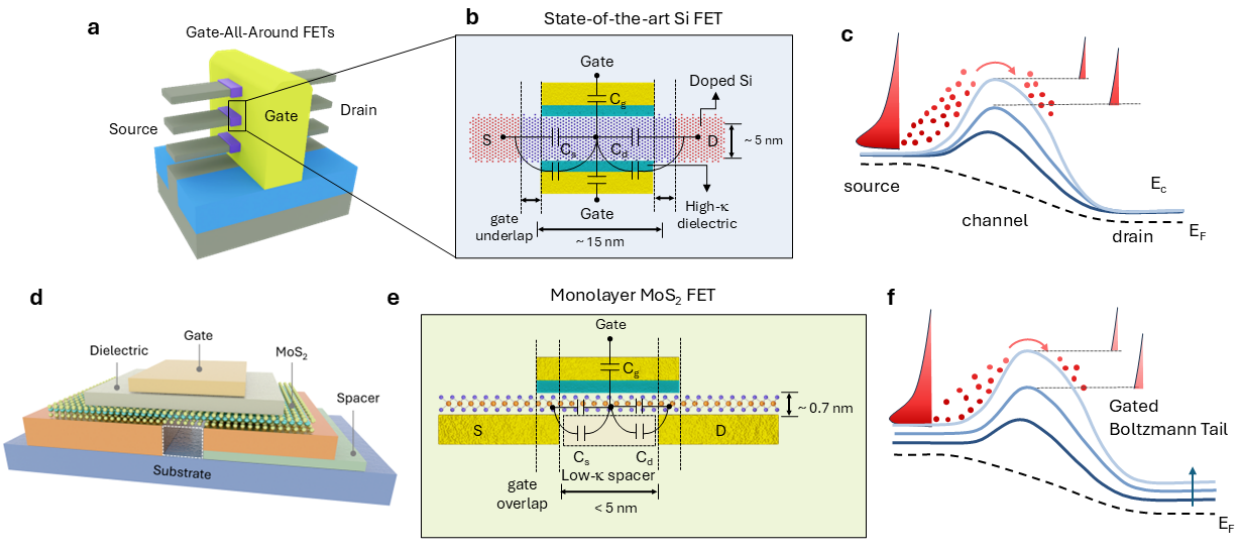
Supplementary Figure 9 Total resistance (R_{total}) as a function of gate voltage (V_{GS}) of the transistor, showing the upper bound of the $2R_c$. At high gate bias, R_{total} saturates, yielding a R_c upper limit of ~486 Ω·μm.



Supplementary Figure 10 Simulated local density of states (color map), energy resolved current spectrum (blue curve) and conduction band edge profile (red curve) under subthreshold bias condition V_{GS} = -2 V (a) and under on-state bias condition V_{GS} = -1 V (b). In the subthreshold regime, current flow is suppressed due to the high energy barrier and it is dominated by thermionic emission over the top of the barrier. In the on state, strong carrier injection is observed, consistent with the experimental data. The current spectrum reveals the spatial and energetic distribution of electron transport across the channel.



Supplementary Figure 11 Electrostatic coupling and equivalent capacitance network of our MoS_2 MOSFET. (Left) Schematic of the transistor structure. The parasitic capacitance between the source/drain and channel is minimized by the air-gap spacer, which is critical for reducing electrostatic interference and improving subthreshold behaviors. (Right) Equivalent capacitor network in the MoS_2 transistor with grounded source. C_S and C_D represent the capacitive coupling from the source and drain to the channel. C_G denotes the effective gate capacitance. The interface trap capacitance C_{it} captures the sensitivity of interface trap charge Q_{it} to changes in channel potential φ_{ch}. The quantum capacitance C_Q reflects the change in carrier density $Q_{carrier}$ with respect to the channel potential φ_{ch}, expressed as $C_Q = dQ_{carrier}/d\varphi_{ch}$. In the subthreshold regime, C_Q is usually negligible compared with the other capacitance terms.



Supplementary Figure 12 Comparison of electrostatic design in state-of-the-art silicon GAAFETs and monolayer MoS_2 MOSFETs. (a) Schematic of GAAFET device structure. (b) Zoom-in view of state-of-the-art GAAFET device, featured by channel length of ~ 15 nm and a body thickness of ~ 5 nm and gate underlap regions. (c) Illustration of the origin of subthreshold leakage current in silicon GAAFETs. The Fermi level in the contacts is essentially fixed. (d) Device structure of our monolayer MoS_2 MOSFET. (e) Side view of the sub-5 nm channel MoS_2 transistor with air gap design. It adopts a channel-on-top architecture with a physical thickness of ~ 0.7 nm and gate-contact overlap, enabling direct electrostatic modulation of both the channel barrier and adjacent contact regions. (f) Due to the low density of states in the MoS_2 contact regions, the gate-contact overlap design allows the gate field to modulate not only the channel potential but also the local Fermi level within the adjacent MoS_2 contact regions.

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