

Wafer-Scale 2D MoS₂ Transistors with Sub-5 nm Channel Length and Subthreshold Performance Beyond the Silicon Limit

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This manuscript has been previously reviewed at another journal. This document only contains information relating to versions considered at Nature Communications.

This file contains all reviewer reports in order by version, followed by all author rebuttals in order by version.

Version 0:

Reviewer comments:

Reviewer #3

(Remarks to the Author)

I have carefully considered the revised manuscript and the authors' responses. Although additional data have been provided, I do not believe that the main concerns have been adequately addressed, and in my view the manuscript is not suitable for publication in Nature Communications.

First, the authors continue to downplay the strongly negative threshold voltage. This is not a secondary issue, especially when the work is presented as relevant for wafer-scale and low-power logic applications. Attributing the shift to adsorbates does not solve the problem; it instead highlights limited control and possible instability.

Second, mobility remains unmeasured in the actual MOCVD-grown and processed MoS₂. This is critical because the claimed 85% ballisticity relies on transport parameters that are not experimentally established. In particular, the use of a phonon-limited mobility of about 400 cm²/Vs is unreasonable for the material used here, since it represents the upper limit due to only electron-phonon interactions.

Using the authors' own estimate, a mobility of 100 cm²/Vs would lead indeed to a β close to 0.58. Thus, a more realistic mobility gives a ballisticity close to 55-60%, rather than 85%. The reported value is therefore strongly model-dependent and not convincingly demonstrated.

For these reasons, I do not recommend acceptance in Nature Communications. The manuscript may be more appropriate for a specialized device or nanotechnology journal, provided that the claims on technological relevance and ballistic transport are substantially moderated.

Reviewer #4

(Remarks to the Author)

In my view, the authors have thoroughly and rigorously addressed all the technical criticisms raised by Referee #1. The revised work now presents a more complete and robust case that monolayer MoS₂ transistors can achieve subthreshold performance beyond the theoretical limit of silicon at deeply scaled dimensions.

However, I have two minor queries. First, the authors claim an on/off current ratio of 10⁸, but this appears to be an overestimation, as the off state current seems to have been taken as the minimum measured value rather than a well defined bias dependent level, which is not rigorous. Second, the authors should specify the thickness of the evaporated Al layer and the resulting aluminium oxide gate dielectric, as these are key parameters for short channel devices.

Overall, I recommend acceptance of this manuscript for publication in Nature Communications.

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Response Letter for

Wafer-Scale 2D MoS₂ Transistors with Sub-5 nm Channel Length and Subthreshold Performance Beyond the Silicon Limit

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Dear Editor,

We sincerely thank the Editor and the Reviewers for the careful assessment of our manuscript “Wafer-Scale 2D MoS₂ Transistors with Sub-5 nm Channel Length and Subthreshold Performance Beyond the Silicon Limit” (NCOMMS-26-051318-T) and for the constructive comments. We have revised the manuscript in response to the remaining concerns. Below, we provide a detailed point-by-point response to each comment.

Referee #3's Comments:

COMMENT 3-1 First, the authors continue to downplay the strongly negative threshold voltage. This is not a secondary issue, especially when the work is presented as relevant for wafer-scale

and low-power logic applications. Attributing the shift to adsorbates does not solve the problem; it instead highlights limited control and possible instability.

Response

Thank you for the comment. In the revised manuscript, we now explicitly acknowledge that the negative threshold voltage leads to depletion-mode operation and would need to be addressed before the present devices could be implemented in industry-level integrated circuits. We have removed the previous attribution of the threshold-voltage shift primarily to adsorbates. Instead, we discuss multiple possible contributions, including unintentional n-type doping associated with sulfur-vacancy-induced donor states, fixed charges and interfacial states in the dielectric stack, and process- or environment-induced charge transfer. We agree that identifying the dominant mechanism and evaluating its stability will require dedicated studies beyond the scope of the present work.

To address the Reviewer's concern constructively, we have also added a discussion of potential strategies for shifting the threshold voltage toward positive values. These include oxygen-mediated passivation of sulfur-vacancy-related donor states and the integration of van der Waals dielectric stacks for improved interface quality and threshold voltage control. Oxygen passivation has been shown to suppress donor states and reduce unintentional n-type doping in monolayer MoS₂¹, while van der Waals dielectrics can enable programmable threshold voltage tuning and reduce static power consumption in 2D logic circuits².

The following discussion has been added to the revised manuscript:

“We note that the present devices exhibit a negative threshold voltage V_{th} and therefore operate in depletion mode (Figure 3d). Although this does not affect the extraction of the subthreshold swing, a negative V_{th} is undesirable for low-power logic IC because the transistor remains partially conducting at $V_{GS} = 0$ V, which can increase standby leakage and static power consumption. Such threshold voltage shifts in MoS₂ transistors have been associated with a combination of fixed dielectric charge, interface traps, surface adsorbates, processing residues, and defect-induced n-type doping, including sulfur vacancies^{1–3}. Future optimization will require deliberate threshold-voltage engineering to shift V_{th} towards positive. One possible route is defect healing through oxygen-mediated passivation of sulfur-vacancy-induced donor states, which can reduce

unintentional n-type doping and shift MoS₂ transistors toward enhancement-mode operation without measurable mobility degradation¹. Recent studies also demonstrated positive threshold voltage tuning in MoS₂ transistors using van der Waals dielectric encapsulation and gate stacks².”

Nevertheless, we respectfully disagree with the Reviewer’s conclusion that the negative threshold voltage renders the present work unsuitable for publication. Threshold voltage engineering is important for practical circuit implementation, but it is distinct from the central scientific question addressed here: whether MoS₂ transistors with sub-5 nm physical channels can retain strong electrostatic control and favorable subthreshold behavior. The negative V_{th} does not invalidate the measured subthreshold swing, the physical channel length scaling, or the experimentally observed suppression of short channel effects. Moreover, the present manuscript does not claim that the devices are immediately ready for industrial logic integration. Rather, it establishes the device architecture and electrostatic design principles required for continued scaling, while explicitly identifying threshold voltage control as an important target for future optimization.

Bringing 2D semiconductors to industrial very-large-scale integrated circuits (VLSI) will require progress across multiple, largely distinct challenges, including high on-state current, low subthreshold swing, low-resistance Ohmic contacts, dielectric and interface control, device uniformity, reliability, and threshold voltage engineering. It would be unreasonable to require a single study to resolve all of these challenges simultaneously. The relevant question is whether the threshold voltage issue undermines the principal claims of the present work; in our view, it does not. Negative V_{th} and depletion-mode operation also remain common in n-type MoS₂ transistors and are actively treated as separate device engineering problems. For example, a recent wafer-scale study demonstrated self-aligned MoS₂ transistors and integrated logic circuits using a depletion-mode (negative V_{th}) load transistor⁴, illustrating that meaningful advances in scaling and integration can be established even while threshold voltage is negative. Applying the reviewer’s criterion consistently would imply that much of the published literature on 2D transistors should not have been published because many reported devices exhibit negative threshold voltages. We respectfully disagree with such a standard. An unresolved threshold voltage issue should be clearly acknowledged and addressed, but it does not invalidate independent and experimentally supported advances in channel scaling and subthreshold electrostatics.

COMMENT 3-2 Second, mobility remains unmeasured in the actual MOCVD-grown and processed MoS₂. This is critical because the claimed 85% ballisticsity relies on transport parameters that are not experimentally established. In particular, the use of a phonon-limited mobility of about 400 cm²/Vs is unreasonable for the material used here, since it represents the upper limit due to only electron-phonon interactions. Using the authors' own estimate, a mobility of 100 cm²/Vs would lead indeed to a B close to 0.58. Thus, a more realistic mobility gives a ballisticsity close to 55-60%, rather than 85%. The reported value is therefore strongly model-dependent and not convincingly demonstrated.

Response

Thank you for the comment. To eliminate the concern regarding the ballisticsity analysis and to make the manuscript more focused, we have removed the entire ballisticsity analysis from the revised manuscript. This includes the reported ballisticsity ratio, the ballistic Virtual Source model, the associated Methods section and Supplementary Figures, and all statements describing the devices as ballistic or quasi-ballistic. The revised manuscript now focuses exclusively on the experimentally established physical channel length, subthreshold swing, drain-current characteristics, leakage behavior, and the electrostatic effects of the dielectric environment and gate-contact overlap.

For completeness, however, we respectfully disagree with the specific technical basis of the Reviewer's criticism. The Reviewer argues that different assumed mobility values would lead to substantially different extracted ballisticsity ratios. This reflects a misunderstanding of the analysis used in our manuscript. The reported ballisticsity ratio was not extracted from a mobility-dependent estimate of the mean free path. Instead, the measured IV characteristics were fitted using the Virtual Source model to extract the carrier injection velocity at the top of the source-channel barrier, which was then compared with the corresponding theoretical ballistic injection velocity. This methodology was clearly described in the original Methods section. The mobility-based analysis shown in the original Extended Data Figure 5 was intended only as a first-order, order of magnitude estimate and it was not how the reported ballisticsity was obtained. Therefore, substituting mobility values of 400 or 100 cm²/Vs does not constitute a recalculation within the model used to obtain the reported ballisticsity.

Conventional mobility is a concept most applicable to the diffusive, low-field transport regime. When the channel length approaches the carrier mean free path, carriers no longer establish local diffusive transport within the channel^{5,6}, and mobility consequently loses its physical relevance and meaning as a descriptor of the terminal current. In this ultrascaled regime, transport is more appropriately described in terms of the carrier charge and injection velocity at the top of the source-channel barrier⁷. Moreover, extracting a meaningful channel mobility from the present device would be strongly complicated by contact resistance, nonuniform lateral fields, and the absence of a sufficiently long diffusive channel. The Virtual Source or top-of-the-barrier framework used in our original analysis is a widely adopted approach for evaluating quasi-ballistic transport in deeply scaled silicon and emerging-semiconductor transistors⁷⁻⁹.

Rather than further debating a specific numerical ballisticity value, we have therefore removed the ballisticity analysis entirely from the revised manuscript. Importantly, this revision does not affect the principal conclusions regarding the measured sub-5 nm physical channel length and subthreshold performance.

Reviewer #4

In my view, the authors have thoroughly and rigorously addressed all the technical criticisms raised by Referee #1. The revised work now presents a more complete and robust case that monolayer MoS₂ transistors can achieve subthreshold performance beyond the theoretical limit of silicon at deeply scaled dimensions.

COMMENT 4-1 First, the authors claim an on/off current ratio of 10^8 , but this appears to be an overestimation, as the off state current seems to have been taken as the minimum measured value rather than a well defined bias dependent level, which is not rigorous.

Response

Thank you for this comment and for the positive assessment of our manuscript. We agree that an on/off current ratio should be evaluated using explicitly defined bias conditions rather than solely from the maximum and minimum currents measured over the full gate-voltage sweep.

Accordingly, we have revised the manuscript to distinguish between the current ratio evaluated at fixed gate biases and the maximum current modulation over the measured gate-voltage range. At $V_{DS} = 0.5$ V, the current ratio evaluated between $V_{GS} = -1$ V and $V_{GS} = 1$ V was approximately 1.1×10^6 . This fixed-bias current ratio is now the value reported in the Abstract and emphasized in the Main Text. The previously reported value of approximately 10^8 is no longer presented as an on/off current ratio and is described only as the maximum current modulation over the full measured gate-voltage range.

The revised text reads:

“At $V_{DS} = 0.5$ V, the current ratio evaluated between $V_{GS} = -1$ V and $V_{GS} = 1$ V was approximately 1.1×10^6 .”

To avoid potentially misleading cross-literature comparisons based on inconsistent bias windows and extraction methods, we have also removed the on/off current ratio benchmarking panel from Figure 4. These revisions have been applied consistently throughout the Main Text, figure captions, and Supplementary Information.

COMMENT 4-2 Second, the authors should specify the thickness of the evaporated Al layer and the resulting aluminium oxide gate dielectric, as these are key parameters for short channel devices.

Overall, I recommend acceptance of this manuscript for publication in Nature Communications.

Response

Thank you for this comment. We agree that the Al deposition and resulting AlO_x thickness are important parameters for these short-channel devices. We have added the detailed fabrication process parameters and dielectric thickness to the Methods section.

The revised Methods text reads:

“The AlO_x gate dielectric was formed through three sequential Al deposition and natural oxidation cycles. Al layers with nominal thicknesses of 1.5, 1.5, and 1.0 nm were successively deposited by electron-beam evaporation, with each layer allowed to oxidize under ambient conditions overnight

before the subsequent deposition. The resulting AlO_x dielectric thickness was approximately 5.5 nm.”

We appreciate the Reviewer’s positive evaluation and recommendation for publication.

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