
Single-crystalline CoSi semimetals with high conductivity and reliability

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Supplementary Information

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References

Supplementary Note 1

Features of CoSi for highly conductive interconnect

When the thickness of conventional metals scales below the electron mean free path, its resistivity greatly increases. The resistivity increase is a result from increased electron scattering at the surfaces and grain boundaries. In addition, impurities and scattering in conventional metal can affect the motion of electrons due to strong momentum loss in the scattering. In the 7-nm technology node of integrated circuits, the resulting higher resistivity of interconnects contributes to over 50% of the total signal delay (**Supplementary Fig. 1**).

We have calculated the band structure along the Brillouin zone path following the theoretical investigation¹. Different from conventional metals, semimetal CoSi has a unique band structure (**Supplementary Fig. 2**) and transport behavior. CoSi hosts spin-1 excitation with Chern number +2 at Γ and the double Weyl fermion with the Chern number -2 at R^2 .

Our calculation results reveal that in a small CoSi supercell of 8 u.c ($a=b=c=4.445$ Å in one u.c.), there are strong surface states contribution and weak bulk states contribution (**Supplementary Fig. 3a** and **Supplementary Fig. 3b**), especially near the Fermi level. Theoretical calculation work³ reveal the thickness-dependent surface/bulk to total charge current fraction ratio (**Supplementary Fig. 3c**). This thickness-dependent trend clearly shows that as the thickness gradually reduces, the surface to bulk charge current ratio increases, revealing the intrinsic feature of the highly conductive surface path of CoSi. As the electrons can move quickly through the Fermi arc surface states with minimal scattering, the conductivity contribution of surface states is dominated when the thickness of CoSi scales down, which results in increased conductivity with decreased thickness. Hence, topological semimetal CoSi with surface states and Fermi arcs can break this trade-off, showing ultrahigh conductivity at room temperature.

Supplementary Note 2

Materials growth and characterization of CoSi nanoflakes

We used the confined flux-assisted growth setup (**Supplementary Fig. 4**) to synthesize CoSi nanoflakes over a wide temperature range of 770 to 920 °C. We employ a rapid thermal profile (**Supplementary Fig. 5**) featuring a controlled heating ramp and an optimized holding time of 6 minutes. This rapid process, culminating in the complete evaporation of the Te flux, kinetically terminates the growth. The flux-assisted confined method enables the growth of nanoflake samples with a high degree of tolerance for growth parameters⁴.

While the CoSi phase can form over a wide temperature range, systematic optimization reveals that the resulting morphology and thickness are highly sensitive to the growth parameters. To identify the optimal window for sub-100 nm nanoflakes, we investigated the influence of growth temperature and precursor-to-flux mass ratio.

The growth temperature primarily dictates the evaporation kinetics of the Te solvent (**Supplementary Fig. 6**). At a low temperature of 770 °C, the vapor pressure of Te is insufficient for effective volatilization, leaving the CoSi nucleation sites entirely encapsulated within the residual flux. As the temperature reaches 800 °C to 830 °C, the progressive removal of Te begins to yield discrete, individual nanoflakes. The optimal growth window is achieved at 860-890 °C, where the complete volatilization of the solvent ensures the isolation of pristine, well-defined, and ultrathin nanoflakes. However, further increasing growth temperature to 920 °C accelerates the vertical mass transport, which inevitably leads to noticeably thicker nanoflakes.

In addition, the precursor-to-flux mass ratio serves as a critical liquid medium for mass transport (**Supplementary Fig. 7**). At lower mass ratios (1:2-1:4), the limited solvent volume fails to establish a continuous transport phase, resulting in fragmented clusters accompanied by unreacted precursors. The optimal growth window is identified between 1:6 and 1:8, where the appropriate flux concentration enables the robust growth of high-quality 2D nanoflakes. While further increasing the Te content (e.g., 1:12) can still yield thin flakes, the excessive solvent severely dilutes the precursor concentration. This over-dilution compromises the stable 2D growth kinetics, leading to sparse nucleation and a significant reduction in the overall

integrity of the samples.

As summarized in **Supplementary Fig. 8** and **Fig. 9**, the statistical results reveal an exceptionally narrow compositional distribution. The average atomic ratio of Co:Si is approximately 49.9:50.1. This result provides robust evidence that the bulk stoichiometry is tightly centered on the 1:1 ratio.

Supplementary Note 3

Transport behaviors of CoSi nanoflakes

The pronounced trend of resistivity scaling is a result of the dominant contribution from surface conduction. To quantify the contributions of bulk and surface carriers in the topological semimetal, we performed Hall effect measurements under a magnetic field up to 6 T. We experimentally measured Hall resistance and acquire thickness-dependent Hall coefficient (R_H). Then, we calculated the total Hall resistivity (ρ_{xy}^T) and Hall conductivity (σ_{xy}^T) of CoSi nanoflake with different thicknesses, respectively. The σ_{xy}^T consists of bulk and surface contribution², which can be described by Equation (1):

$$\sigma_{xy}^T = \sigma_{xy}^B + \sigma_{xy}^S = \sigma_{xy}^B + G_{xy}^S/t \quad (1)$$

where σ_{xy}^T consists of the bulk Hall conductivity (σ_{xy}^B) and the surface Hall conductivity (σ_{xy}^S). Furthermore, $\sigma_{xy}^S = G_{xy}^S/t$, where G_{xy}^S is the surface sheet Hall conductance, and t is the sample thickness, respectively. We can extract: $\sigma_{xy}^B = -17.1 \mu\Omega^{-1}\text{m}^{-1}\text{T}$ and $G_{xy}^S = -4.8 \Omega^{-1}\text{T}$. According to equations $R_H=1/(G_{xy}B)$ and $n=1/(R_{HE})$, we can acquire the thickness-dependent surface carrier density (n_{2D}^S) and bulk carrier density (n_{2D}^B). Following the fundamental conductivity relationship $\sigma = n \mu e$ (where σ denotes electrical conductivity, n represents carrier density, μ is charge carrier mobility, and e stands for elementary charge), we quantitatively analyzed the thickness-dependent carrier mobilities for both surface and bulk transport pathways.

The total conductivity is treated as the parallel combination of surface and bulk conductivities: $\sigma_{total} = \sigma_b + \sigma_s$, where σ_{total} is the total conductivity, σ_b is the bulk conductivity, and σ_s is the surface conductivity. Therefore, $\sigma_{total} = \sigma_b + \sigma_s = (G_b + G_s)/t$ where $G_b = n_b \mu_b e t$, $G_s = n_s \mu_s e$. Consequently, $\sigma_{total} = n_b \mu_b e + n_s \mu_s e/t$.

We have determined all four fundamental quantities by fitting the experiment results:

$$n_b = 1.07 \times 10^{20} \text{ cm}^{-3}, \quad \mu_b = 704 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}, \quad n_s = 2.9 \times 10^{15} \text{ cm}^{-2}, \quad \mu_s = 1.51 \times 10^4 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}.$$

We further carried out calculations based on this formula and compared them against experimental data from both as-grown nanoflakes and bulk samples. Our experimental results are in agreement with the simulation results (**Supplementary Fig. 19**).

Comparison between nanoflakes and nanowires

The resistivity of our CoSi nanoflake crystal is much lower than that of the reported nanowires^{5,6}. This observation aligns with the findings in topological semimetal TaAs, where TaAs nanowires exhibit resistivity 1000 times higher than their nanoflake counterparts with similar dimensions⁷. In contrast, the surface transport property in nanoflakes remains relatively unaffected by the geometric confinement along the z-direction. The elevated resistivity in nanowires is attributed to: (i) a high density of surface defects introduced during synthesis, or (ii) enhanced boundary scattering from in-plane confinement effects.

Supplementary Note 4

Working frequency benchmark for interconnects with different resistivities

There is about 40% increase (**Supplementary Fig. 23a**) of relative maximum frequency ($F_{\max}$) as the resistivity is reduced to $1 \mu\Omega \text{ cm}$ for the circuit of 700 W in the 5-nm-technology node¹. For comparison, we calculated the relative $F_{\max}$ for Bi, Pt, Ru, Co, W, and CoSi, normalizing to Cu ($F_{\max} = 1$). $F_{\max}$, representing the reciprocal of delay, was computed using the Elmore delay model. This model is extensively employed in estimating interconnect delays within VLSI design. This model provides a simplistic delay analysis that avoids time-consuming numerical integration/differential equations of a Resistance-Capacitance network. Top panel of **Supplementary Fig. 23b** shows the simplified lumped-element model for predicting the impact of wire geometry on circuit delay, as expressed as the Equation (2)⁸:

$$\text{Delay} = 0.69R_{\text{Drive}}C_{\text{Load}} + 0.69R_{\text{Drive}}C_W + 0.69R_W C_{\text{Load}} + 0.38R_W C_W \quad (2)$$

where R_{Drive} is drive resistance that refers to the resistance offered by a circuit or component when it is driving a signal to the next stage; C_{Load} , load capacitance, is the total capacitance that a circuit or component must drive, R_W and C_W are the wire resistance and capacitance for the considered interconnect length, respectively. The wire resistance R_W is calculated with the following Equation (3):

$$R = \rho \frac{L}{A} \quad (3)$$

where ρ denotes to the resistivity, A refers to the cross-sectional area, and the L represents the length of the interconnect. The capacitance C_W is calculated with the following Equation (4):

$$C = \frac{\varepsilon_0 \varepsilon_r A}{L} \quad (4)$$

where ε_0 is the vacuum permittivity (8.85×10^{-12}), ε_r is the dielectric constant of silicon oxide which is 3.9, A refers to the cross-section area, and L represents the length of the oxide. The length of oxide between two contact or via is equals to the length of the interconnection.

The relative $F_{\max}$ is calculated with the $F_{\max}$ of copper as baseline, which could be calculated by the following Equation (5):

$$F_{max} = 1 + \frac{\left(\frac{1}{Delay} - \frac{1}{Delay_{Cu}}\right)}{\left(\frac{1}{delay_{Cu}}\right)} \quad (5)$$

We calibrated the model by adjusting the R_{Drive} and C_{Load} to match the experimental result from this work¹. The calculation of relative F_{max} for Bi, Pt, Ru, Co, W, and CoSi are shown in the bottom panel of **Supplementary Fig. 23b**, with all simulation parameters for frequency normalization detailed in **Supplementary Table S3**.

Supplementary Note 5

High-frequency transmission of CoSi interconnect

As the testing frequency is not higher than 40 GHz, we adopted Equation (6) in the de-embedding process with tested scattering parameters:

$$Y_{DUT} = Y_{Total} - Y_{Open} \quad (6)$$

Then, we can acquire the S_{21} of thru and CoSi interconnect with de-embedding in **Supplementary Fig. 26**, respectively. Both thru and CoSi interconnect show the decreasing S_{11} from about -20 dB to -10 dB, while the S_{21} gradually increases to about -2 dB as the frequency increase from 1 to 40 GHz.

The interconnection transmission can be described by a transmission line model consisting of a conductor and a dielectric layer (SiO_2). R represents the series resistance, L represents the series inductance, G represents the shunt conductance (the dielectric loss between CoSi and SiO_2), and C represents the shunt capacitance. These distributed parameters and impedance can be extracted from S-parameter measurements. Wave equations for this equivalent circuit model yield the propagation constant γ and impedance Z as a function of frequency.

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \quad (7)$$

$$Z = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (8)$$

The S-parameters for a two-port network can be converted to ABCD parameters to obtain the propagation constant γ and impedance Z .

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \frac{1}{2S_{21}} \times \begin{bmatrix} (1 + S_{11} - S_{22} - \Delta S) & Z_0(1 + S_{11} + S_{22} + \Delta S) \\ (1/Z_0)(1 - S_{11} - S_{22} + \Delta S) & (1 - S_{11} + S_{22} - \Delta S) \end{bmatrix}, \quad (9)$$

where $\Delta S = S_{11}S_{22} - S_{21}S_{12}$, and Z_0 denotes the controlled impedance in an RF measurement system (50 Ω). γ and Z are extracted by using the ABCD parameter matrix as follows:

$$\gamma = \cosh^{-1} A \quad (10)$$

$$Z = \sqrt{B/C} \quad (11)$$

Transmission parameters such as R , L , G , and C can be obtained by Equation (12):

$$R = \text{Re}\{\gamma Z\}$$

$$L = \text{Im}\{\gamma Z\}/\omega$$

$$G = \text{Re}\{\gamma/Z\}$$

$$C = \text{Im}\{\gamma/Z\}/\omega \quad (12)$$

The relationship between the propagation constant $\gamma = \sqrt{(R + j\omega L)(G + j\omega C)}$ and impedance $Z = \sqrt{(R + j\omega L)/(G + j\omega C)}$ was used to obtain the individual transmission parameters of R , L , G , and C .

The “thru” device has a width of 20 μm , whereas our CoSi interconnect device measures merely 4.5 μm in width, constituting less than one-quarter of the “thru” device’s width. Despite this significant size variance, the S_{21} curve of the CoSi interconnect remarkably mirrors that of the “thru” device. The characteristic propagation constant and impedance of CoSi transmission line were acquired directly from the measured scattering parameters. We can further extract the resistance (R) and normalized resistance (R per width) of CoSi and thru devices. Both devices show the increasing R as the frequency range from 0 to 40 GHz. The normalized R shows that CoSi interconnect shows lower resistance than thru structure. On the whole, the R of CoSi and thru devices slight increase as the frequency increase from 0 to 40 GHz (Supplementary Fig. 27).

Supplementary Note 6

On-chip integration of CoSi interconnect with a ring oscillator

Oscillation frequency f of the ring oscillator circuit is determined by the total delay time of the signal traveling through all the inverters in the loop, which is expressed by Equation (13):

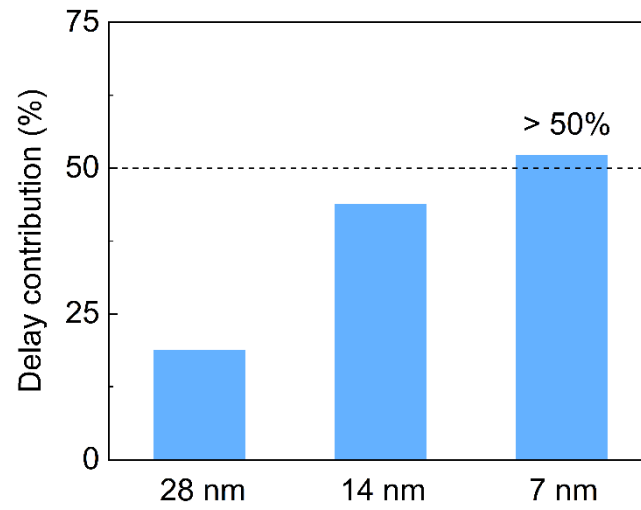
$$f = \frac{1}{2NT} \quad (13)$$

where N is the number of stages in the ring oscillator and T is the delay time for each stage, which is determined by the RC delay of inverter. Thus, the oscillation frequency f is expressed by Equation (14):

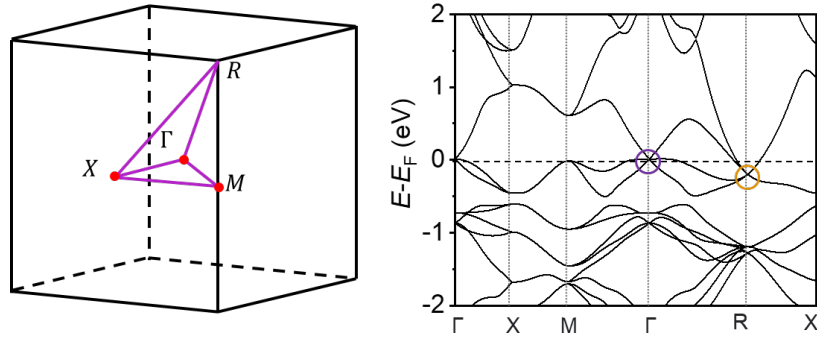
$$f = \frac{1}{2NRC} \quad (14)$$

where R and C refer to equal resistance and capacitance of the interconnect.

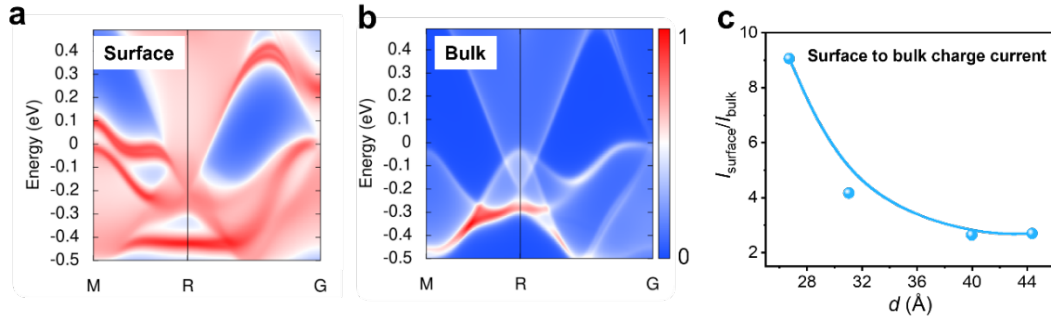
As shown in Fig. 4f, the change of f is negligible after embedding our CoSi interconnect, reflecting the high conductivity of the material and its suitability for interconnect applications.



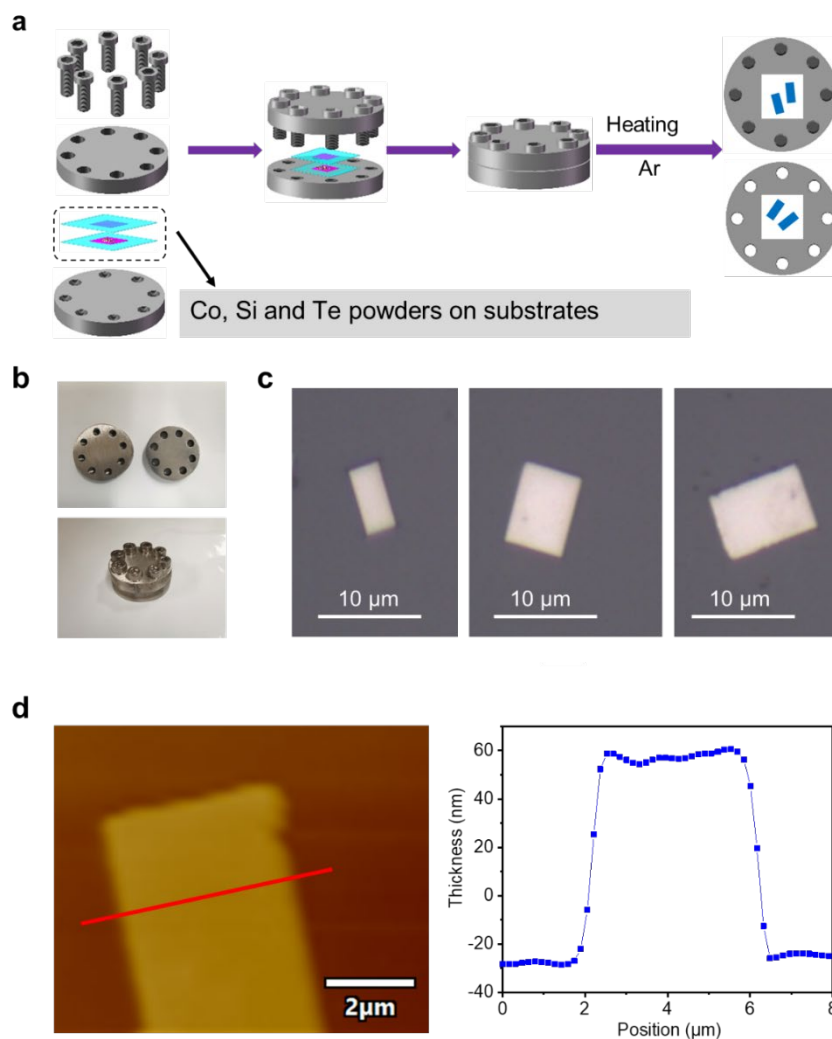
Supplementary Figure 1. The signal delay contribution ratio from the Cu interconnect⁹.



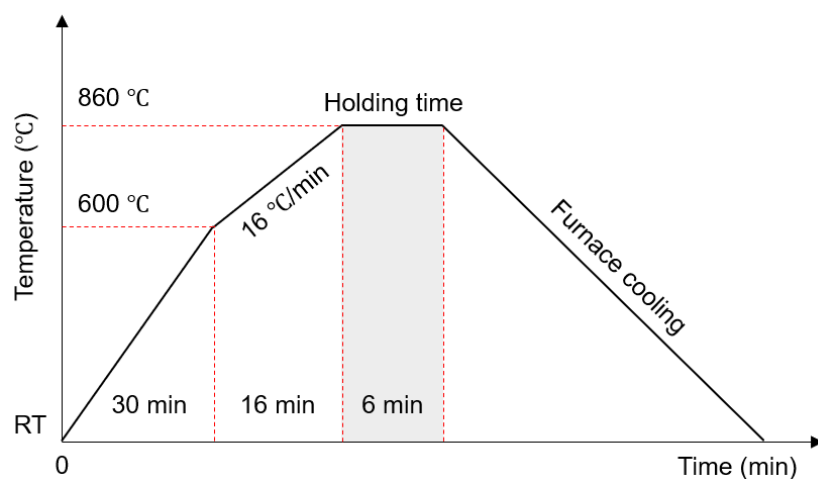
Supplementary Figure 2. Band structure and topological Fermions of CoSi. Purple and orange circles mark the topological Fermions in the band structure along the corresponding Brillouin zone path.



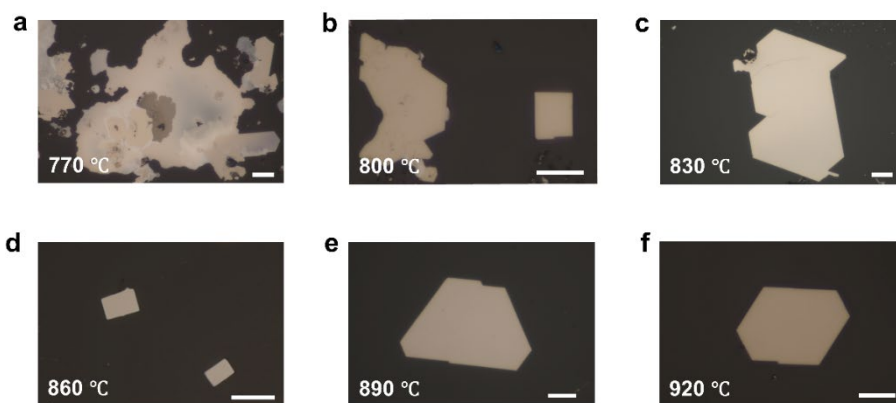
Supplementary Figure 3. Surface and bulk states contribution of thin CoSi. **a**, Surface states contribution to the band structure along M-R-G based on a small CoSi supercell (8.u.c). **b**, Bulk states contribution to the band structure along M-R-G on a small CoSi supercell (8.u.c). **c**, Thickness-dependent surface to bulk charge current. The calculation is based on the surface/bulk to total charge current fraction ratio, as derived from theoretical work³.



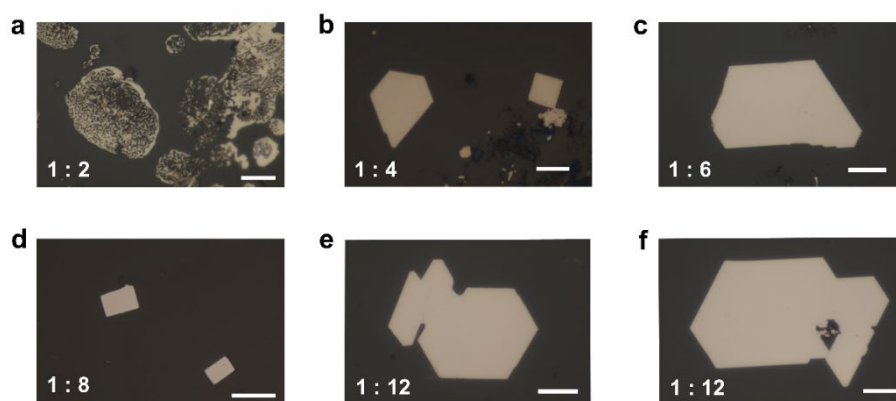
Supplementary Figure 4. Flux-assisted growth setup for synthesizing CoSi nanoflakes. a, Schematic of using the confined setup, mixed Co/Si powders and flux material for growing CoSi samples. **b,** Optical images of the growth setup. **c,** Optical images of as-grown CoSi samples on the sapphire substrates. **d,** Atomic force microscope image and corresponding thickness-position curve of a representative CoSi nanoflake.



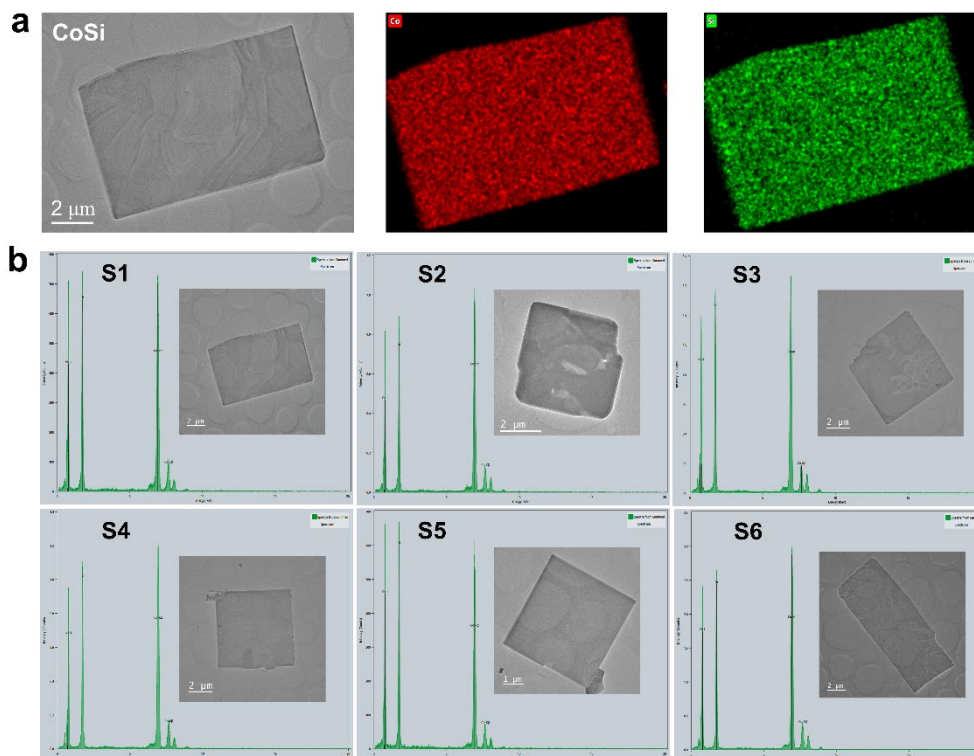
Supplementary Figure 5. Representative thermal profile for the kinetically controlled growth. The curve illustrates a typical heating process for the synthesis of CoSi nanoflakes, using a target temperature of 860 °C as an example. To achieve the kinetic trapping of the ultrathin state, the temperature is first raised to 600 °C, followed by a precise heating ramp of 16 °C/min to reach the growth window.



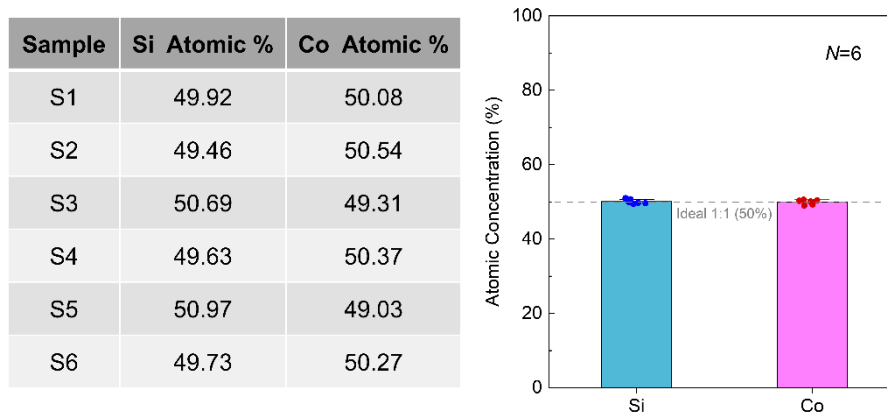
Supplementary Figure 6. Temperature effects on the CoSi crystal growth. Optical microscopy images of CoSi crystals grown at various temperatures (from 770 °C to 920 °C). The precursor-to-flux mass ratio is 1:8.



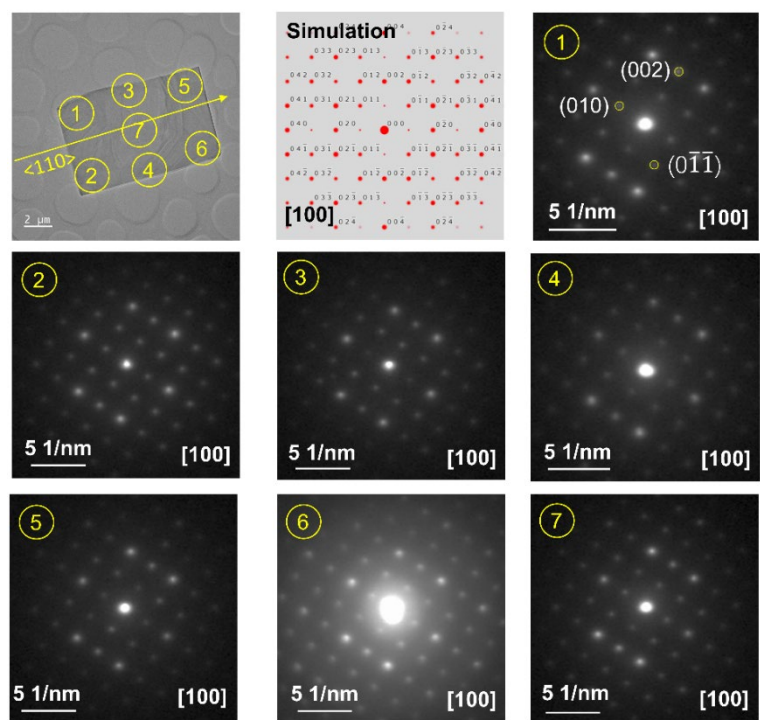
Supplementary Figure 7. Effect of precursor-to-flux mass ratio on the CoSi crystal growth. Optical microscopy images showing the morphological evolution from 1:2 to 1:12. The growth temperature is 860 °C.



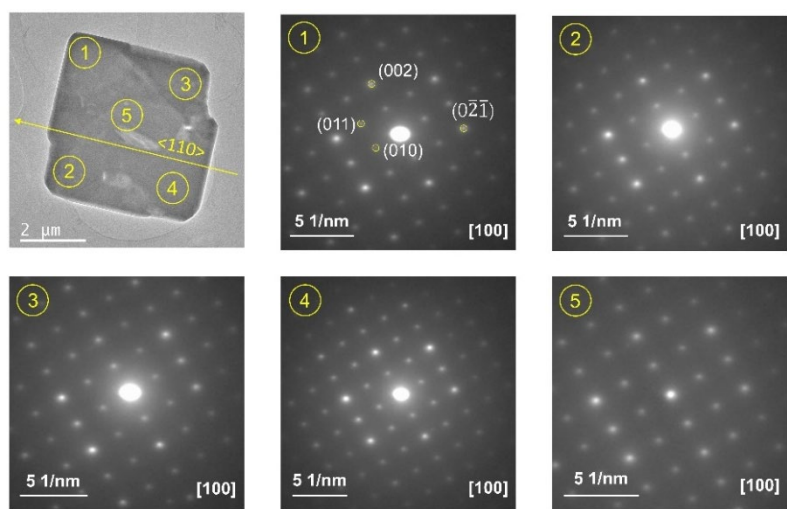
Supplementary Figure 8. Morphology and chemical composition of the as-grown CoSi nanoflakes. **a**, EDS mapping of Sample #S1. **b**, The elemental energy spectrum for Samples #S1 to #S6.



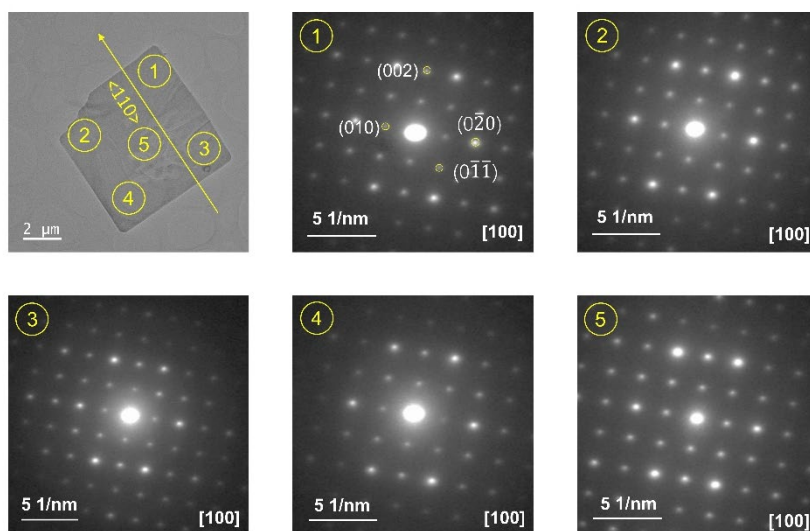
Supplementary Figure 9. Statistical chemical composition analysis of the as-grown CoSi nanoflakes. The table (left) and corresponding bar chart (right) summarize the atomic percentages of Si and Co obtained from EDX point analysis on 6 randomly selected nanoflakes. The individual experimental data points ($n = 6$, overlaid as colored dots) display an extremely narrow distribution tightly clustered around the ideal 50% dashed line. This robust statistical evidence confirms a highly uniform, near-perfect global stoichiometric 1:1 ratio across the synthesized macroscopic samples, well within the instrumental error range.



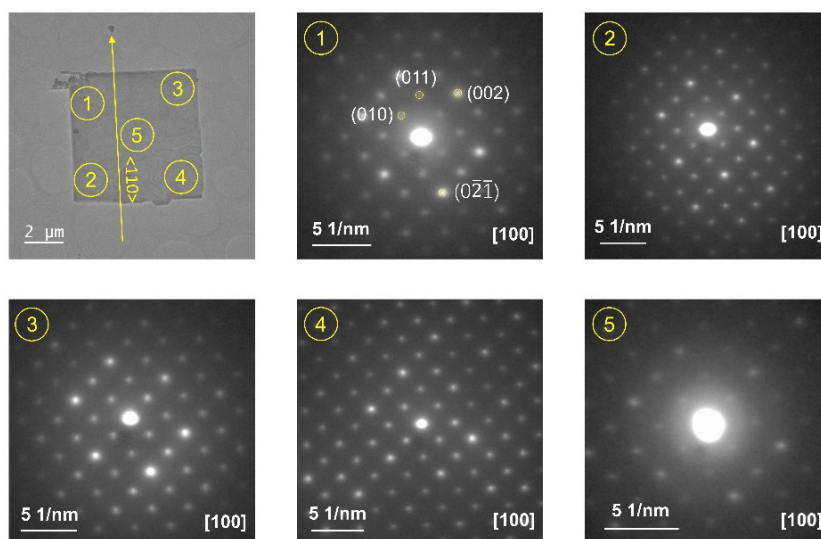
Supplementary Figure 10. Statistical verification of single-crystalline nature across global and local scales (Sample 1). The top-left low-magnification TEM image displays the selected measurement locations (labeled 1 to 7, covering the corners, edges, and center) across the entire macroscopic nanoflake. The corresponding experimental SAED patterns collected from these spatially distinct regions are crystallographically identical and match perfectly with the theoretically simulated diffraction pattern (top-middle panel). All patterns can be unequivocally indexed to the [100] zone axis. This strict experimental-theoretical consistency rigorously confirms a true single-domain nature without any grain boundaries or lattice misorientation.



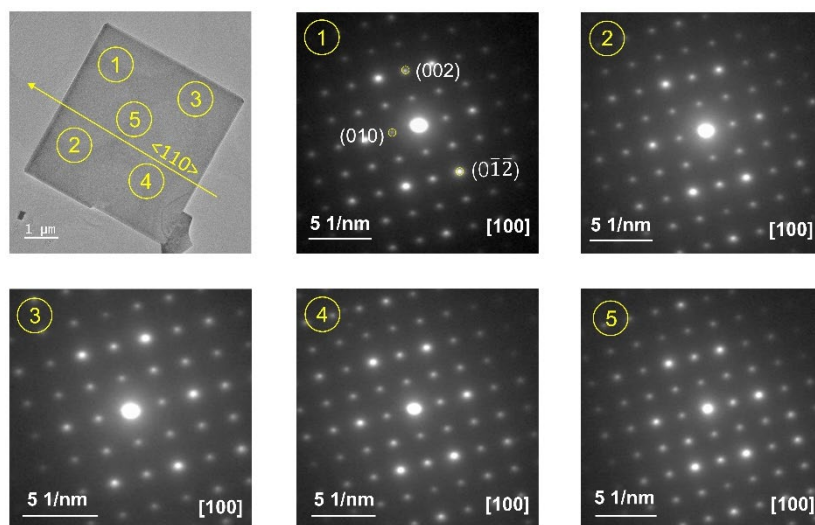
Supplementary Figure 11. Verification of single-crystalline nature for Sample 2.



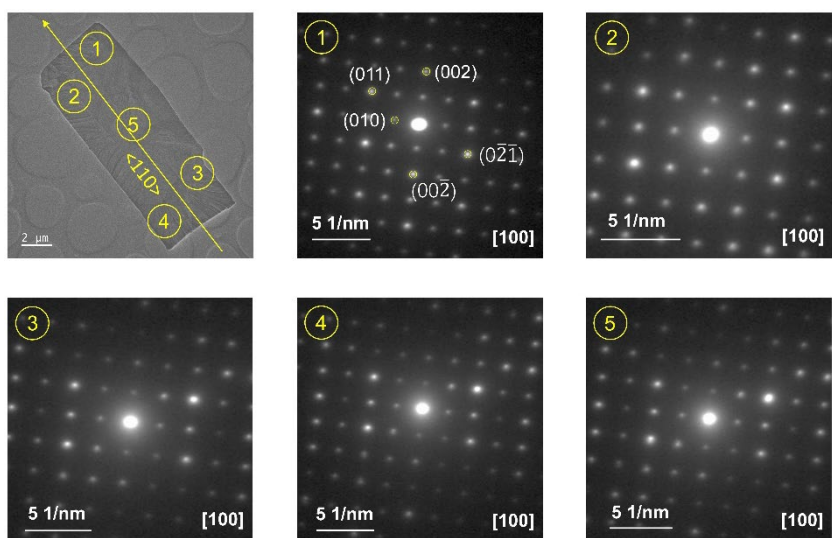
Supplementary Figure 12. Verification of single-crystalline nature for Sample 3.



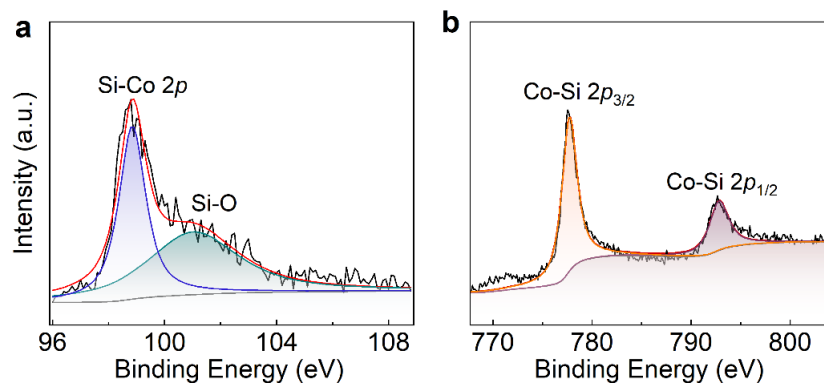
Supplementary Figure 13. Verification of single-crystalline nature for Sample 4.



Supplementary Figure 14. Verification of single-crystalline nature for Sample 5.

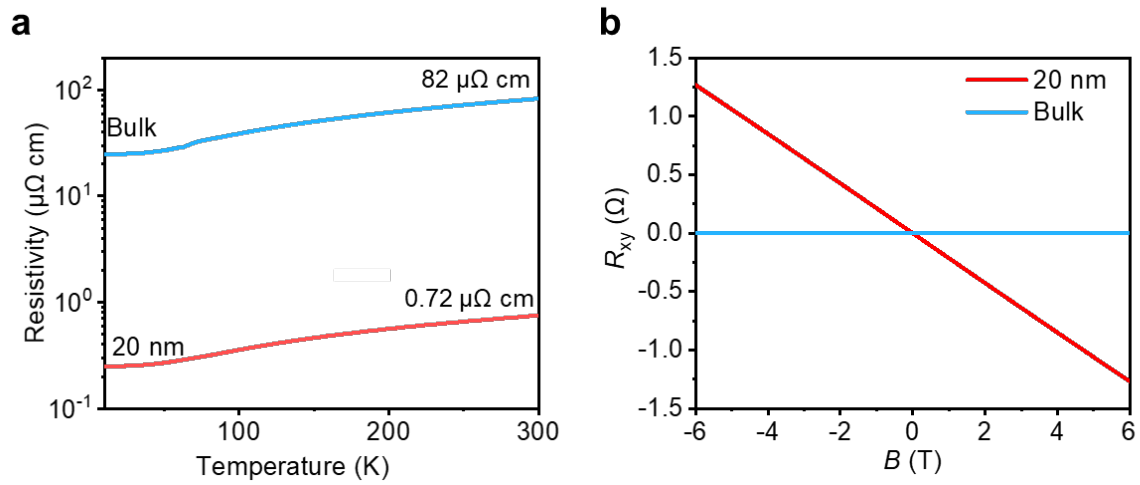


Supplementary Figure 15. Verification of single-crystalline nature for Sample 6.

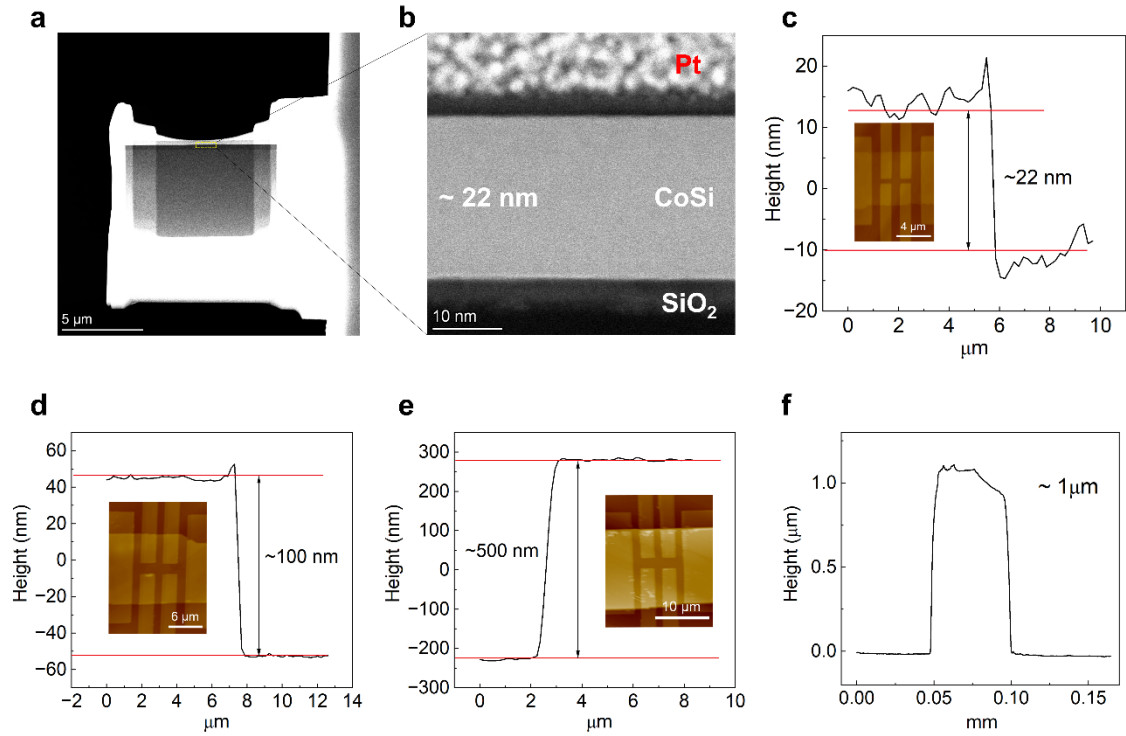


Supplementary Figure 16. Deconvoluted XPS spectra of (a) Si 2p and (b) Co 2p core levels.

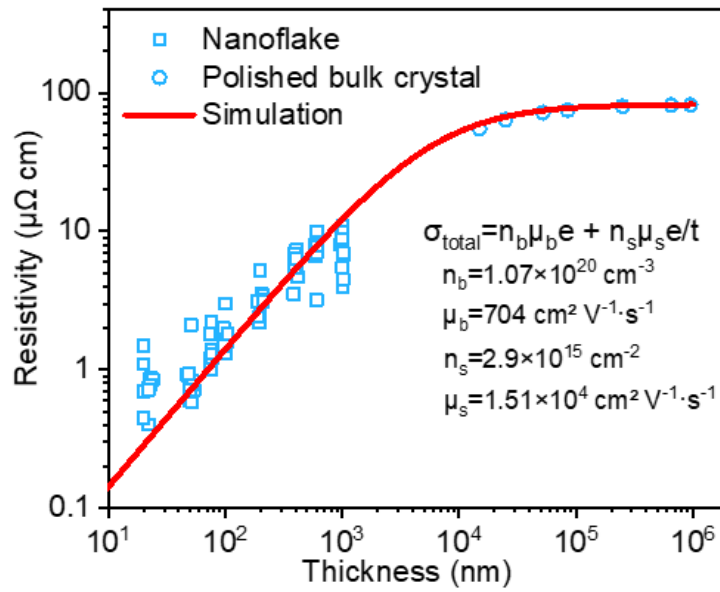
The spectra clearly distinguish the intrinsic Co-Si bonding (sharp peaks) from the surface passivation layer (broad shoulder).



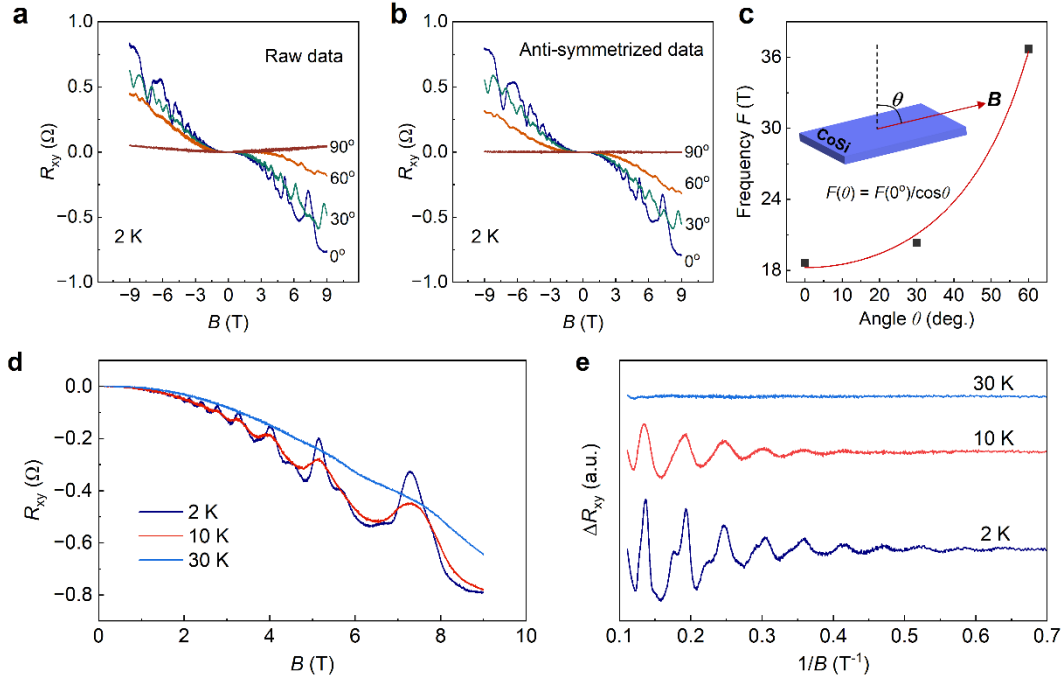
Supplementary Figure 17. Temperature-dependent resistivity and Hall resistance curve of representative bulk and 20-nm samples. a, Temperature-dependent resistivity. **b,** Hall resistance curves.



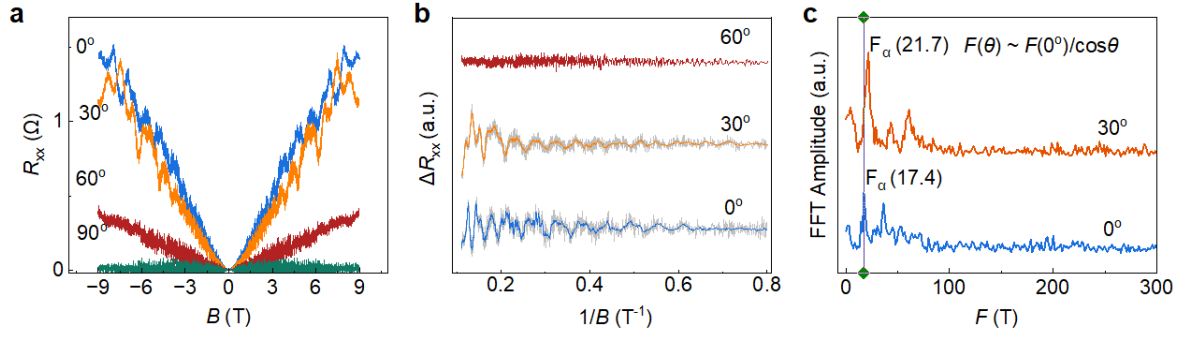
Supplementary Figure 18. Thickness verification of CoSi nanoflakes across different scaling regimes. **a, b**, Low-magnification (a) and high-resolution (b) cross-sectional transmission electron microscopy (TEM) images of a representative ultra-thin CoSi nanoflake, confirming a physical thickness of ~22 nm. **c**, Atomic force microscopy (AFM) height profile of a CoSi device in the same ultra-thin regime, demonstrating excellent quantitative agreement with the TEM structural calibration. **d, e**, Representative AFM height profiles for intermediate-thickness CoSi nanoflakes in the ~100 nm (d) and ~500 nm (e) regimes. The insets show the corresponding AFM images of the fabricated Hall bar devices. **f**, Height profile of a 1000-nm CoSi sample measured using a stylus profilometer.



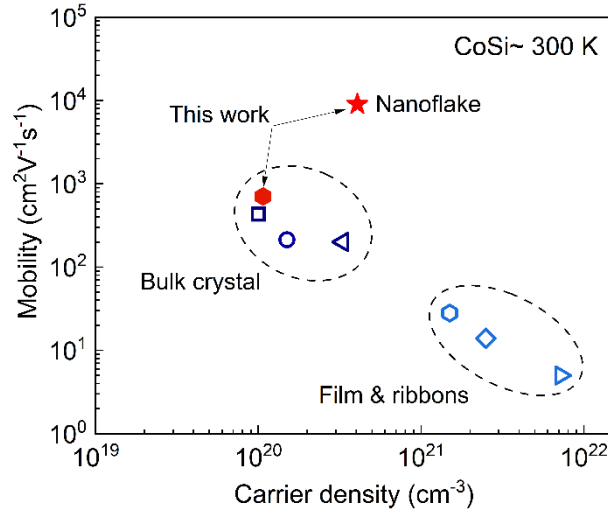
Supplementary Figure 19. Experimental results of CoSi nanoflake and polished bulk crystal compared with the simulation results based on $\sigma_{\text{total}} = n_b \mu_b e + n_s \mu_s e / t$. Bulk samples are mechanically polished from one bulk CoSi crystal with 650 μm .



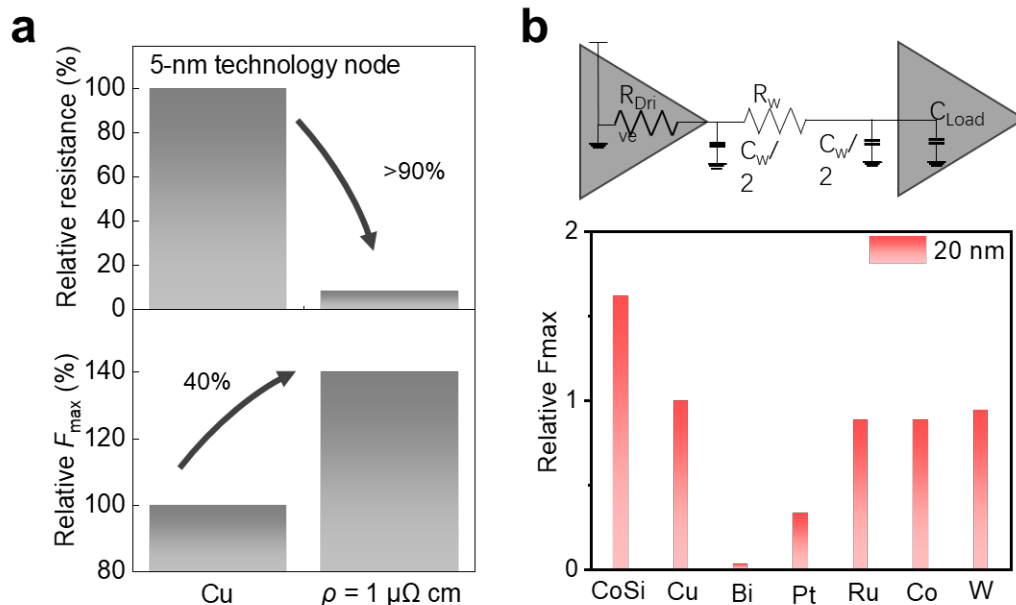
Supplementary Figure 20. Shubnikov-de Haas oscillations in the CoSi nanoflake. **a**, Raw Hall resistance data measured from -9 T to 9 T at various tilt angles. **b**, Anti-symmetrized pure Hall resistance obtained by extracting the anti-symmetric component to eliminate longitudinal resistance mixing. **c**, Angle dependence of the oscillation frequency where the solid red line represents the perfect theoretical fit to the 2D Fermi surface model. The inset illustrates the measurement geometry, defining the tilt angle θ between the applied magnetic field and the surface normal of the CoSi nanoflake. **d**, Hall resistance (R_{xy}) measured under perpendicular magnetic field at 2 K, 10 K, and 30 K. **e**, The extracted oscillatory component (ΔR_{xy}) plotted against the inverse magnetic field ($1/B$). The quantum oscillations are clearly visible at 2 K and 10 K, but are completely suppressed by thermal smearing at 30 K.



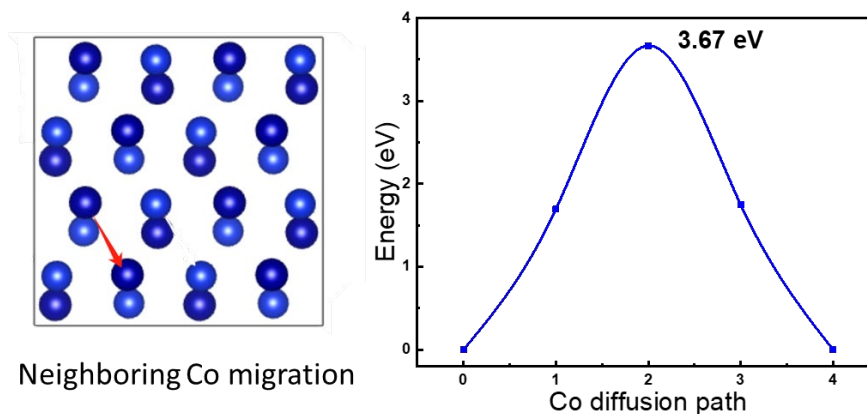
Supplementary Figure 21. Angle-dependent Shubnikov-de Haas oscillations of R_{xx} in the CoSi nanoflake at 2 K. **a**, Resistance R_{xx} measured as a function of magnetic field B from -9 T to 9 T at various tilt angles θ . **b**, Oscillatory component ΔR_{xx} plotted against inverse magnetic field $1/B$ for angles 0° , 30° , and 60° after subtracting a smooth background. Clear SdH oscillations are observed at low angles. **c**, Fast Fourier Transform (FFT) spectra of the oscillations. The primary frequency F_α exhibits a systematic blue-shift from 17.4 T at 0° to 21.7 T at 30° . The inset formula $F(\theta) \sim F(0^\circ)/\cos\theta$ indicates the 2D nature of the Fermi surface.



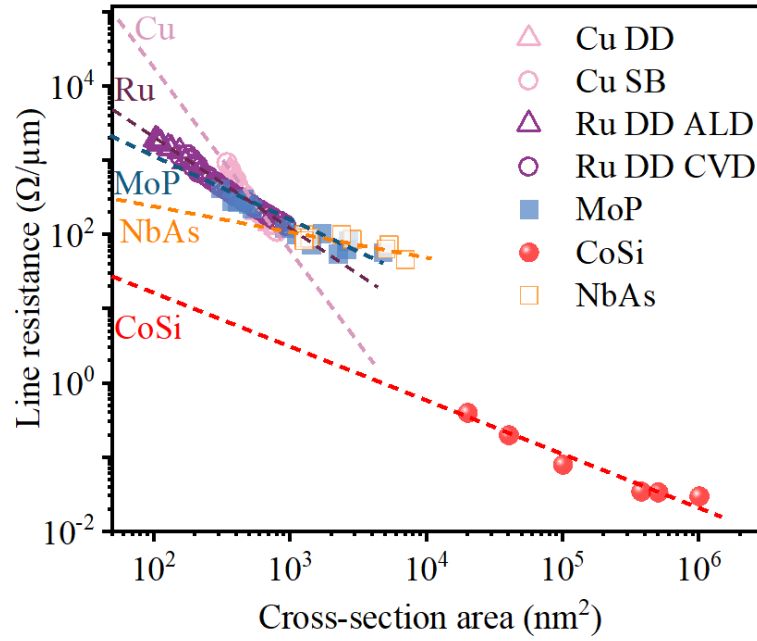
Supplementary Figure 22. Room-temperature Hall mobility versus Hall carrier density for CoSi. Solid red symbols (star and hexagon) represent the CoSi nanoflake and bulk single crystal from this work, respectively. The dashed ovals guide the eye to the general trends of conventional bulk crystals and low-dimensional systems. Open symbols represent representative data from the literature for comparison (bulk crystals¹⁰⁻¹² and thin films/micro-ribbons^{13,14}).



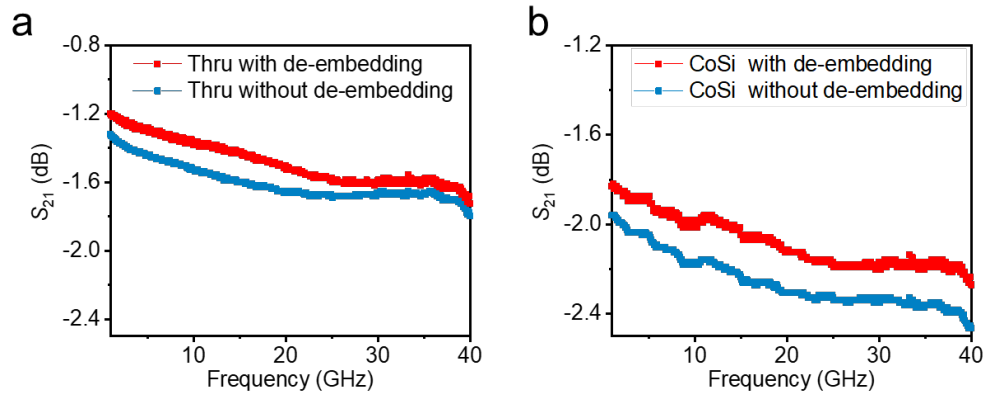
Supplementary Figure 23. The effects of reduced resistance on relative maximum frequency ($F_{\max}$). **a**, The significant increase (40%) of $F_{\max}$ as the resistivity is reduced to $1 \mu\Omega \text{ cm}$ for the circuit of 700 W in the 5-nm-technology node¹. **b**, Signal delay and working frequency benchmark results of CoSi, Cu, Bi, Pt, Ru, Co and W at 20-nm thickness. Simplified lumped-element model for circuit delay and power predictions. Circuit delay and $F_{\max}$ is computed by applying the Elmore approximation.



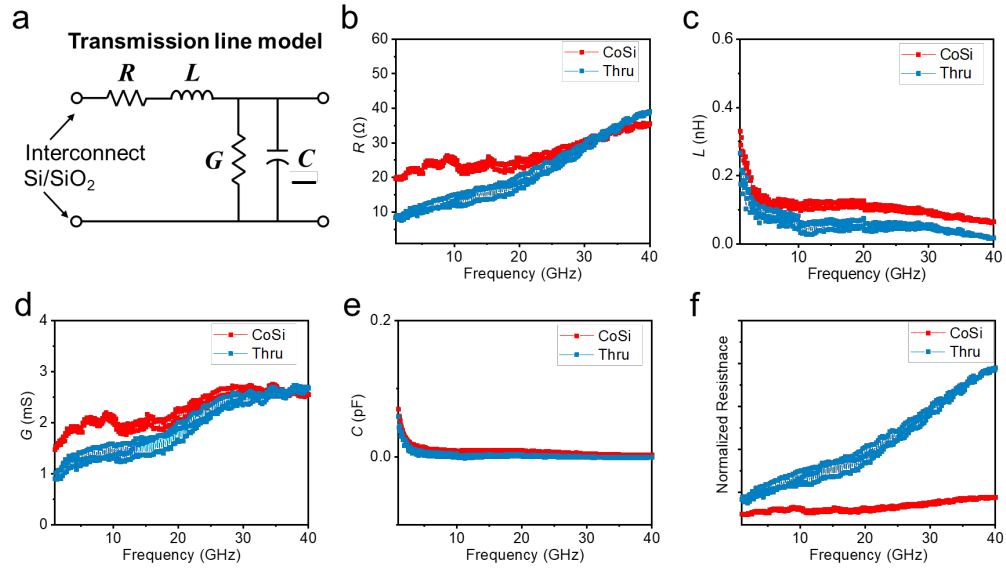
Supplementary Figure 24. Migration barrier of neighboring Co in CoSi. The calculated activation energy of neighboring Co migration is 3.67 eV, a very high value for ion migration.



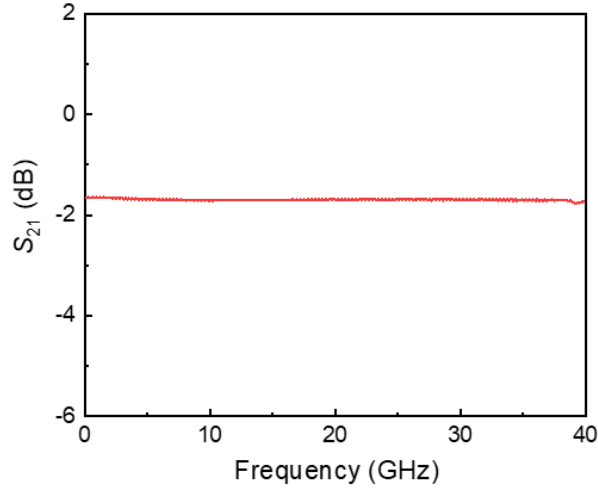
Supplementary Figure 25. Line-resistance scaling of CoSi and representative interconnect materials. Line resistance versus cross-sectional area for CoSi nanoflakes (this work), NbAs nanowires¹⁵, MoP nanowires¹⁶, and Ru/Cu interconnects¹⁶. The Cu data include liner/barrier contributions. DD, dual damascene; SB, selective barrier; ALD, atomic layer deposition; CVD, chemical vapor deposition. Dashed lines denote power-law fits and extrapolations.



Supplementary Figure 26. The S_{21} of metal and CoSi interconnect with/without de-embedding.

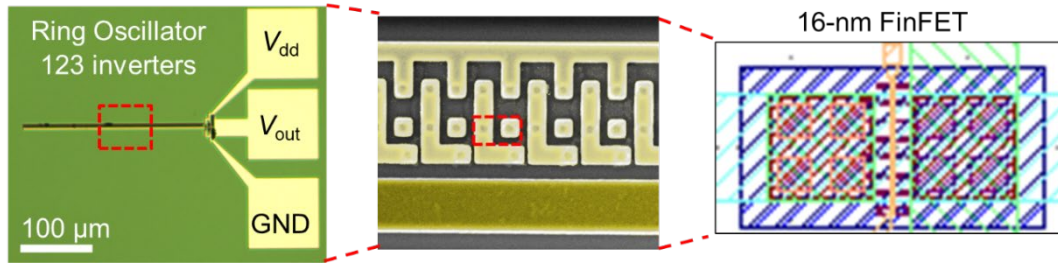


Supplementary Figure 27. The extracted R of metal and CoSi interconnect. a, The equivalent transmission line circuit model. **b-e**, The extracted R , L , G and C of CoSi and thru devices. **f**, The normalized resistance of CoSi and thru devices.

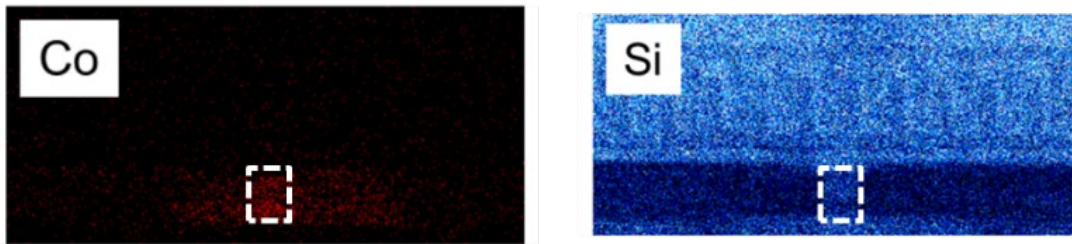


Supplementary Figure 28. S_{21} of the CoSi transmission lines with the quartz substrate.

The transmission losses in our samples are primarily due to dielectric losses, transmission line geometry, and parasitic effects. The Si/SiO₂ substrate with a thickness of 280/0.285 μm has a high dissipation factor ($\tan\delta$), leading to significant dielectric losses. Additionally, the use of transferred CoSi nanoflakes alters the signal line width and signal-to-ground spacing in the coplanar waveguide (CPW) and introduces parasitic factors like contact interfaces. These effects can cause impedance mismatches with the RF measurement system, resulting in large reflections and increased transmission losses. To address these issues, we re-fabricated the RF transmission line using a quartz substrate with low $\tan\delta$ and a thickness of 500 μm , which can reduce the transmission loss (**Supplementary Fig. 27**).



Supplementary Figure 29. The ring oscillator with 123 inverters. Each inverter is comprised of one pair of p-and n-FET.



Supplementary Figure 30. Integration of CoSi interconnect onto the ring oscillator. Co and Si element mapping in the SEM image of Fig. 4e. The white dash box indicates the etched area.

Table S1. Detailed resistivity of CoSi nanoflakes.

Sample	Thickness (nm)	Resistivity ($\mu\Omega$ cm)
#1	20	0.7
#2	22	0.73
#3	23	0.87
#4	24	0.85
#5	23	0.78
#6	22	0.72
#7	20	1.1
#8	20	1.5
#9	22	0.4
#10	20	0.45
#11	50	0.75
#12	53	0.82
#13	47	0.92
#14	49	0.93
#15	54	0.72
#16	53	0.78
#17	50	0.6
#18	52	0.58
#19	51	2.1
#20	50	0.71
#21	74	1.2
#22	75	1
#23	77	1.3
#24	76	2.2
#25	75	1.1
#26	76	1.4
#27	74	1.8
#28	77	1.2
#29	75	1
#30	76	1.3
#31	100	1.3
#32	103	1.8
#33	98	1.7
#34	104	1.6
#35	99	1.7
#36	97	2
#37	100	3
#38	105	1.7
#39	105	1.8
#40	98	1.5

#41	205	3.5
#42	210	3.4
#43	198	2.6
#44	195	2.2
#45	203	3.2
#46	194	2.2
#47	189	3.1
#48	199	5.2
#49	211	3.1
#50	193	2.4
#51	402	6.1
#52	385	3.5
#53	408	7.3
#54	394	5
#55	389	6.5
#56	395	6.9
#57	402	5.3
#58	417	4.7
#59	394	5.4
#60	407	6.3
#61	588	7.2
#62	592	6.6
#63	595	6.9
#64	596	8.1
#65	604	10
#66	599	7.4
#67	601	7
#68	603	3.2
#69	616	7.9
#70	602	7.8
#71	1000	5.5
#72	1030	6.8
#73	960	8
#74	1010	4
#75	1020	4.5
#76	1020	7
#77	1000	10
#78	1010	11
#79	1010	9.8
#80	990	8.8

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Table S2. CoSi mobility comparison for bulk samples and our nanoflake sample.

Sample	Sample form	Quantum oscillation observation method	Onset field	T (K)	Frequencies F (T)	Effective Mass m^* (m_e)	Quantum mobility estimated from B_{onset} μ_q ($\text{cm}^2/\text{V}\cdot\text{s}$)	Transport mobility based on Hall resistance μ_H ($\text{cm}^2/\text{V}\cdot\text{s}$)	Carrier Density n
Chin. Phys. Lett. 36, 077102, 2019	Bulk	Electrical Transport	~ 7 T	0.35	564,665	0.82,0.88	~ 1400	3200-4100	$\sim 10^{20} \text{ cm}^{-3}$
Physical Review B 100, 045104, 2019	Bulk	Thermoelectric	~ 6 T	2	568,671	0.94-1.30	~ 1700	6300	$\sim 10^{20} \text{ cm}^{-3}$
Physical Review B 102, 115129, 2020	Bulk	Magnetization	~ 3 T	2	19.6, 557.6, 656.7	0.11,0.36, 0.37	~ 3400	—	—
Our work	Nanoflake	Electrical Transport	~ 1.5 T	2	18.64	~ 0.11 (Est.)	~ 6700	\	\
		Electrical Transport	\	300	\	\	\	Total: 1.1×10^4 Surface: 1.5×10^4 Bulk: 7×10^2	Surface: $2.90 \times 10^{15} \text{ cm}^{-2}$ Bulk: $1.07 \times 10^{20} \text{ cm}^{-3}$
	Bulk	Electrical Transport	\	300	\	\	\	7×10^2	$\sim 10^{20} \text{ cm}^{-3}$

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Table S3. Parameters for calculating the normalized working frequencies

Parameters	Value						
Material	CoSi	Cu	Bi	Pt	Ru	Co	W
Resistivity($\mu\Omega\cdot\text{cm}$)	0.72	7	500	40	9.1	9.1	8
Length of wire(μm)	1						
Cross sectional area(μm^2)	450						
Permittivity (pF/ μm)	8.85×10^{-12}						
Relative permittivity	3.9						
Area of plate(μm^2)	450						
Separation distance(μm)	1						
RDrive (m Ω)	0.21						
CLoad(nf)	910						

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