

Highly reproducible van der Waals integration of two-dimensional electronics on the wafer scale

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Supplementary text

Energy release rate analysis of van der Waals (vdW) integration process over large-area

The picking-up and releasing process is modeled by competing separation between the polydimethylsiloxane (PDMS) and polymethyl methacrylate (PMMA) interface and the PMMA/substrate interface. According to the Griffith criterion, energy release rate (G) was used to describe the energy of interfacial bond breaking and adhesive dissipation around the crack tip¹. Additionally, the energy release rate was determined by

$$G = \frac{F}{w} \quad (1)$$

Where F and w is the peeling force and width of the interface, respectively. When the value of G reaches the critical G value, the crack starts to propagate at the interface. For convenience, we denote $G_{\text{PDMS/PMMA}} (T_{\text{pick-up}})$, $G_{\text{PDMS/PMMA}} (T_{\text{release}})$, $G_{\text{PMMA/sacrificial substrate}}$, and $G_{\text{PMMA/receiving substrate}}$ as the critical G of PDMS/PMMA at the temperature for picking-up and releasing, PMMA/sacrificial substrate, and PMMA/receiving substrate interface, respectively. The criterion for picking-up and releasing can be obtained by comparing the critical G , that is

$$G_{\text{PDMS/PMMA}} (T_{\text{pick-up}}) > G_{\text{PMMA/sacrificial substrate}} \quad (2)$$

for picking-up the electrodes from sacrificial substrate and

$$G_{\text{PDMS/PMMA}} (T_{\text{release}}) < G_{\text{PMMA/receiving substrate}} \quad (3)$$

for releasing the electrodes on receiving substrate².

To further facilitate the interface analysis, the $G_{\text{PDMS/PMMA}} (T_{\text{pick-up}})$ and $G_{\text{PMMA/sacrificial substrate}}$ was experimentally measured at 20 °C, while $G_{\text{PDMS/PMMA}} (T_{\text{release}})$ and $G_{\text{PMMA/receiving substrate}}$ was measured at 120 °C. The $G_{\text{PDMS/PMMA}} (T_{\text{pick-up}})$, $G_{\text{PDMS/PMMA}} (T_{\text{release}})$, $G_{\text{PMMA/sacrificial substrate}}$, and $G_{\text{PMMA/receiving substrate}}$ is about 124.2, 21.6, 27.0 and 56.7 J m⁻², respectively, which is completely coherent with the criterion for picking-up and releasing process (Supplementary Fig. 5a). The energy release rate was tested by a tensile testing machine³.

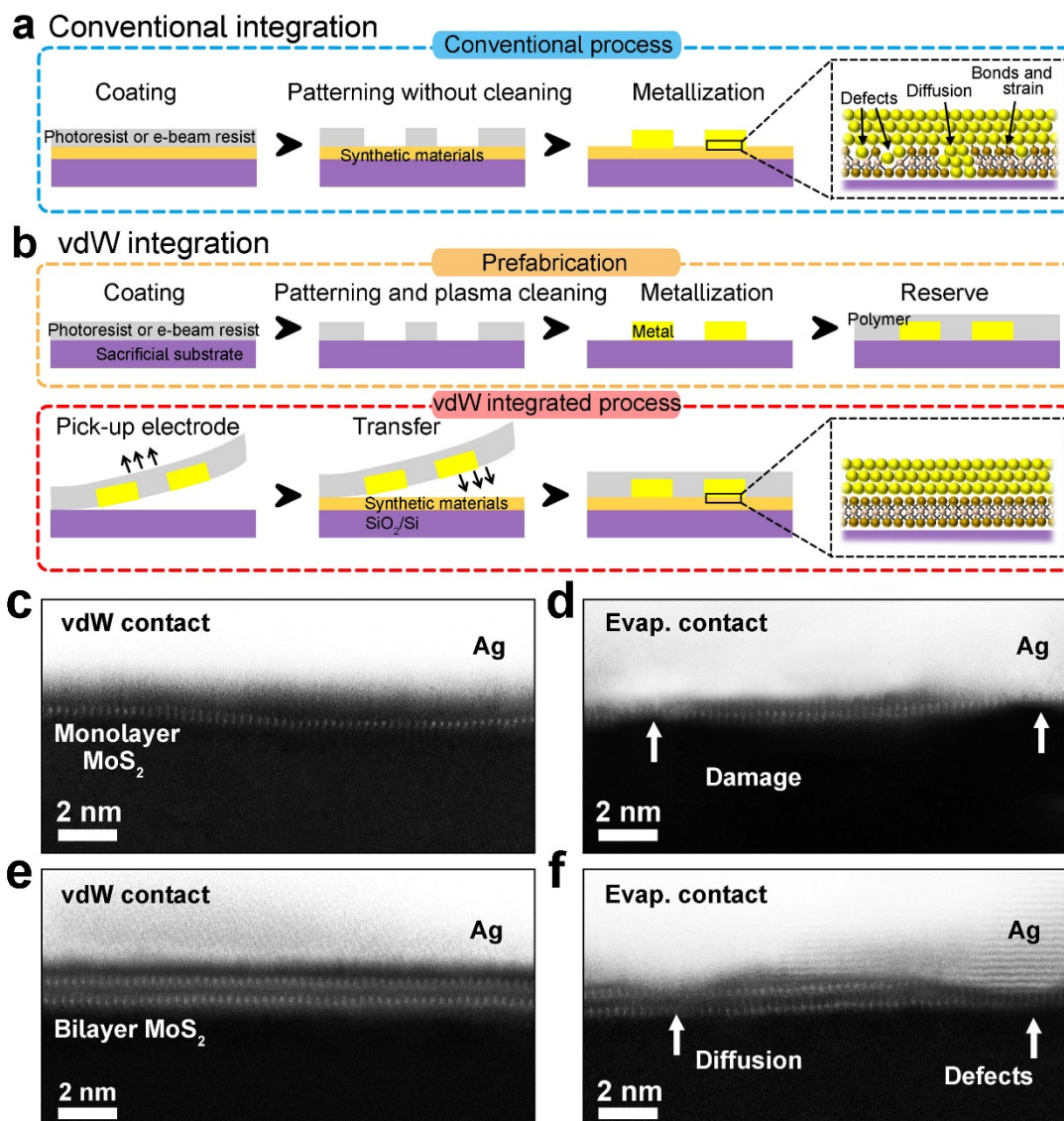
These experimental results clearly highlight that the PDMS/PMMA interface control is essential for achieving reliable picking-up/releasing processability.

Finite element analysis of vdW integration process over large area

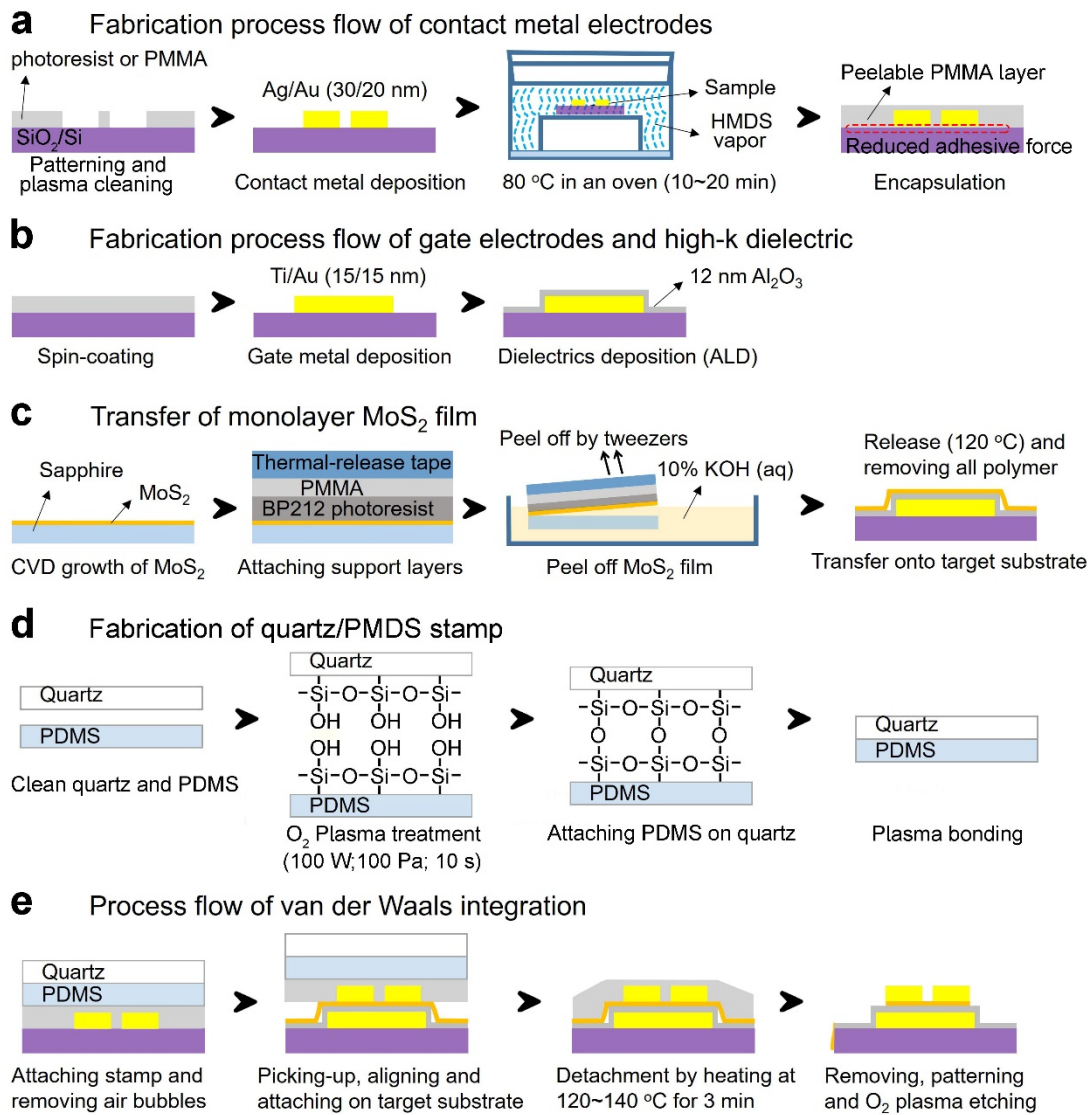
To further achieve reliable vdW integration over large area, a finite element analysis (FEA)

is performed to visualize the stress distribution in the PMMA layer when a small and uniform pulling up force was applied on the quartz/PDMS stamp. We used ABAQUS commercial software to perform the FEA before the PMMA layer was picked-up. Thus, we can assume that there is no relative slip existing at the interface between the quartz, PDMS, PMMA and substrate. We created two mechanical model, with one of the model with an air bubble in the PDMS/PMMA interface and another is bubble-free. The thickness of quartz, PDMS, PMMA and substrate are 2 mm, 1 mm, 1.5 μm and 0.5 mm, respectively, and the length and width of the model are both 10 mm. The PDMS and PMMA were both modeled by linear elastic material. The Young's modulus and Poisson's ratio of PDMS were 3 MPa and 0.5, respectively. The Young's modulus and Poisson's ratio of PMMA were set to be 2.9 GPa and 0.39, respectively. In the mechanical simulations, the quartz was applied a uniform pulling up force of 0.2 N and the substrate was fixed to obtain the stress distribution of PMMA layer. In the mechanical simulations, the quartz was applied a small and uniform pulling up force and the substrate was fixed to obtain the stress distribution of PMMA layer. According the stress distribution contour plot of FEA results, if there is an air bubble in the PDMS/PMMA interface, an obvious large stress on PMMA layer occurred around the edge of the air bubble, which is at least one order of magnitude larger than that in the conformal contact area (Supplementary Fig. 5b). The large difference in stress distribution in PMMA layer around the bubble could result in failure of scalable picking-up process and contribute to the failure of PMMA layer or expansion of air bubble based on our experimental experiences. On the other hand, in the model with bubble-free PDMS/PMMA interface, the FEA results show that the stress distribution in PMMA layer is very uniform (Supplementary Fig. 5c). Consequently, the PMMA layer received a uniform pulling force to guarantee a successful picking-up of PMMA layer over large area. Therefore, the PDMS/PMMA interface control is critical for competing separation between the PDMS/PMMA interface and the PMMA/substrate interface, and is a key parameter to ensure reliable and scalable picking-up/releasing processability over large area.

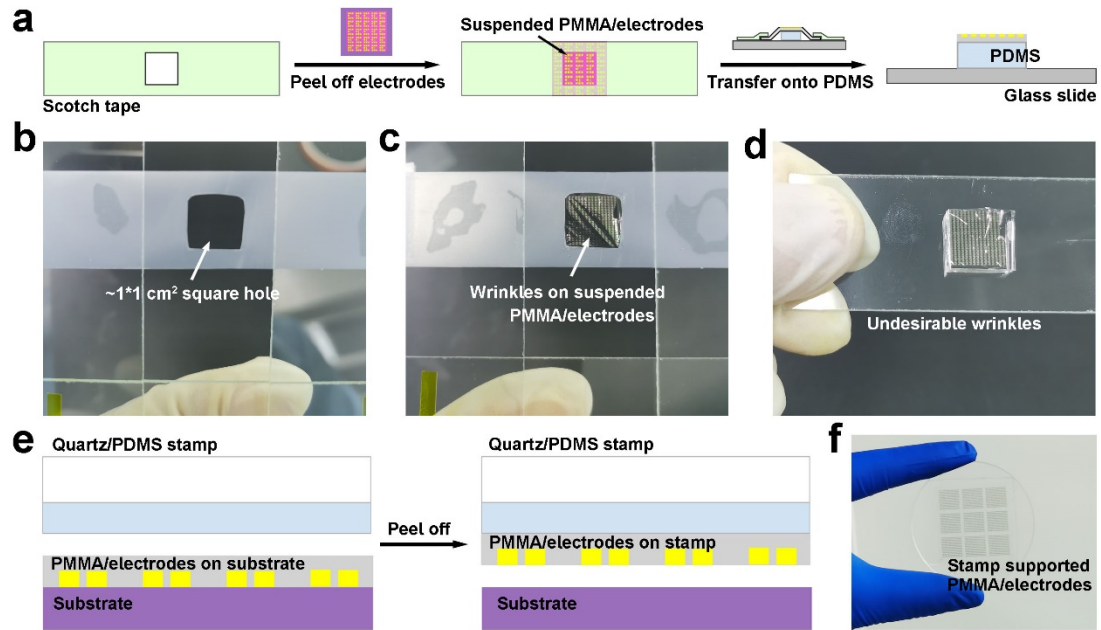
Supplementary Figures



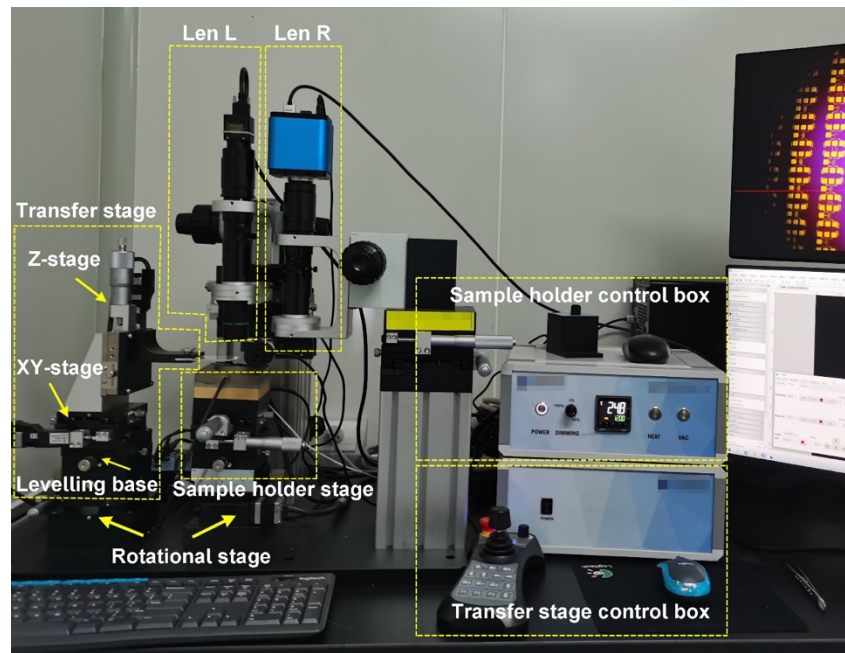
Supplementary Fig. 1 | Schematic illustration of fabrication process. a, b, Schematic illustration of conventional integration (**a**) and vdW integration (**b**). **c, d,** Metal/semiconductor interface of monolayer MoS₂ device with vdW Ag/Au contact (**c**) and deposited Ag/Au contact (**d**). **e, f,** Metal/semiconductor interface of bilayer MoS₂ FETs with vdW contact (**e**) and deposited contact (**f**).



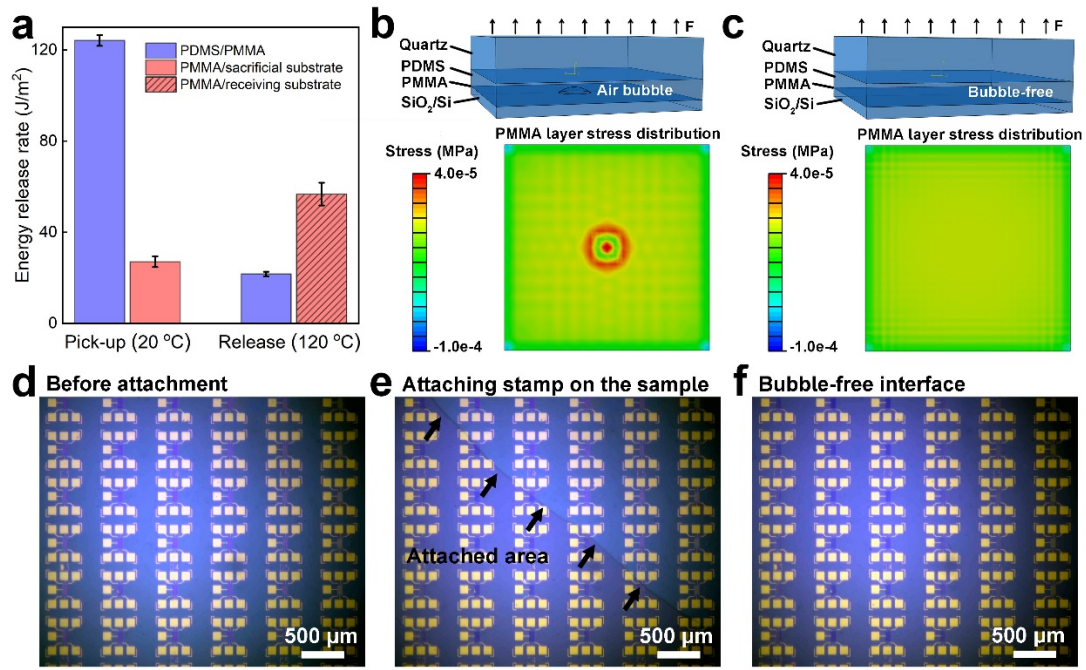
Supplementary Fig. 2 | Fabrication process flow of all vdW integration. a, b, Fabrication process flow of contact metal electrodes (**a**), gate electrodes and high-*k* dielectric (**b**). **c**, Transfer of monolayer MoS₂ film. **d**, Fabrication of quartz/PDMS stamp. **e**, Process flow of vdW integration.



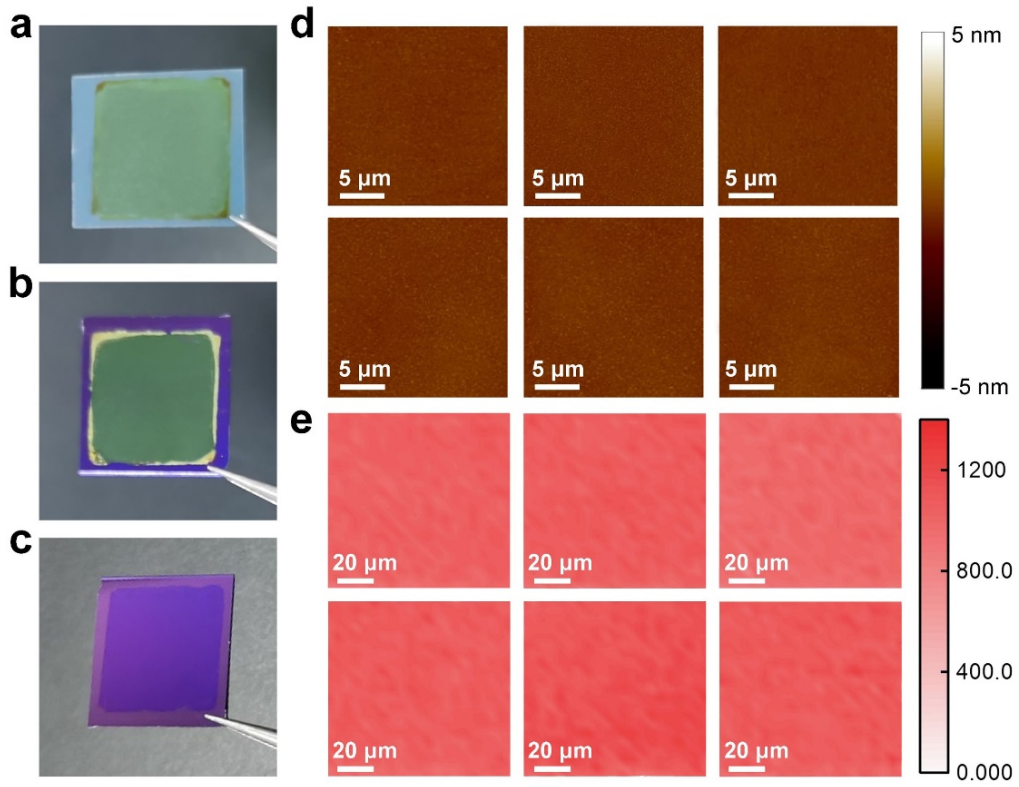
Supplementary Fig. 3 | Comparison of conventional vdW integration method and large scale vdW integration method with quartz/PDMS hybrid stamp. a, Schematic of a conventional vdW integration method. **b-d,** Picture of scotch tape with a $\sim 1 \times 1 \text{ cm}^2$ square hole (**b**), suspended PMMA/electrodes layer on scotch tape (**c**) and PMMA/electrodes layer on a PDMS stamp (**d**). **e,** Schematic of large scale vdW integration method. **f,** Picture of PMMA/electrodes layer on quartz/PDMS stamp.



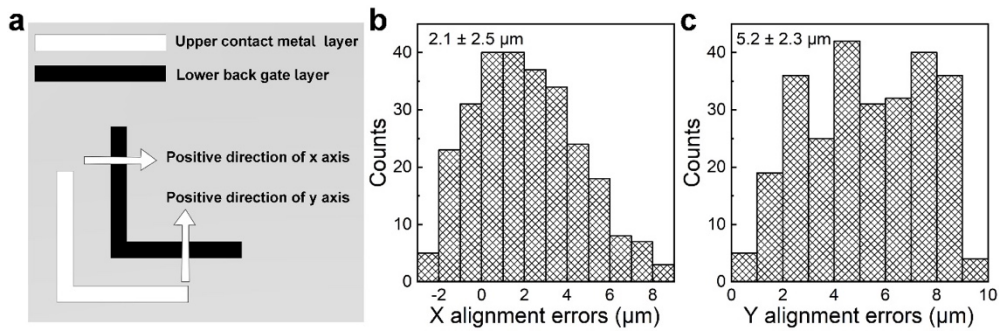
Supplementary Fig. 4 | Picture of a customized 2-lens transfer platform.



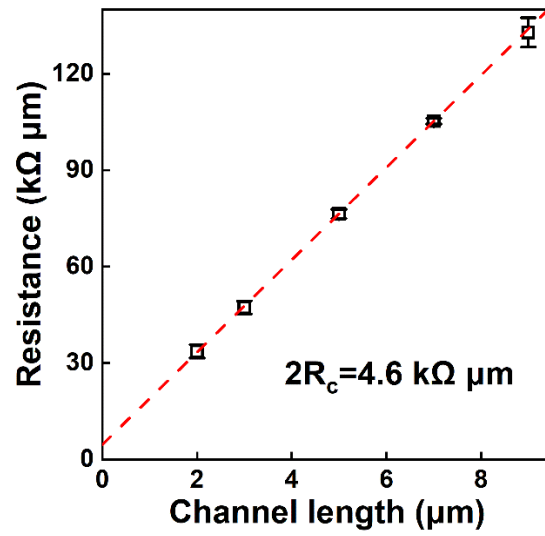
Supplementary Fig. 5 | Large scale vdW integration analysis. **a**, Energy release rate of PDMS/PMMA and PMMA/substrate interfaces in picking-up and releasing process. Data are presented as mean $\pm$ S.E. ($n = 3$). **b**, The simulation model with an air bubble trapped at the PDMS/PMMA interface and the corresponding stress distribution in PMMA layer in the picking-up process. **c**, The simulation model with bubble-free PDMS/PMMA interface and the corresponding stress distribution in PMMA layer in the picking-up process. **d-f**, Optical microscope images of before attachment (**d**), attaching stamp on the sample (**e**) and after forcing the air bubbles out (**f**). The black arrows in panel **f** highlights the lamination contacting edge.



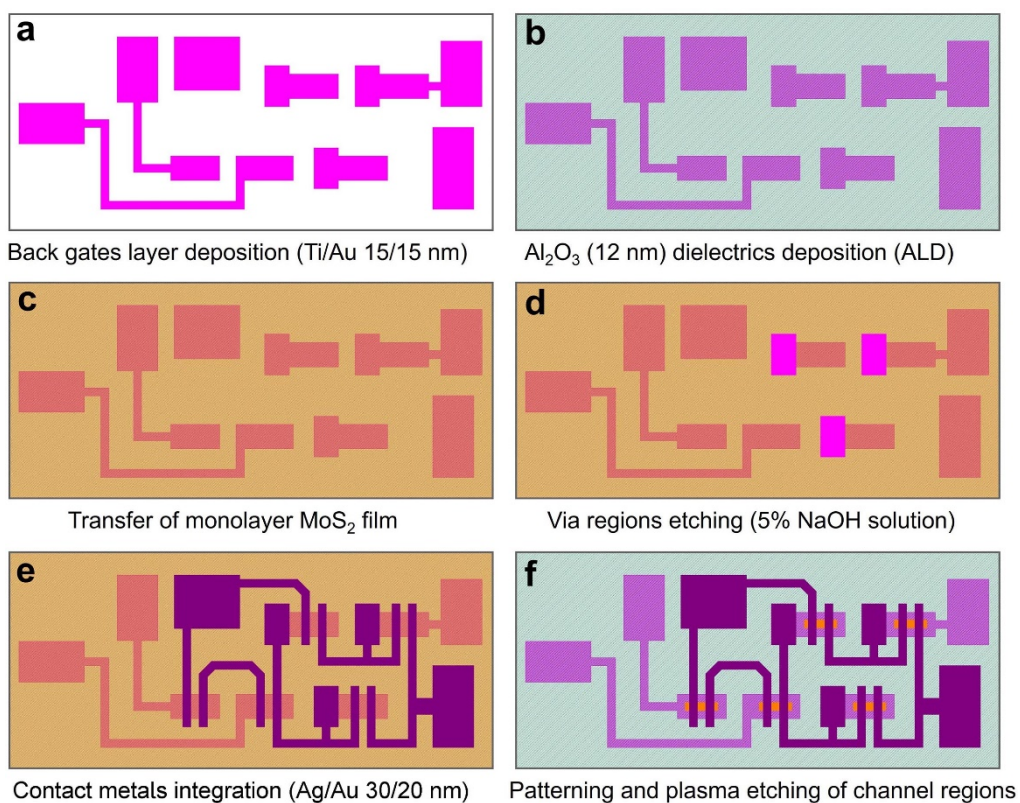
Supplementary Fig. 6 | Smooth surface and uniformity of large scale MoS₂ film. a-c, Picture of TRT/PMMA/photoresist/MoS₂ layer (a), PMMA/photoresist/MoS₂ layer on SiO₂/Si substrate (b) and MoS₂ film on SiO₂/Si substrate (c). d, e, AFM images (d) of 6 randomly selected locations and PL mapping images (e) of 6 randomly selected locations over a large scale.



Supplementary Fig. 7 | Alignment errors distribution of vdW integration technology. a, Schematic of the definition of positive direction of x- and y-axis alignment offset. **b, c,** Alignment errors distribution for x-axis (**a**) and y-axis (**b**).



Supplementary Fig. 8 | Contact resistance (R_c) extraction using the transfer-length method (TLM) for MoS₂ FETs with vdW Ag contact. Data are presented as mean $\pm$ SD (n = 3).



Supplementary Fig. 9 | Top-view process flow of MoS₂-based logic gates (AND gates).

References

- 1 Yan, Z. C. *et al.* Thermal release transfer printing for stretchable conformal bioelectronics. *Adv. Sci.* **4**, 1700251 (2017).
- 2 Feng, X. *et al.* Competing fracture in kinetically controlled transfer printing. *Langmuir* **23**, 12555–12560 (2007).
- 3 Peng, Z. L., Wang, C., Chen, L. & Chen, S. H. Peeling behavior of a viscoelastic thin-film on a rigid substrate. *Int. J. Solids Struct.* **51**, 4596–4603 (2014).