
Millisecond phonon lifetimes in piezoelectric nanomechanical resonators

In the format provided by the
authors and unedited

1. SHADOW-MASK DISTORTION IS NEGLIGIBLE

There are several possible contributions to misalignment in shadow-masked patterning which are addressed in the bonding scheme described in the Methods. The most direct contribution is the misalignment in the flip-chip bonding tool, which causes global translation and rotation of the observed pattern compared to the desired pattern. Here, we work within the $\approx 1\text{ }\mu\text{m}$ translational tolerance of a research-grade flip-chip bonder. This is insufficient compared to the $100\text{ nm} - 500\text{ nm}$ tolerance in alignment required for the PnC contact metallization. As a brute-force solution to this problem, we pattern a large array of 10×6 devices on each LN chip, offsetting the device and shadow-mask positions in a vernier capable of accommodating up to $\approx 2\text{ }\mu\text{m}$ translational mask-pattern shift while still yielding aligned devices. The deliberate misalignment of the vernier limits the metallization yield, but this yield is now independent of the overall misalignment between the shadow-mask and LN chip. In practice, we see an expected and observed 10 % to 20 % metallization yield for devices with the narrowest electrode spacing, which increases to 70 % to 80 % for the devices with the largest electrode spacing. For these large electrode spacing devices, κ_e is largely insensitive to electrode misalignment.

There are multiple routes towards improving the shadow-mask alignment. Production die bonders reach alignment tolerances of 300 nm , which would provide adequate alignment with no vernier for all but the smallest electrode spacing devices. Even for these devices, the vernier steps can be reduced, increasing the minimum yield. Beyond the bond tool tolerance, the shadow-mask technique admits self-alignment with $\leq 100\text{ nm}$ tolerance [1][2], using approaches such as etched divots in the shadowmask chip, compatible with our current fabrication, which mate with LN bumps. This may entirely decouple the ultimate shadowmask alignment from the bonder tolerance and provide sufficient alignment to remove the vernier entirely.

The second, more subtle, source of misalignment is due to deformation of the shadow-mask membrane relative to the chip. Asymmetric clamping forces can cause spacing variation over the membrane, which causes a position-dependent (nonlinear) shift of the deposited pattern [3]. Furthermore, deposition of material onto a membrane modifies its strain, which can lead to a deflection of the membrane during deposition, ‘smearing’ out a deposited pattern on the LN. This effect is exacerbated when the membrane is asymmetrically clamped at the beginning of the deposition. We use thick ($525\text{ }\mu\text{m}$) and therefore stiff silicon substrate and optimize the clamping uniformity to minimize this.

In general, the coordinates of a shadow-mask-deposited feature $\vec{x}_{\text{actual}}$ will vary from the desired

position $\vec{x}_{\text{target}}$ by:

$$\vec{x}_{\text{actual}} = \mathbf{R}\vec{x}_{\text{target}} + \vec{\Delta x} + \vec{\delta}(\vec{x}) \quad (\text{S1})$$

where $\mathbf{R}$ and $\vec{\Delta x}$ correspond to the global rotational and translational misalignment due to flip-chip bonding, and $\vec{\delta}(\vec{x})$ is an additional catch-all position-dependent misalignment that we name the ‘distortion’. There are many plausible contributions to $\vec{\delta}$. Here, our focus is on deformation of the shadow-mask membrane, which leads to a position-dependent displacement. Other contributions may include distortions in lithography, such as write-field stitching, or thickness variations in the spacer layer. While the deformation will fundamentally limit the alignment precision achievable with these shadowmasks, lithographic pattern or spacer thickness variations can be improved with better nanofabrication. It is difficult to identify the precise makeup of the net distortion, so measurements of $\vec{\delta}$ provide only an upper bound on the effect of shadow-mask deformation on the LN metallization.

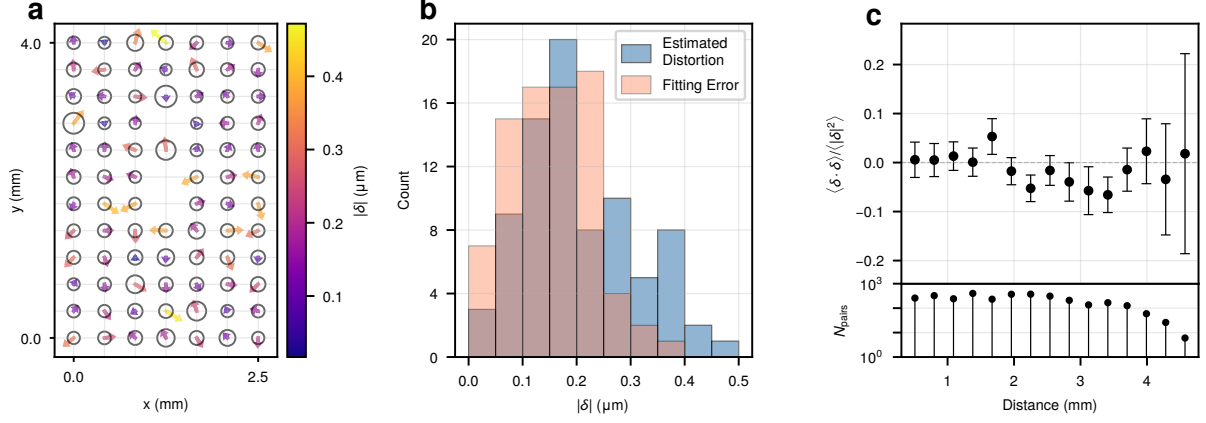
We characterize $\vec{\delta}$ of our shadow-masking process by performing an aligned deposition of 81 markers over a $2.5 \text{ mm} \times 4 \text{ mm}$ region of a test chip, forming a 7×12 index grid. We compare the position of the shadow-masked markers to their corresponding reference markers on the target chip, which are patterned through optical lithography, to measure $\vec{x}_{\text{actual}} - \vec{x}_{\text{target}}$ at each grid position. We least-squares fit the entire dataset to determine the global translation $\vec{\Delta x}$ and rotation $\mathbf{R}$ misalignments, where the residual of this fit for each grid position is $\vec{\delta}(\vec{x}_{\text{target}})$. Marker position and position uncertainty are estimated through computer vision on optical images of the chip following deposition, and uncertainties are propagated through Monte Carlo.

Supplementary Fig. 1 illustrates (a) the measured $\vec{\delta}$ at each grid position, and (b) the distribution of measured $|\vec{\delta}|$ compared to the distribution expected given measurement uncertainty and assuming $|\vec{\delta}| = 0$. The experiment is generally limited by uncertainties but bounds distortion at $\leq 500 \text{ nm}$ across the chip, well below the alignment error. We calculate the spatial autocorrelation

$$C(r) = \frac{1}{2n} \sum_k^n \frac{\langle \vec{\delta}(\vec{x}_k) \cdot \vec{\delta}(\vec{x}'_k) \rangle}{\langle |\vec{\delta}|^2 \rangle} \quad (\text{S2})$$

where $k = 1, 2, 3 \dots n$ are the grid point pairs (x_k, x'_k) that fulfill the condition $\left| |\vec{x}_k - \vec{x}'_k| - r \right| \leq \Delta$. 2Δ is our bin width that we set as $300 \mu\text{m}$. This autocorrelation does not reveal any length scale over which distortion is self-similar as would be expected for membrane deformation (Supplementary

Fig. 1c). The lack of strong evidence for distortion in this experiment is unsurprising, as deposition at normal incidence is to first order insensitive to height variation in the mask. More broadly, this suggests that shadow-mask membrane deformation is negligible for this fabrication process.



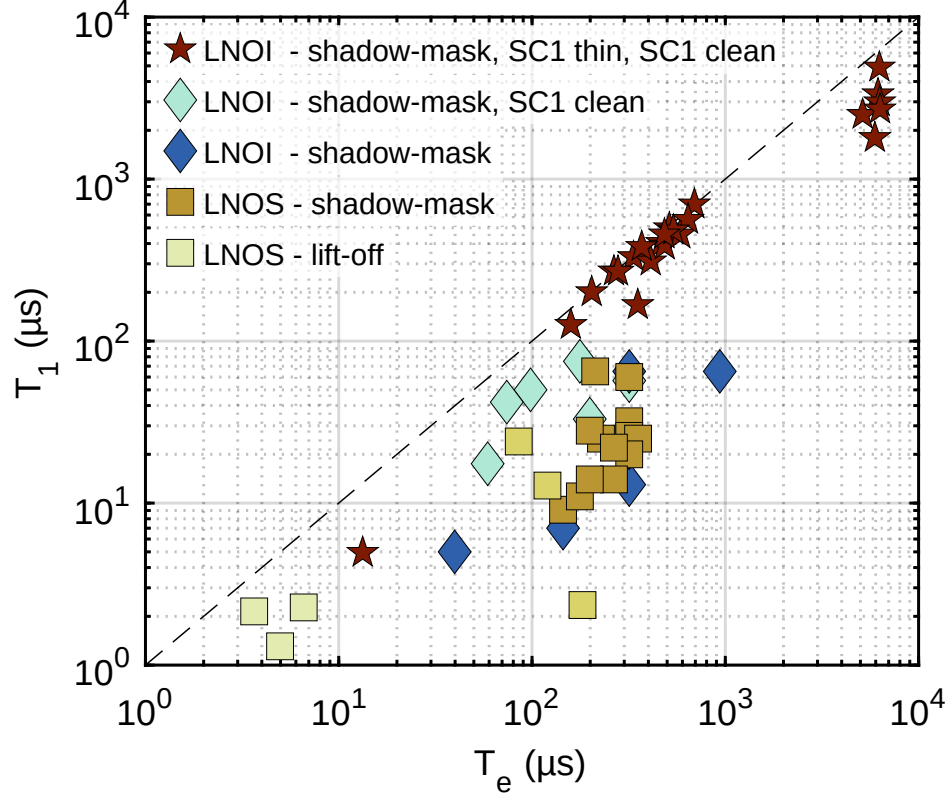
Supplementary Fig. 1: **Shadow-mask distortion characterization.** **a**, Distortion vectors measuring the displacement between each alignment marker and its corresponding shadow-mask deposited marker on the sample. Uncertainty is estimated through 30 independent fits on unique subsets of identified alignment marker boundary pixels, and represented by the circle radii. The (x, y) position of each distortion arrow starting point and circle center shows the position of the marker pair on the chip. The empty regions are used for coarse alignment features. **b**, The distribution of measured distortion vector magnitudes is shown in blue, and is compared to the distribution expected from solely from fitting errors shown in red. **c**, The spatial autocorrelation of the magnitude of distortion. Each point shows the average autocorrelation across a $300 \mu\text{m}$ wide bin of distances.

2. COMPARISON OF PHONON LIFETIMES FOR SEVERAL FABRICATION FLOWS

To support the reproducibility of the measured lifetimes and resolve the effect of the surface restoration techniques enabled by shadow-masking, we present an extended set of measurements that compare eight variants of the fabrication flow. Importantly, all devices share the same crystal orientation and shear mode defect resonance embedded within a phononic bandgap, while the precise geometries are perturbed slightly within a device array and between devices to allow for frequency multiplexing. As a result, the resonant frequency, T_e and T_1 are naturally expected to vary between devices, therefore, we report T_1/T_e , a dimensionless coupling limit saturation ratio, as the informative statistic to compare between designs. The main fabrication steps as well as the mean, standard deviations, and sample sizes of the T_1/T_e ratios are reported in Supplementary Table 1. Coming from the same lithium niobate on insulator (LNOI) wafer, variants 1–3 correspond to the devices discussed in the main text and variants 4–6 represent the switch to shadow-masking and experimentation with different surface restoration techniques. Meanwhile, variants 7–8 represent the legacy fabrication process with lift-off metalization and a lithium niobate on silicon (LNOS) stack. We find that in the absence of metal losses, the implementation of shadow-mask metalization and the surface restoration techniques it enables (variants 1 and 2) results in higher T_1/T_e , indicating reduced intrinsic phonon losses compared to the other fabrication variants. Supplementary Fig. 2 shows T_1 and T_e for all resonators that enter this comparison.

Supplementary Table 1: **Process variants and statistics.** Each variant lists the film stack, electrode gap, metalization method, whether SC1 thinning or final SC1 cleaning were performed, the mean and standard deviation of the external-coupling saturation T_1/T_e , and the number of measured resonators n within the variant. The devices presented in the main text belong to variants 1, 2 and 3. [†]Variant 3 has an insufficient sample size to report a standard deviation.

Variant	Stack	Electrode gap	Metalization	SC1 thin	SC1 clean	T_1/T_e	n
1	LNOI	4760 nm	shadow-mask	Y	Y	0.50(16)	6
2	LNOI	2800 nm	shadow-mask	Y	Y	0.86(15)	16
3	LNOI	360 nm	shadow-mask	Y	Y	0.37 [†]	1
4	LNOI	1700 nm	shadow-mask	N	Y	0.36(17)	6
5	LNOI	1700 nm	shadow-mask	N	N	0.09(6)	6
6	LNOS	1850 nm	shadow-mask	N	Y	0.11(7)	13
7	LNOS	1700 nm	lift-off-resist	N	N	0.13(14)	3
8	LNOS	400 nm	lift-off-resist	N	N	0.42(16)	3



Supplementary Fig. 2: **Phonon lifetime versus external coupling lifetime for different fabrication flows.** Each point represents an individual resonator measured at large intracavity phonon number $\bar{n} \gg 1$. Measurements are grouped according to shared fabrication flows, with red, cyan, blue, orange and yellow data points corresponding to Supplementary Table 1 variants 1–3, 4, 5, 6, and 7–8 respectively.

SUPPLEMENTARY REFERENCES

- [1] Tung, B. T., Watanabe, N., Kato, F., Kikuchi, K. & Aoyagi, M. Flip-chip bonding alignment accuracy enhancement using self-aligned interconnection elements to realize low-temperature construction of ultrafine-pitch copper bump interconnections. In *2014 IEEE 64th Electronic Components and Technology Conference (ECTC)* 62–67 (2014).
- [2] Bui, T. T. *et al.* High-precision heterogeneous integration based on flip-chip bonding using misalignment self-correction elements. In *2012 International Conference on Optical MEMS and Nanophotonics* 93–94 (2012).
- [3] Tiggelaar, R. M. *et al.* Spreading of thin-film metal patterns deposited on nonplanar surfaces using a shadow mask micromachined in Si (110). *J. Vac. Sci. Technol. B* **25**, 1207–1216 (2007).