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SUPPLEMENTARY INFORMATION

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Scalable energy-efficient magnetoelectric spin–orbit logic

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SI Guide

A. **Switching logic states of MESO:** Two operating states of MESO are described. The electric field of the ME ($\mathbf{E_{ME}}$), Effective switching field from the magneto-electric effect ($\mathbf{H_{ME}}$), Direction of the injected spin ($\boldsymbol{\sigma}$) and topologically generated charge current ($\mathbf{I_c}$) are reversed for the two states of the switch. The power supply remains uni-polar.

B. **Vector Spin Circuit Modeling of MESO Logic:** We verify the functionality of MESO spin logic using an equivalent spin circuit model, which comprehends magnetization dynamics of the nanomagnet, stochastic nature of switching, vector spin injection, spin to charge transduction and the magneto-electric switching.

C. **Magnetization dynamics and stochastic behavior:** We modeled the magnetization dynamics of the nanomagnet using two complementary approaches: a) Landau-Lifshitz-Gilbert (LLG) equation for the average magnetization dynamics affected by thermal noise; b) Fokker-Planck equation to determine the probability distribution of the stochastic part of magnetization.

D. **Logic Error Rates using Fokker-Planck equation:** To study and compare the logic error rates (Figure 4D of main manuscript), we use Fokker-Planck equation governing the probability of the direction of the magnetic moment.

E. **Simulation Comparison of Spin Torque Logic and MESO Logic:** We compared the MESO logic with All Spin Logic (ASL) using vector spin circuit modeling.

F. **Benchmarking to beyond CMOS logic options:** We adopted the benchmarking methodology for digital logic, applied to circuit such as a fanout-4 inverter, a 2-input NAND, and a 32-bit ripple-carry adders to compare the MESO logic with leading beyond CMOS logic options.

G. **Energy calculation and scaling for MESO logic device :** The switching energy (E_{MESO}) of a Magnetoelectric Spin-Orbit (MESO) logic device is composed of the sum of all the dissipation

sources and energy storage: energy stored in the magnetoelectric ferroelectric (FE) (E_{CME}), dissipation in the interconnect (E_{IC}), dissipation in the spin to charge conversion layer (E_{ISOC}), dissipation in the power supply transistor (E_{RT}), dissipation in the supply and ground paths (E_{SG}).

H. **MESO parameters and benchmarks:** Here we provide a detailed MESO switching energy calculation following the methodology of beyond-CMOS benchmarking .

I. **SPICE simulation of the charge circuit with equivalent ferroelectric model :** We validated our assumptions of the charge transport in the MESO device via a SPICE circuit simulation solver using compact model that includes the physics of the ferroelectrics and the spin to charge conversion

J. **Scaled MESO switching operation comprising all parasitic effects :** We further show the SPICE simulation for a sub 10 aJ switching operation of a MESO logic device comprehending: a) Energy stored in C_{me} b) Energy dissipation in the Interconnect-R_{IC}; c) Energy dissipation in the Rashba source's resistance R_{isoc}; d) Supply resistor losses.

K. **MESO energy and energy scaling measured in circuit simulation:** We performed the parameter analysis of C_{FE} in circuit simulation with scaling of the ferroelectric charge from 320aC to 32aC without changing the other MESO circuit parameters.

L. **Bidirectional, logic "0" to "1" and "1" to "0" switching in cascaded MESO devices:** The circuit simulation of the cascaded MESO devices for combinatorial operation is shown.

M. **Requirements for the resistivity of the spin-orbit coupling materials - Note on internal resistance of ISOC current controlled current source.**

N. **Interconnect modeling for MESO**

O. **Stochasticity (Dynamic switching error) of magneto-electric switching logic**

P. **Spin-orbit transduction devices: Experimental proto-device nanofabrication and details.**

Q. **Magnetoelectric coupling devices: Growth and materials properties, Electrical measurement of the ME devices.**

Supplementary Materials

Magnetoelectric Spin-Orbit Logic with Non-volatility and Energy Efficiency

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A. Switching logic states of MESO:

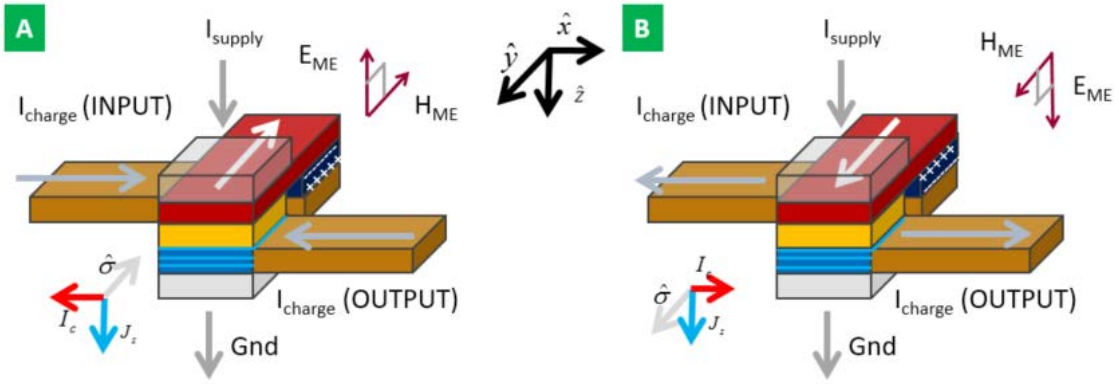


Figure S1. Two operating states of MESO. The electric field of the ME ($\mathbf{E_{ME}}$), Effective switching field from the magneto-electric effect ($\mathbf{H_{ME}}$), Direction of the injected spin ($\boldsymbol{\sigma}$) and topologically generated charge current ($\mathbf{I_c}$) are reversed for the two states of the switch. The power supply remains uni-polar.

B. Vector Spin Circuit Modeling of MESO Logic:

We verify the functionality of MESO spin logic using an equivalent spin circuit model, which comprehends magnetization dynamics of the nanomagnet, stochastic nature of switching, vector spin injection, spin to charge transduction and the magneto-electric switching. The equivalent circuit model is based on vector spin circuit theory [S1-4] (magneto-electric circuit analysis).

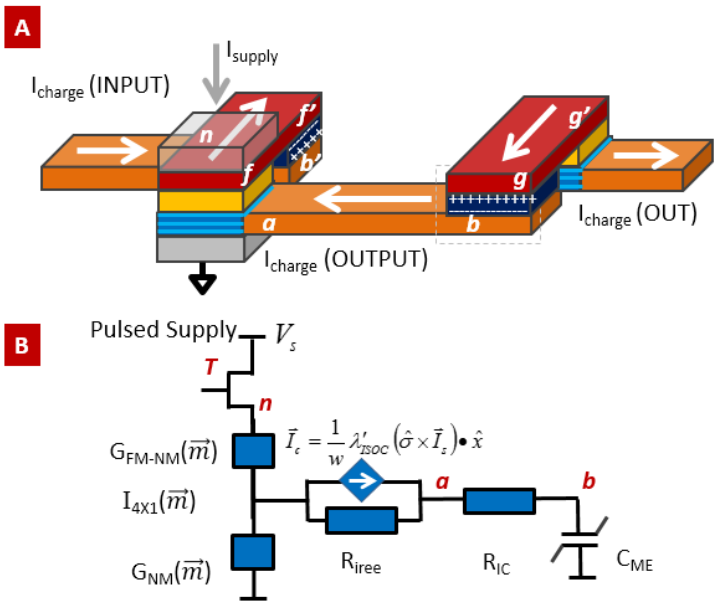


Figure S2. Vector Spin Equivalent Model for MESO Logic device. A. Physical scheme. B. Circuit schematics.

In figure S2, the node labels of the MESO circuit schematics correspond to the equivalent points in the physical scheme of the device. **ab** is a charge interconnect connecting two stages of MESO devices, where ***a*** is the node at the output terminal of the ISOC current source, ***b*** is the node at the terminal of the magneto-electric capacitor. ***FF'*** represents the ferromagnet (FM). The ferromagnet is adjacent to a magneto-electric capacitor **F'b'**. The spin to charge conversion layer is represented by a current controlled current source and an internal shunt resistance. Drive transistor (**T**) is connected to the FM to provide supply voltage. The pulse of current through the transistor is conducted to the ground terminal designated in the scheme by a triangle. Transistor (**T**) is shared among several MESO logic devices to provide supply voltage/current which plays the role of clocking. No logic signal is passed through these transistors. The ferroelectric capacitance of ***bg*** is designated C_{ME}. G_{FM} is the 4x4 matrix of spin conductance of the interface between FM and the spin injection layer. I_c is the equivalent current source

due to spin to charge conversion in the SOC layer with intrinsic source resistance. Interconnect resistance is designated R_{ic}.

The functional form of the spin matrices G_{FM} is obtained by using a Landauer-Büttiker formalism with spin transport [1, 5] applied to metallic circuits. The spin equivalent circuit modeling is described in [4]. The conductance matrix describing the spin transport across a ferromagnet (FM) to normal magnet (NM) interface is

$$\begin{bmatrix} I_c \\ I_{sx} \\ I_{sy} \\ I_{sz} \end{bmatrix} = \begin{bmatrix} G_{11} & \alpha(V_c)G_{11} & 0 & 0 \\ \alpha(V_c)G_{11} & G_{11} & 0 & 0 \\ 0 & 0 & G_{SL}(V_c) & G_{FL}(V_c) \\ 0 & 0 & -G_{FL}(V_c) & G_{SL}(V_c) \end{bmatrix} \begin{bmatrix} V_c \\ V_{sx} \\ V_{sy} \\ V_{sz} \end{bmatrix} \tag{S1}$$

where G_{11} is the interface conductivity (for each interface), $\alpha(V)$ is the spin polarization of current across the interface as a function of voltage, $G_{SL}(V_c)$ and $G_{FL}(V_c)$ are the Slonczewski and field like torque contributions to the spin current across the interface. The voltage dependence of spin polarization $\alpha(V)$, $G_{SL}(V)$, $G_{FL}(V)$ is determined by the detailed band structure of the electrode materials (see e.g. [6, 7]). The expressions for the elements of the 4x4 spin conduction matrix (A1) have first been derived in [1]. The above expression is valid in a coordinate system where the x-axis is aligned to the direction of magnetization. For an arbitrary direction $\hat{m}$ of magnetization, the spin conduction matrix is obtained by applying a rotation transform

$$G_{FN}(\hat{m}) = R(\hat{m})^{-1} G_{FN}(\hat{x}) R(\hat{m}) \tag{S2}$$

Where the rotation matrix

$$R(\hat{m}) = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & r_{22} & r_{23} & r_{24} \\ 0 & r_{32} & r_{33} & r_{33} \\ 0 & r_{42} & r_{43} & r_{44} \end{bmatrix} \quad \text{(S3)}$$

The elements of G_{FM} conductance can be related [1] to the ab-initio calculated reflection and transmission coefficients of the interface as follows

$$G^{\uparrow\uparrow} = \frac{e^2}{h} \sum_{m,n} \left| t_{\uparrow}^{nm} \right|^2 \quad \text{(S4)}$$

$$G^{\downarrow\downarrow} = \frac{e^2}{h} \sum_{m,n} \left| t_{\downarrow}^{nm} \right|^2 \quad \text{(S5)}$$

$$G^{\uparrow\downarrow} = G^{\downarrow\uparrow *} = \frac{e^2}{h} \sum_{n} \left(1 - \sum_{m} r_{\uparrow}^{nm} r_{\downarrow}^{nm *} \right) \quad \text{(S6)}$$

where e^2/h is the conductance per spin of a ballistic channel with ideal contacts [1]; $t_{\downarrow}^{nm}, t_{\uparrow}^{nm}$ are the transmission coefficients for majority and minority spin electrons; $r_{\uparrow}^{nm}, r_{\downarrow}^{nm}$ are the reflection coefficients of the majority and minority spin electrons; *n* is the index of modes in the non-magnetic material, and *m* is the index of modes in the ferromagnet. From the above expressions we note relations

$$G_{SL} = G_{11} + \frac{e^2}{h} \sum_{m,n} \left| r_{\uparrow}^{nm} - r_{\downarrow}^{nm *} \right|^2 \quad \text{(S7)}$$

$$G_{FL} = -i \frac{e^2}{h} \sum_{m,n} \left(r_{\uparrow}^{nm} r_{\downarrow}^{nm *} - r_{\uparrow}^{nm *} r_{\downarrow}^{nm} \right) \quad \text{(S8)}$$

The functional form of the spin to charge conversion is simulated using a spin controlled current source (SCCS) modeled as a current source with open circuit resistance (G_s)

$$I_{c\,\mathrm{int}} = \frac{1}{w}\left(\lambda_{IREE} + \Theta_{SHE}\lambda_{sf}\,\tanh\left(\frac{t}{2\lambda_{sf}}\right)\right)\left(\hat{\sigma}\times\vec{I}_s\right)\bullet\,\hat{y} \qquad \text{(S9)}$$

The bulk spin Hall coefficient may be enhanced by the use of a super-lattice of high spin orbit materials [9]. The interconnect resistance R_{ic} and C_{ic} are modeled by the following Mayadas- Shatzkes (MS) scaling law [10]

$$\rho = \rho_0\left(1 + \frac{3\lambda_{ebulk}}{8t}\left(1+\frac{p}{2}\right) + \frac{3\lambda_{ebulk}}{2D}\left(\frac{R}{1-R}\right)\right) \qquad \text{(S10)}$$

Where ρ_0 is bulk resistivity, λ_{ebulk} is the electron mean free path, p, R are specularity, reflection parameter from grain boundaries) as critical interconnect dimensions approach electron mean free path. We assume that $\lambda_{ebulk} = p = R$. We also include the interconnect capacitance of the charge interconnect BC.

C. Magnetization dynamics and stochastic behavior

We modeled the magnetization dynamics of the nanomagnet using two complementary approaches: a) Landau-Lifshitz-Gilbert (LLG) equation [11] for the average magnetization dynamics affected by thermal noise; b) Fokker-Planck equation [12, 13] to determine the probability distribution of the stochastic part of magnetization. The phenomenological LLG equation describing the dynamics of nanomagnet with a magnetic moment unit vector ($\hat{\mathrm{m}}$), modified with spin transfer torques is (see Table S1 for parameters) $\frac{\partial\hat{m}}{\partial t} = -\gamma\mu_0[\hat{m}\times\overline{H}_{eff}] + -\gamma\mu_0[\hat{m}\times\overline{H}_{exc}] + \alpha\left[\hat{m}\times\frac{\partial m}{\partial t}\right] + \frac{\vec{I}_{\perp}}{eN_s}$

(S11)

where γ is the electron gyromagnetic ratio; μ_0 is the free space permeability; $\vec{H}_{eff}$ is the effective magnetic field due to the combination of material, shape, and surface anisotropy; α is the Gilbert damping and $\vec{I}_{\perp}$ is the component of spin polarization perpendicular to the magnetization ($\hat{m}$) in the current exiting the nanomagnet, N_s is the total number of Bohr magnetons per magnet. $\vec{I}_{\perp}$ can be equivalently rewritten as $\vec{I}_{\perp} = \vec{I}_s - \hat{m}(\hat{m}.\vec{I}_s) = \hat{m} \times (\vec{I}_s \times \hat{m})$. The dynamics of nanomagnets is strongly affected by the thermal noise [14]. The thermal noise can be considered a result of microscopic degrees of freedom of the conduction electrons and the crystal lattice of the ferromagnet. At room temperature T, the thermal noise is described by a Gaussian white noise (with a time domain Dirac-delta auto-correlation). The noise field acts isotropically on the magnet. The internal field in (S12) is:

$$\overline{H}_{eff}(T) = \overline{H}_{eff} + (H_i\hat{x} + H_j\hat{y} + H_k\hat{z}) \qquad \text{(S12)}$$

$$\langle H_l(t) \rangle = 0 \qquad \text{(S13)}$$

$$\langle H_l(t)H_k(t') \rangle = \frac{2\alpha k_B T}{\mu_0^2 \gamma M_s V}\delta(t-t')\delta_{lk} \qquad \text{(S14)}$$

The initial conditions of the magnets should also be randomized to be consistent with the distribution of initial angles of magnet moments in a large collection of magnets.

At temperature T, the initial angle of the magnets follows:

$$\langle \theta^2 \rangle = \frac{kT}{M_s V \mu_0 H_{ani}} \qquad \text{(S15)}$$

We used a mid-point integration method [15, 16] to apply the Stratonovich calculus while integrating the LLG equation. The discretized integration rule is

$$y_{n+1} = y_n + \Delta t.f\left(t_n + \Delta t/2, y_n + \Delta t/2.f\left(t_n, y_n\right)\right) \quad \text{(S16)}$$

Where $y = d\hat{m}/dt$. The variance of the noise varies depending on the time step size. The discretization was performed internally using an implicit self-consistent solver.

D. Logic Error Rates using Fokker-Planck equation

To study and compare the logic error rates (Figure 4D of main manuscript), we use Fokker-Planck equation governing the probability of the direction of the magnetic moment [12, 13, 17],

$$\frac{\partial \rho(\theta,\tau)}{\partial t} = -\nabla.J(\theta,\tau) = -\frac{1}{\sin\theta}\frac{\partial}{\partial\theta}\left[\sin\theta J_\theta(\theta,\tau)\right] \quad \text{(S17)}$$

Which relates the rate of change of probability density $\rho(\theta,\tau)$ at a given angle to the net rate of probability density flow. $J_\theta(\theta,\tau)$ is the flow of probability given by drift and diffusion components

$$J_\theta(\theta,\tau) = \rho(\theta,\tau)\frac{\partial\theta}{\partial\tau} - D\frac{\partial\rho(\theta,\tau)}{\partial\tau} \quad \text{(S18)}$$

The flow term $\frac{\partial\theta}{\partial\tau} = \left(i - h - \cos\theta\right)\sin\theta$ where $i = I/I_c$, $h = H/H_{kc}$ are the current and field driving terms for the probability, D=1/2Δ is the diffusion constant given by the thermal barrier of the magnet. For completeness, we have compared the Fokker-Planck models with Monte Carlo simulations of the magnetization from (A12).

E. Simulation Comparison of Spin Torque Logic and MESO Logic

We compared the MESO logic with All Spin Logic (ASL) [18] using vector spin circuit modeling. All spin logic operates by injection of spin currents into the spin channels and the detection by spin torque. The assumed equivalent models for ASL devices are shown in figure S3. G_{FM1} and G_{FM2} are vector spin conductances describing the spin injection from the magnets to the spin channel. The spin conduction conductances G_{seT}, G_{sfT} describe the conduction through the spin channel. We represent the metallic spin channel between node 1 and 2 as a combination of two T-equivalent circuits. The conductance G_{sfT} models the loss of spin current due to spin flip in the channel. The nanomagnet conductance is modeled by the spin conductance tensors $G_{FM1}(\hat{m}_1)$, $G_{FM2}(\hat{m}_2)$. The dynamics of the spin device are solved self-consistently with the spin transport in the equivalent circuit models. Please see [4, 19] for more details on the methodology.

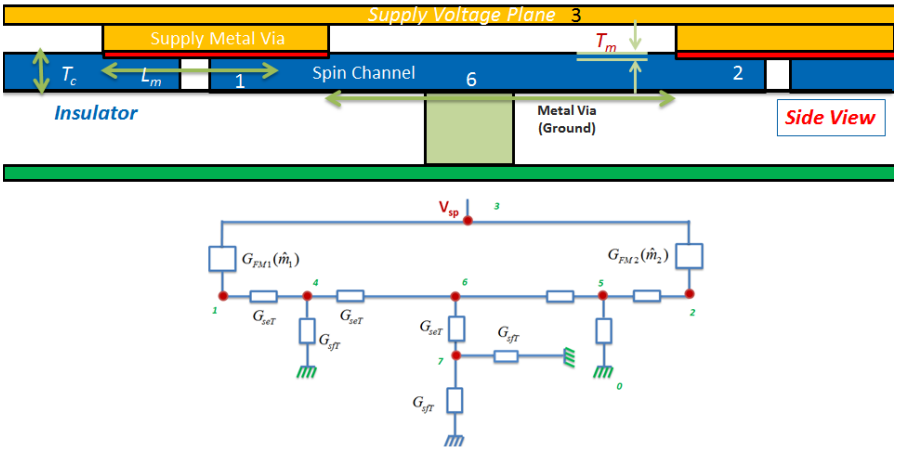


Figure S3. Benchmark All Spin Logic device and vector spin circuit model

To benchmark the MESO device with ASL device, we considered two material systems: a) All Spin logic with perpendicular magnetic anisotropy (ASL-PMA) and perpendicular spin currents; b) All Spin logic with Heusler alloy PMA magnets (ASL-Heusler). The gate

level energy delay of ASL-PMA and ASL-Heusler are 170 aJ·ns and 10 aJ·ns respectively [19].

Table 1. Nanomagnet and transport parameters used for Spin torque logic			
Variable	**Notation**	**Value/Typical Value**	**Units (SI)**
Free Space Permeability	μ_0	$4\pi x10^{-7}$	$JA^{-2}m^{-1}$
Gyromagnetic ratio	γ	$17.6x10^{10}$	$s^{-1}T^{-1}$
Saturation Magnetization of the Magnet	M_s	10^6	A/m
Damping of the Magnet	α	0.007	-
Effective Internal Anisotropy Field	H_{eff}	$3.06x10^4$	A/m
Barrier of the magnet	Δ/kT	40	
Number of spins	N_s	10^3 -10^6	-
Thickness of Magnet	T_m	3	nm
Magnet Dimensions	W_m	37.8X75.7	nm
Length of channel	L_c	100	nm
Thickness of channel	T_c	200	nm
Length of ground lead	L_g	200	nm
Thickness of ground lead	T_g	100	nm
Channel conductivity	ρ	$7x10^{-9}$	Ω.m
Sharvin conductivity	G_{sh}	$0.5x10^{15}$	$\Omega^{-1}.m^{-2}$
Polarization	α_c	0.8	

For scaling the ASL devices, we assume the use of perpendicular anisotropy and Heusler

alloys. The effect of scaling up the anisotropy field while reducing the saturation magnetization of the nanomagnets by the same factor allows strong improvement in ASL performance. The nanomagnet volume and the effective thermal energy barrier remain constant. A factor of 4 scaling of Ms and H_k from the benchmark material (CoFeB) shows that the energy-delay product can reach 10 aJ·ns.

F. Benchmarking to beyond CMOS logic options

We adopted the benchmarking methodology [20, 21] for digital logic, applied to circuit such as a fanout-4 inverter, a 2-input NAND, and a 32-bit ripple-carry adders to compare the MESO logic with leading beyond CMOS logic options. Circuit layout of the terminal signals signal impacts the switching time/delay and energy. A detailed description of the layout assumptions (following the constraints of advanced lithography) are described in [20].

Numerical values in this study are obtained for the technology with the Dynamic Random Access Memory (DRAM) metal half-pitch F=15nm [22]. It is a measure of the semiconductor process's minimum critical dimension. Spintronic circuits are more compact due to the use of majority gates. Switching delay and energy of electronic devices are calculated according to well-known estimates for a capacitor charging. Switching estimates of a spintronic intrinsic element depends on the mechanism of switching: a) spin torque (for STT-DW: Spin Transfer Torque Domain Wall logic, ASLD: All Spin Logic Device, CSL: Charge Spin Logic, STO logic: Spin Torque Oscillator logic) b) dipole field (for NML, Nano-Magnetic Logic) c) magneto-electric (MESO, SMG: Spin Majority Gate logic, SWD: Spin Wave Device).

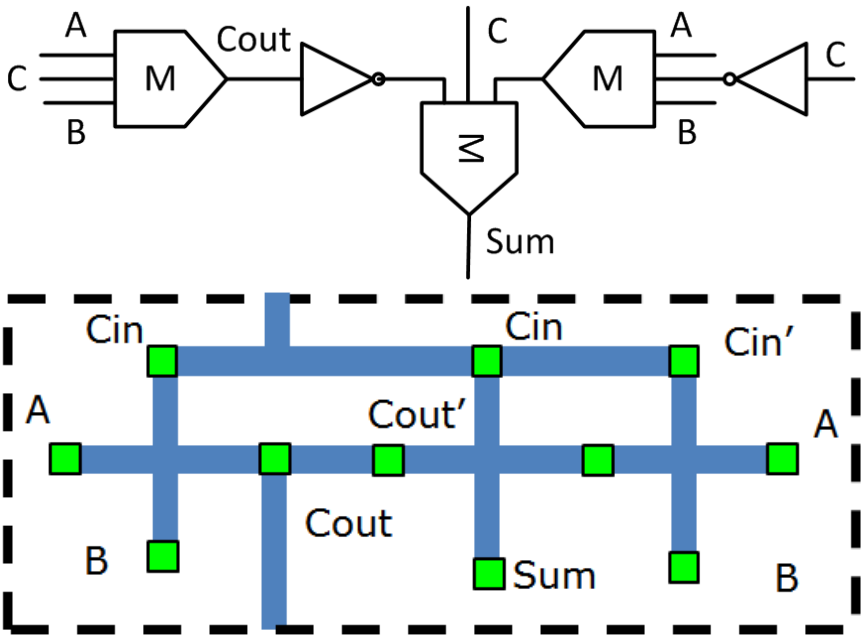


Figure S4. Circuit schematics and layout of the benchmark circuit, a 32-bit adder (one bit cell of the adder is shown).

To estimate the energy and the delay of the spin torque devices, we use the critical current $I_c = e\alpha\mu_0 M_s^2 v_{nm} / (\hbar P)$, the switching time $t_{stt} = eM_s v_{nm} L_f / (2g\mu_B P I_c)$, and the switching energy is $E_{stt} = 3I_c V_{dd} t_{stt}$. For devices switched by the magnetoelectric effect, the charging energy for a ME capacitor is $E_{me} = Q_{me} V_{dd}$, the magnetic switching time is limited by the ME field $t_{mag} = \pi / 2\gamma B_{me}$. Electronics is limited in supply voltage of 0.1 to 0.7V, while spintronics permits operation at 10 to 100mV, with the disadvantage of slower switching time. Both electronic and spintronic circuits need metal wires and contacts at the terminals of their gates. Switching time and energy of the intrinsic devices (transistors or nanomagnets), considering their parasitic as well as interconnects [23], are shown in figure 10.

G. Energy calculation and scaling for MESO logic device

The switching energy (E_{MESO}) of a Magnetoelectric Spin-Orbit (MESO) logic device is composed of the sum of all the dissipation sources and energy storage: energy stored in the magnetoelectric ferroelectric (FE) (E_{CME}), dissipation in the interconnect (E_{IC}), dissipation in the spin to charge conversion layer (E_{ISOC}), dissipation in the power supply transistor (E_{RT}), dissipation in the supply and ground paths (E_{SG}).

$$E_{MESO} = E_{CME} + E_{IC} + E_{ISOC} + E_{RT} + E_{SG} \quad \text{(S19)}$$

G.1. Equivalent charge circuit model for MESO logic device for energy calculation

MESO logic device comprises: a) magnetoelectric capacitor for voltage controlled switching of a ferromagnet (FM); b) a spin to charge conversion layer for charge readout of the magnetic state of the FM; and c) a charge interconnect connecting the MESO devices. An equivalent lumped element charge circuit model to capture the functioning of the MESO device is shown in Figure S5. Nodes a and b represent the two ends of the

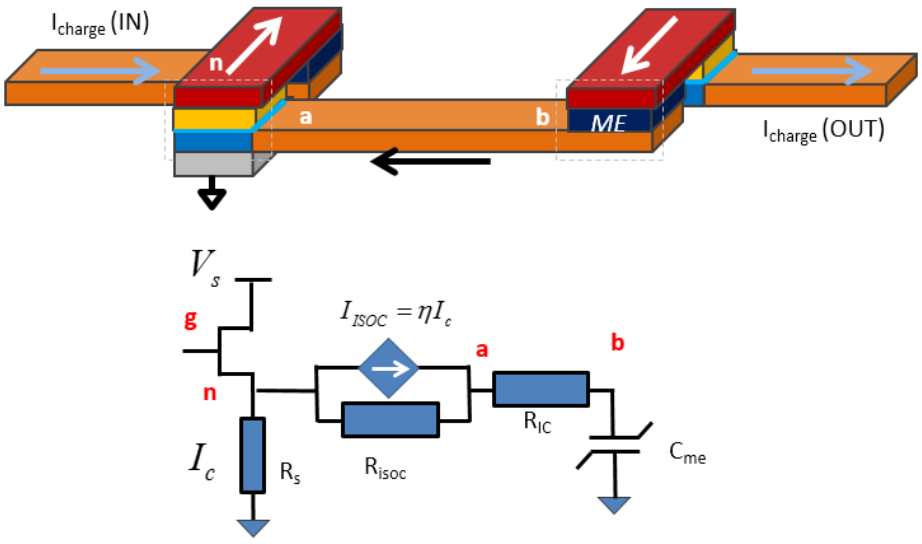


Figure S5. **(Charge equivalent circuit for MESO)** MESO device comprising a magnetoelectric (ME) switchable capacitor representing the MESO input loading combined with a spin to charge transduction mechanism for the MESO magnetic state

read-out. The spin to charge conversion is modeled as a current controlled current source with an internal resistance R_{ISOC}, the charge dynamics of the ME are modeled with a ferroelectric capacitor. R_{ic} is the interconnect resistance forming the charge interconnect ab. η is net spin to charge current conversion ratio.

charge interconnect with interconnect resistance (R_{ic}). The spin to charge conversion element formed with inverse spin-orbit coupling (ISOC) materials is shown between node ***n*** and ***a.*** The ISOC module is modeled as a current controlled current source (CCCS) with an internal parallel resistance (R_{isoc}) [24, 25]. The charge dynamics of the magnetoelectric node are modeled via a ferroelectric capacitance (C_{me}) [26]. We present both an analytical expression for the total energy of a state transition of MESO, including the sum of all the dissipation and storage sources viz. energy stored in the ferroelectric (magnetoelectric), dissipation in the interconnect, dissipation in the supply-ground path, dissipation in the power supply transistor. We provide an analytical derivation of the transition energy, and support this with time-domain circuit simulations using a self-consistent ferroelectric compact model. The equivalent charge circuit is applicable for calculating the energy due to charge dynamics and does not capture the vector spin dynamics.

The explanation for the total energy of MESO device is as follows: a) The energy to switch a capacitor and FE is independent of the interconnect resistance to the first order [24, 25] b) The current shunted in the spin to charge conversion current source depends on the equivalent source resistance (R_{ISOC}), which is material dependent parameter c) The losses in the parasitic paths are second order and device design can mitigate the energy losses extrinsic to magnetoelectric/ferroelectric switching. We also present an

example method for mitigating energy losses extrinsic to magnetoelectric switching via proper choice of supply-ground path resistance (R_s).

G.2. Energy calculation and scaling for MESO logic device

a. Switching energy of a capacitor/ferroelectric is independent of the interconnect resistance

We first note that the energy to switch a capacitor (or a fixed charge switchable device such as a ferroelectric) is independent of the interconnect resistance. For simplicity, we start with a linear dielectric capacitor. In the first stage it is switched from voltage 0 to voltage V through an interconnect of resistance of R by a voltage supply of V. We see that, the interconnect dissipated energy is independent of the interconnect resistance,

$$E_{Ohmic} = R\int_0^\infty i^2 dt = \frac{V^2}{R}\int_0^\infty e^{-2t/RC} dt = \frac{CV^2}{2} \qquad \text{(S20)}$$

The total energy supplied by the voltage source is given by

$$E_{\text{supply}} = V\int_0^\infty i dt = \frac{V^2}{R}\int_0^\infty e^{-t/RC} dt = CV^2 \qquad \text{(S21)}$$

So one half of it dissipated in the charging stage, according to S20, and the other half goes to the increase of energy of the capacitor. In the second stage, the voltage supply is removed, and the capacitor evolves from voltage V to voltage 0. In this stage the energy stored in the capacitor is dissipated in the resistor. Therefore, the overall energy dissipated in the charge-discharge cycle is equal to (S21).

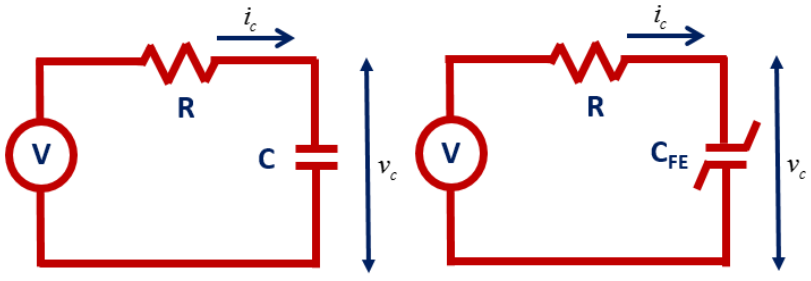


Figure S6. RC circuit to show that the interconnect resistance does not impact the total energy to switch a capacitor. Linear dielectric capacitor used in the schematic on the left, a ferroelectric capacitor is used in the schematic on the right.

The ferroelectric capacitor is treated somewhat differently. It starts with zero voltage but non-zero charge $-Q_{fe}$, corresponding to reversed spontaneous polarization $-P_{fe}$. It is then charged to voltage V and polarization P_{fe}. In the discharge stage, the voltage returns to zero, but there still remains the charge of Q_{fe}, corresponding to spontaneous polarization P_{fe}. The energy of the ferroelectric capacitor remains the same after the charge-discharge cycle. Similar to the linear dielectric capacitor, the total energy supplied by the voltage source to switch a ferroelectric is independent of the pulse shape of the current and is given by

$$E_{\text{supply}} = V\int_0^\infty idt = 2VQ_{fe} = C_{ME}V^2 \qquad \text{(S22)}$$

where we introduced the ferroelectric capacitance C_{me}. Hence, the Ohmic losses in switching a ferroelectric capacitor are only different from a linear capacitor by the factor of 2.

b. Switching energy of MESO

The total energy consumption of MESO can be written as sum of all the dissipation and storage sources Viz. energy stored in the FE, dissipation in the interconnect, dissipation in the supply-ground path, dissipation in the power supply transistor. We now consider two simplified equivalent models for the MESO for the energy consumption calculation comprising of the power supply (pulsed), Supply-ground path for spin to charge conversion, SOC current source, interconnect resistance and equivalent capacitance for

ME. Figure S7A shows the simplified equivalent circuit to derive an analytical expression. We convert the spin to charge conversion current source (a current controlled current source) to a voltage source using Thevenin equivalence in Fig.S7 B.

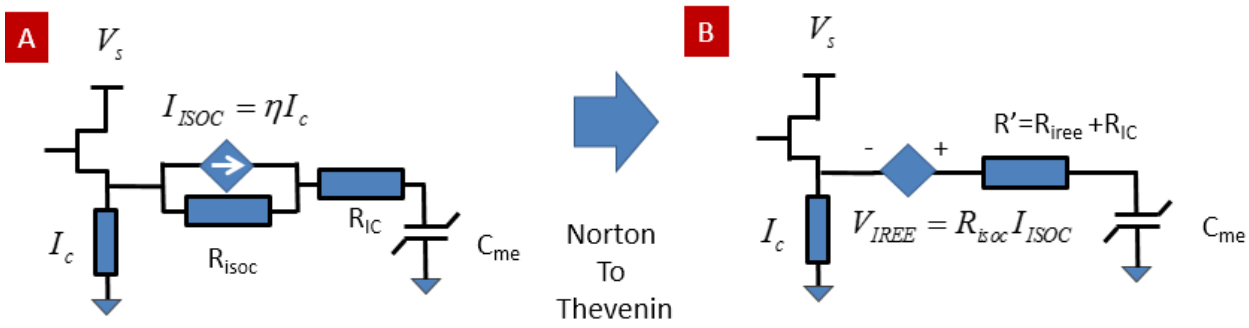


Figure S7. A) Equivalent circuit for MESO with current controlled current source B) Current controlled voltage source. We apply Norton to Thevenin conversion.

Energy to switch the FE and the interconnect losses: The total power dissipated in the interconnect resistance R_{ic} and the ISOC internal resistance R_{isoc} can be combined into R'. The power dissipated in the R_{ic}, R_{isoc} and stored in ME capacitor are given by:

$$E_{CME} + E_{IC} + E_{ISOC} = C_{me} V_{me}^2 \qquad \text{(S23)}$$

Joule losses occur in the resistances in the current delivery paths of the transistor and the resistive supply-ground path: The energy dissipated in the supply-ground path is given by

$$E_{SG} = \int_0^{\infty} i_{sh}^2 R_{sh} dt = i_{sh}^2 R_{sh} \frac{2Q}{I_c} = kC_{me} V_{me}^2 \frac{W}{\lambda} \qquad \text{(S24)}$$

Where we use the relation, $i_{sh} R_{sh} = kV_{me}$, $i_{sh}/i_c = W/\lambda$, $2Q = C_{me} V_{me}$. W is the width of the magnet and λ is the ISOC parameter. It can be further shown that, the energy dissipated in the transistor and supply-ground path is given by

$$E_{SG} + E_{RT} = \alpha C_{me} V_{me}^2 \frac{W}{\lambda} \quad \text{(S25)}$$

Where α is a circuit dependent function of transistor resistance, supply-ground path resistance.

The total energy of MESO can be written as

$$E_{MESO} = E_{CME} + E_{IC} + E_{ISOC} + E_{RT} + E_{SG} = C_{me} V_{me}^2 \left(1 + \alpha \frac{W}{\lambda}\right) \quad \text{(S26)}$$

H. MESO parameters and benchmarks

Here we provide a detailed MESO switching energy calculation following the methodology of beyond-CMOS benchmarking [20, 21]. As the reader will see, the estimates below are in approximate agreement with the rigorous SPICE simulations (Section G). For our estimates we assume the following material and device parameters (Table 2). The calculation of the circuit area is outside the scope of this section. The charge circuit model of MESO operation is shown in Figure S5. Even though CMOS auxiliary circuits play a crucial role in the operation of MESO, here we will not describe the performance of a CMOS transistor. For details please see [20, 21].

I. Magnetoelectric effect.

In order to achieve the magnetoelectric field necessary to switch a nanomagnet, the following electric field needs to be applied to the multiferroic $BiFeO_3$:

$$\mathrm{E}_r = \mathrm{E}_{mf} B_c / B_{mf} \,. \quad \text{(S27)}$$

(For the definition of terms in Eq. (3.1) see Table 2 below). The total charge at the terminals of the multiferroic capacitor comprises the saturated ferroelectric polarization

charge at the interface and the linear dielectric polarization in response to the applied electric field:

Table 2. Material and structure parameters serving as inputs into MESO estimates.

Quantity	Symbol	Units	Value
Characteristic critical dimension	F	m	1e-8
Copper wire resistivity	ρ_{Cu}	Ω*m	2.5e-7
Magnetization in a ferromagnet, perpendicular	M_{sp}	A/m	3e5
Thickness of ferromagnetic	t_{fm}	m	2e-9
Spin polarization from a ferromagnet	P_{fm}		0.7
Perpendicular magnetic anisotropy	K_u	J/m^3	6e5
Spin-orbit coupling effect coefficient	λ_{ISOC}	m	1.4e-8
Resistance*area of the FM and ISOC stack	r_{fm}	Ω.m^2	3e-14
Internal resistance of the ISOC current source	R_{isoc}	Ω	4000
Magnetoelectric field for switching nanomagnet	B_c	T	0.1
Multiferroic ferroelectric polarization (BFO)	P_{mf}	C/m^2	0.3
Multiferroic electric switching field	E_{mf}	V/m	1.8e6
Multiferroic exchange bias at switching field	B_{mf}	T	0.03
Dielectric constant of multiferroic	ε_{mf}		54
Thickness of multiferroic	t_{mf}	m	5e-9
Ferroelectric intrinsic switching time	τ_{fe}	s	2e-11
Lande factor	g		2

Gate voltage for the access transistor	V_x	V	0.73
On current for the access transistor	$\tilde{I}_x$	A/m	1648
Gate capacitance per unit width of the access transistor	c_g	F/m	1e-9
Resistance of a power or a ground distribution network	R_s	Ω	4000

$$Q_{me} = A_{me}\left(\varepsilon_0 \varepsilon_{mf} \mathrm{E}_r + P_{mf}\right). \quad \text{(S28)}$$

The voltage drop on the magnetoelectric element is

$$V_{me} = \mathrm{E}_r t_{mf} \ . \quad \text{(S29)}$$

The time to charge the multiferroic capacitor from 0 voltage to V_{me} is

$$\tau_{me} \approx 2Q_{me} / I_{ISOC}\,, \quad \text{(S30)}$$

Since the charge in the capacitor needs to be changed from $-Q_{me}$ to Q_{me}. Here I_{ISOC} is the current produced by the spin-orbit effect.

From the treatment below we will see that the capacitor charging time is limited also by the intrinsic switching time for the ferroelectric BFO to reverse polarization, τ_{fe}. However the magnetization is even slower to react to the applied exchange bias and takes optimistically the following time (optimistically) to complete the precession:

$$\tau_{mag} \approx \pi / \left(\gamma B_c\right). \quad \text{(S31)}$$

Where the gyromagnetic ratio is

$$\gamma = ge/(2m_e). \quad \text{(S32)}$$

The total time is obtained as the combination of the above two times:

$$\tau_{tot} = \tau_{me} + \tau_{mag}\,, \quad \text{(S33)}$$

Where the last term makes the dominant contribution. The capacitance of the magnetoelectric element is

$$C_{me} = Q_{me}/V_{me}\,, \quad \text{(S34)}$$

And the switching energy is

$$E_{me} = 2Q_{me}V_{me}\,. \quad \text{(S35)}$$

II. Spin-orbit coupling effect.

The power supply enable transistor provides current I_c traveling through the ferromagnet. This current is related to the supply voltage V_{sup} and the total resistance in the supply path.

$$V_s = I_c(R_T + R_{fm} + R_s) \equiv I_c R_{sum}\,. \quad \text{(S36)}$$

The enable transistor is in the linear regime. Its resistance is related to its width:

$$R_{ON} = r_L / w_x\,. \quad \text{(S37)}$$

This transistor width (w_x) is set by the objective to provide sufficient current to be converted by spin-orbit effect. The value of this width turns out to be smaller than a minimal transistor width. That means that one transistor can be shared to supply

current to several parallel MESO devices, or a longer than minimum transistor channel length is used.

The resistance across the ferromagnet and spin-orbit coupling stack in the supply path is:

$$R_{fm} = r_{fm} / A_{me} . \quad \text{(S38)}$$

We assume that the contact resistance is included in the definition of the I-V characteristic of the MOSFET. R_{ON} resistance is related to the on-current per unit width at the low source-to drain voltage and high gate to source voltage

$$r_L \approx V_x / \left(3\tilde{I}_x\right). \quad \text{(S39)}$$

The current extracts spin polarized current from the ferromagnet in the vertical direction

$$I_s = P_{fm} I_{\sup} . \quad \text{(S40)}$$

Inverse spin-orbit coupling effect (the combination of the bulk spin Hall effect and the interface Rashba-Edelstein effect) converts the spin polarized current into charge current in the charging path (horizontal direction) of the multiferroic capacitor of the next MESO gate with its sign determined by the direction of magnetization in the ferromagnet.

$$I_{ISOC} = \lambda_{ISOC} I_s / w_m , \quad \text{(S41)}$$

Where w_m is defined in table 1. This current source is related to the voltage it can produce, which must be equal to the magnetoelectric voltage:

$$V_{me} = I_{ISOC}\left(R_{ISOC} + R_{fe} + R_{ic}\right) = I_{ISOC}R_{tot}\ . \tag{S42}$$

The resistances in the charging path in the equation above are the ISOC current source internal resistance (longitudinal resistance of the thin ISOC layer), the resistance of the ferroelectric capacitor, and the interconnect resistance. The resistance of the ferroelectric capacitor is caused by damping in the ferroelectric and is related to the ferroelectric intrinsic switching time

$$R_{fe} = \tau_{fe} / C_{me}\ . \tag{S43}$$

The ISOC current source needs to be active over time τ_{me}, necessary to charge the magnetoelectric capacitor. Thus energy dissipated in the vertical, supply path of the circuit is given by Joule power dissipation as:

$$E_{\text{sup}} = V_s I_c \tau_{me}\ . \tag{S44}$$

We can show that

$$E_{\text{sup}} = V_{\text{sup}} Q \frac{w_m}{P_{fm}\lambda_{IREE}}\ . \tag{S45}$$

Table 3. Operating parameters of MESO devices.

Quantity	Symbol	Units	Value
Metal wire pitch (=4F)	p_m	m	4e-8
Supply voltage	V_s	V	0.1
Access transistor width	w_x	m	2e-9

Resistance per width of the access transistor in the linear regime	r_L	Ω/m	1.48e-4
Total resistance in the supply path	R_{sum}	Ω	2.5e4
Characteristic interconnect length (=10p_m)	l_{ic}	m	4e-7
Capacitance of a characteristic interconnect	C_{ic}	F	3.7e-17
Resistance of a characteristic interconnect	R_{ic}	Ω	1e3
Width of the magnet (=F)	w_m	m	1e-8
Magnetoelectric switching area (=F^2)	A_{me}	m^2	1e-16
Magnetoelectric voltage	V_{me}	V	0.03
Switching time for the magnetoelectric capacitor	τ_{me}	s	5e-11
Effective magnetoelectric capacitance	C_{me}	F	1e-15
Resistance of the ferroelectric capacitor	R_{fe}	Ω	1e4
Total resistance in the charging path	R_{tot}	Ω	1.8e4
Switching time for magnetization	τ_{mag}	s	2e-10
Current in the supply path	I_c	A	1.2e-6
Current generated by the ISOC effect	I_{ISOC}	A	1.2e-6
Energy of magnetoelectric capacitor	E_{me}	J	1.8e-18
Energy dissipation in the supply path	$E_{\sup}$	J	6.4e-18
Energy to charge the access transistor	E_{ga}	J	1.1e-18

Thus this contribution into energy dissipation is related to the energy of the magnetoelectric capacitor too. Together the energy loss in the C_{me} charging/discharging and supply paths is

$$E_{MESO} = E_{me}\left(1+\frac{w_m}{P_{fm}\lambda_{IREE}}\frac{V_s}{V_{me}}\right). \quad \text{(S46)}$$

An additional energy loss comes from charging the gate of the power supply gating transistor

$$E_{ga} = w_x c_g V_x^2. \quad \text{(S47)}$$

III. MESO switching performance.

For a characteristic interconnect between MESO elements, the switching time is calculated according [20, 21, 27]:

$$t_{ic} \approx 0.38R_{ic}C_{ic} + 0.7R_{on}C_{ic} + 0.7R_{ic}C_L, \quad \text{(S48)}$$

as well as the interconnect switching energy:

$$E_{ic} \approx C_{ic}V_{me}{}^2. \quad \text{(S49)}$$

Here one needs to substitute for the load capacitance $C_L = C_{me}$ and for the on-state resistance $R_{on} = \left(R_{ISOC} + R_{ic}\right)$. The total delay time of an intrinsic device (not including the interconnect) is

$$t_{\text{int}} \approx \tau_{tot}, \quad \text{(S50)}$$

The intrinsic device in our case means 'one MESO element'. The way we calculate the performance of more complicated circuits, such as a 32-bit adder and an ALU, follows [20, 21]. Energy dissipation in the charging path of the circuit, is not a separate

contribution to switching energy. It is equal to the energy accumulated in the magnetoelectric capacitor and just represents the way this energy is dissipated each time the voltage is turned on or off (see Section F for the explanation).

Thus the total intrinsic device switching energy is composed of

$$E_{\text{int}} = E_{me} + E_{\text{sup}} + E_{ga} . \quad \text{(S51)}$$

The results of the calculation following the method of [27] are summarized in Table 4.

Table 4. Resulting performance of MESO devices and circuits.

Quantity	Symbol	Units	Value
Area of the intrinsic device	a_{int}	m^2	1.4e-14
Switching time of the intrinsic device	t_{int}	s	2.3e-10
Switching energy of the intrinsic device	E_{int}	J	9.3e-18
Switching time of the interconnect	t_{ic}	s	2.9e-12
Switching energy of the interconnect	E_{ic}	J	1.8e-19
Area of 1 bit of a full adder	a_1	m^2	8.6e-14
Switching time of 1 bit of a full adder	t_1	s	2.4e-10
Switching energy of 1 bit of a full adder	E_1	J	1.3e-16

I. SPICE simulation of the charge circuit with equivalent ferroelectric model

We validated our assumptions of the charge transport in the MESO device via a SPICE circuit simulation solver using compact model that includes the physics of the ferroelectrics and the spin to charge conversion.

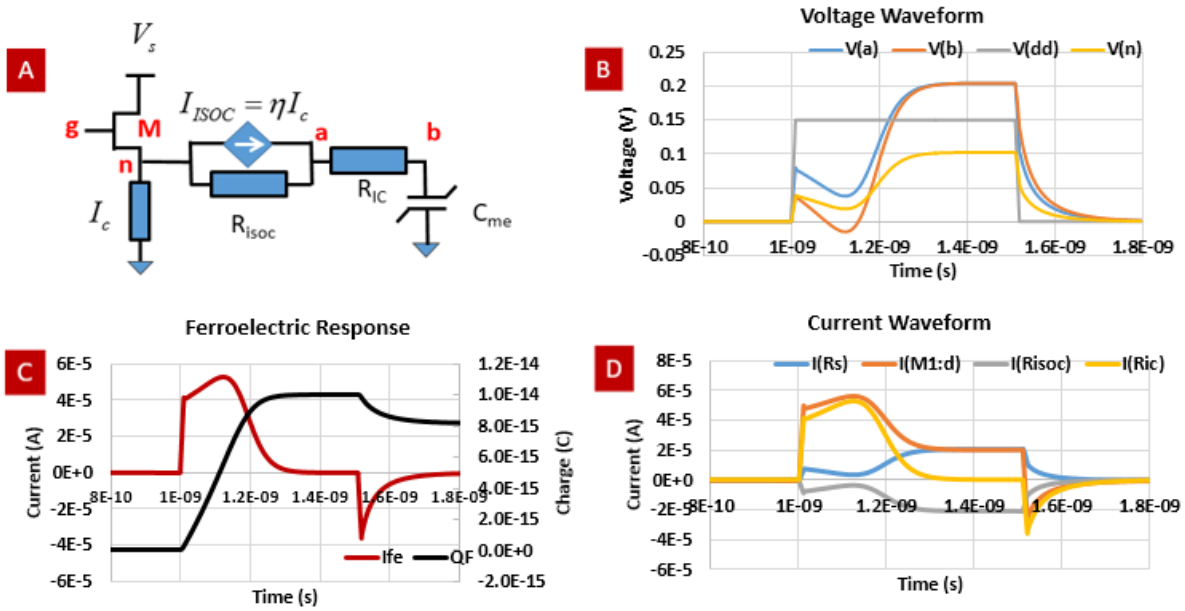


Figure S8. SPICE Simulation of MESO showing the self-consistent charge dynamics of the MESO device **(for clarity of transient waveforms we simulated a 8 fC stored ferroelectric charge which is significantly higher than a scaled MESO logic device)** (A) Charge circuit model for MESO with ISOC current controlled current source and ME capacitor modeled with Landau-Khalatnikov equations B)Voltages applied/measured at supply transistor gate (**V(dd)**), magnetoelectric capacitor (**V(b)**), interconnect (**V(a)**) and the transistor terminal (**V(n)**) C) Current and charge across FE capacitor D) Currents measured through ISOC internal resistance (R_{isoc}), supply resistance (R_s), supply transistor (M) & interconnect resistance (R_{IC}) (Pulse width=500ps, R_{isoc}=R_s=5k, Vdd=150mV (clk), Vg=1V (dc))

We model the ferroelectric switching dynamics of the magnetoelectric using the Landau-Khalatnikov (LK) equation [26]:

$$\rho \frac{dQ_F}{dt} = -\frac{dU}{dQ_F} = -\left(2\alpha Q_F^1 + 4\beta Q_F^3 + 6\gamma Q_F^5 - V_F\right) \qquad \text{(S52)}$$

Where Q_F is the ferroelectric polarization, ρ internal equivalent resistance (damping term) of the ferroelectric, U is the energy density per unit area, α, β, γ are the rescaled internal anisotropy constants of the FE (figure S8). The ferroelectric switching exhibits a non-linear equivalent capacitance during the charging and discharging of the ferroelectric.

$$C_F\left(Q_F\right)=\left(2\alpha+4\beta Q_F^2+6\gamma Q_F^4\right)^{-1} \tag{S53}$$

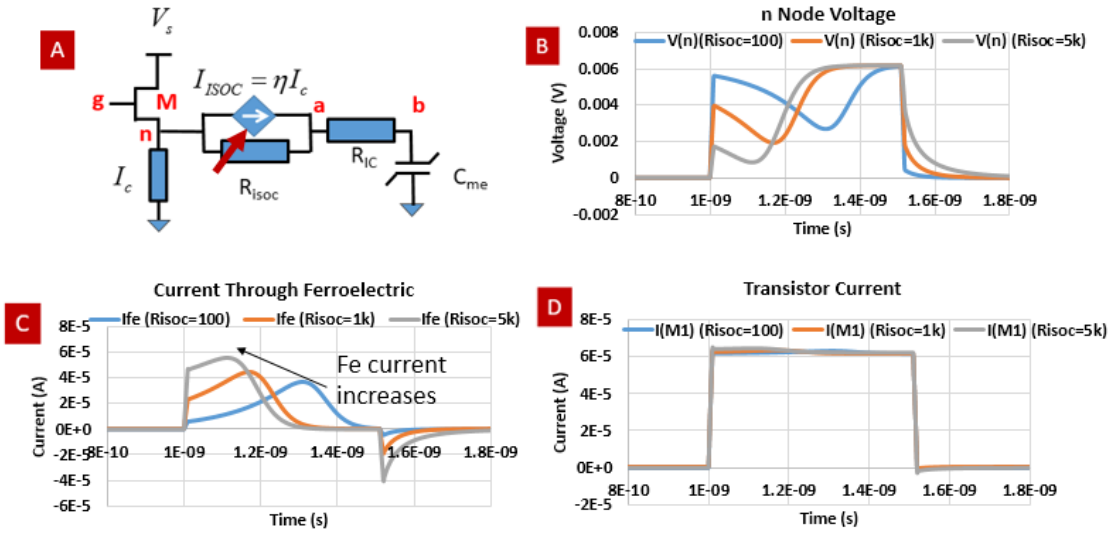


Figure S9. **(Impact of ISOC internal current source resistance) (Impact of ISOC source resistance) (For clarity of transient waveforms we simulated an 8 fC stored ferroelectric charge which is significantly higher than a scaled MESO logic device)** SPICE Simulation of MESO showing the self-consistent charge dynamics of the MESO device B) Node voltage at n1 at varying values of R_{isoc} (100 Ω, 1kΩ, 5kΩ) C) Ferroelectric node current (Sweep R_{isoc}, Pulse width=500ps, R_s=100, Vdd=150mV, Vg=1V). D) Transistor current at varying values of R_{isoc} (100 Ω, 1kΩ, 5kΩ) For high ISOC resistance FE node current approaches the transistor current for high spin to charge conversion ratio.

We show the impact of the ISOC internal resistance and in particular show that interconnect current is close to the supply current for high internal resistance SOC materials. The currents measured through the various branches show that ISOC generated charge current is shared between the internal shunt path resistance and the

interconnect resistance. The extent of shunting via internal resistance depends on the resistivity of the ISOC material (Figure S9).

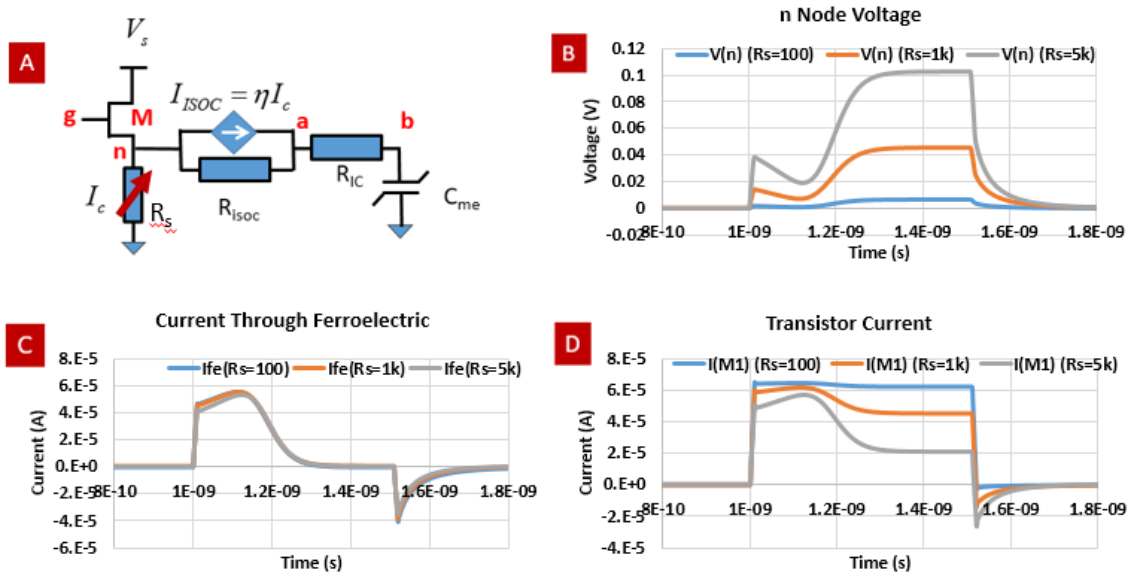


Figure S10. **(Impact of R_s, Supply Resistance) (For clarity of transient waveforms we simulated an 8 fC stored ferroelectric charge which is significantly higher than a scaled MESO logic device)** A) SPICE Simulation of MESO showing the impact of R_s, supply resistance B) Node voltage at n at varying R_s (100 Ω, 1kΩ, 5kΩ) C) Ferro-electric/Interconnect current through R_{IC} D) Transistor current at varying R_s (100 Ω, 1kΩ, 5kΩ) (Sweep R_s, Pulse width=500ps, Risoc=5k, Vdd=150mV (clk), Vg=1V(dc))

We study the impact of the supply resistor (R_s) on the switching dynamics of MESO. We show that the impact of supply path current (i.e., current through the resistor R_s) can be mitigated by a higher impedance without impacting the interconnect current and the switching dynamics of the ferroelectric (Figure S10).

J. Scaled MESO switching operation comprising all parasitic effects.

We further show the SPICE simulation for a sub 10 aJ switching operation of a MESO logic device comprehending: a) Energy stored in C_{me} b) Energy dissipation in the

Interconnect-R_{IC}; c) Energy dissipation in the Rashba source's resistance R_{isoc}; d) Supply resistor losses.

The total energy of MESO is smaller than 10 aJ for scaled device dimensions with scaled material properties. Figure S11 shows the charge dynamics of a scaled MESO with ~35 aC stored charge corresponding to 35 µC.cm^{-2} FE polarization charge density on a 10 nm X 10 nm ME capacitor. The impact of the supply current path can be mitigated via use of high resistive path to limit the current to the required magnitude for switching (Figure S11.B). A supply voltage of 100 mV is applied for 15 ps in Figure S11A, and the resultant voltages at magnetoelectric capacitor (**V(b)**), interconnect (**V(a)**) and the transistor terminal (**V(n)**) are shown. Currents measured through ISOC internal resistance (R_{isoc}), supply resistance (R_s), supply transistor (M) & interconnect resistance (RIC) are shown in Figure S11B. FE polarization charge with retention and charge storage of ~ 35 aC can be observed in Figure S11C. The current in the interconnect follows the voltage difference across the transistor node and the FE node.

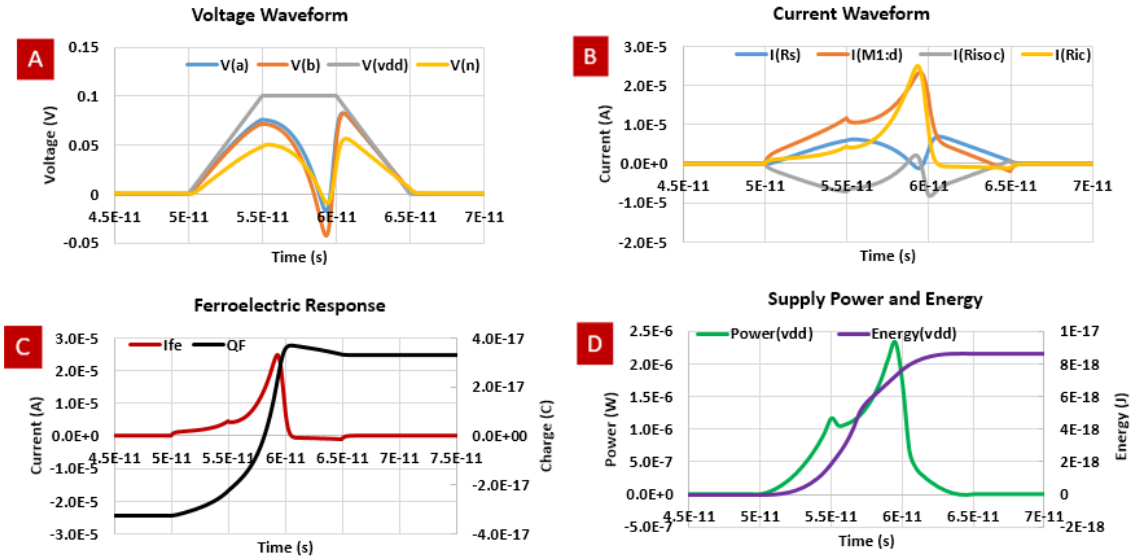


Figure S11. **(Scaled MESO with 35 aC stored charge, sub 10 aJ switching energy)** A)

Voltages applied/measured at supply transistor gate (**V(dd)**), magnetoelectric capacitor (**V(b)**), interconnect (**V(a)**) and the transistor terminal (**V(n)**) B) Currents measured through ISOC internal resistance (R_{isoc}), supply resistance (R_s), supply transistor (M) & interconnect resistance (R_{IC}) C) Ferroelectric node current and stored charge D) Supply power and energy vs time showing the total power delivered by the supply (Pulse width=15 ps, R_{isoc}=4 kΩ, R_s=8 kΩ, R_{ic}=1 kΩ, V_{dd}=100 mV (clk), V_g=0.8 V(dc))

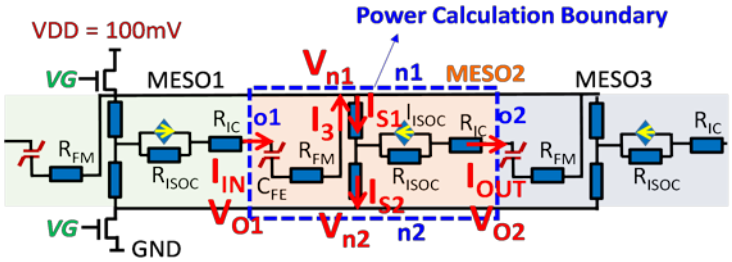
We probe the total power delivered by the supply for the scaled MESO to include the effect of energy loss/storage from all the parts of the device. Figure.S11D shows that the total integrated energy per switching transition is ~ 10 aJ. We note that these devices assumed ~ 35 aC of stored polarization per device which is equivalent to 35 $\mu C.cm^{-2.}$ Further significant scaling in total energy is possible with a reduction of the FE polarization

K. MESO energy and energy scaling measured in circuit simulation

We performed the parameter analysis of C_{FE} in circuit simulation with scaling of the ferroelectric charge from 320aC to 32aC without changing the other MESO circuit parameters. Please note that our calculation only focuses on energy dissipated in MESO device. We first explain how we conduct the energy measurement in circuit simulation and then will show the path to sub-10aJ switching.

Figure S12 shows the measurement method of single MESO device energy in circuit simulation. We illustrate a power calculation boundary for MESO2. The nodes (voltages, currents) connected MESO2 to driver (MESO1), load (MESO3), supply (header transistor) and ground (footer transistor) are o1 (V_{O1}, I_{IN}), o2 (V_{O2}, I_{OUT}), n1(V_{n1}, I_{S1} - I_3), n2 (V_{n2}, I_{S2}). Hence the power measurement of MESO2 ($Power_{MESO2}$) uses the node voltages and currents at the power boundary, as shown in Figure S12. Using this method, the

$Power_{MESO2}$ and $Energy_{MESO2}$ comprehend both the joule heating and ferroelectric switching effects.



$$Power_{MESO2} = V_{n1}*(I_{S1}-I_3) - V_{n2}*I_{S2}+I_{IN}*V_{o1}- I_{OUT}*V_{o2}$$

$$Energy_{MESO2} = \int [V_{n1}*(I_{S1}-I_3) - V_{n2}*I_{S2}+I_{IN}*V_{o1}- I_{OUT}*V_{o2}]\, dt$$

Figure S12. Power and energy measurement method of single MESO device in circuit simulation.

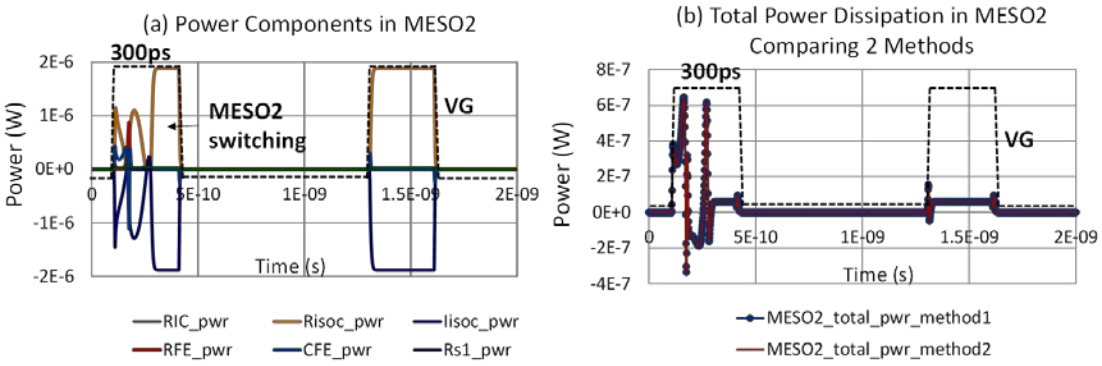


Figure S13. Power components of MESO2 for baseline configuration (QFE=320aC). Method1: power boundary calculation. Method2: adding power dissipation of different components.

The device energy can be calculated using a) Joule heating power of the individual components in MESO b) SPICE (Cadence Spectre) measurements. To show the consistency, we show the power components of each element in MESO2 measured by Cadence Spectre "pwr option" at Q_{FE}=320aC, V_G period of 1.2ns, duration of 300ps, rise/fall time of 10ps. Figure S13 shows 2 periods, where MESO2 only switches in period 1. Method 1 simplifies power calculation in a drawing power boundary regardless of how many circuit components in the boundary and complex circuit behavior.

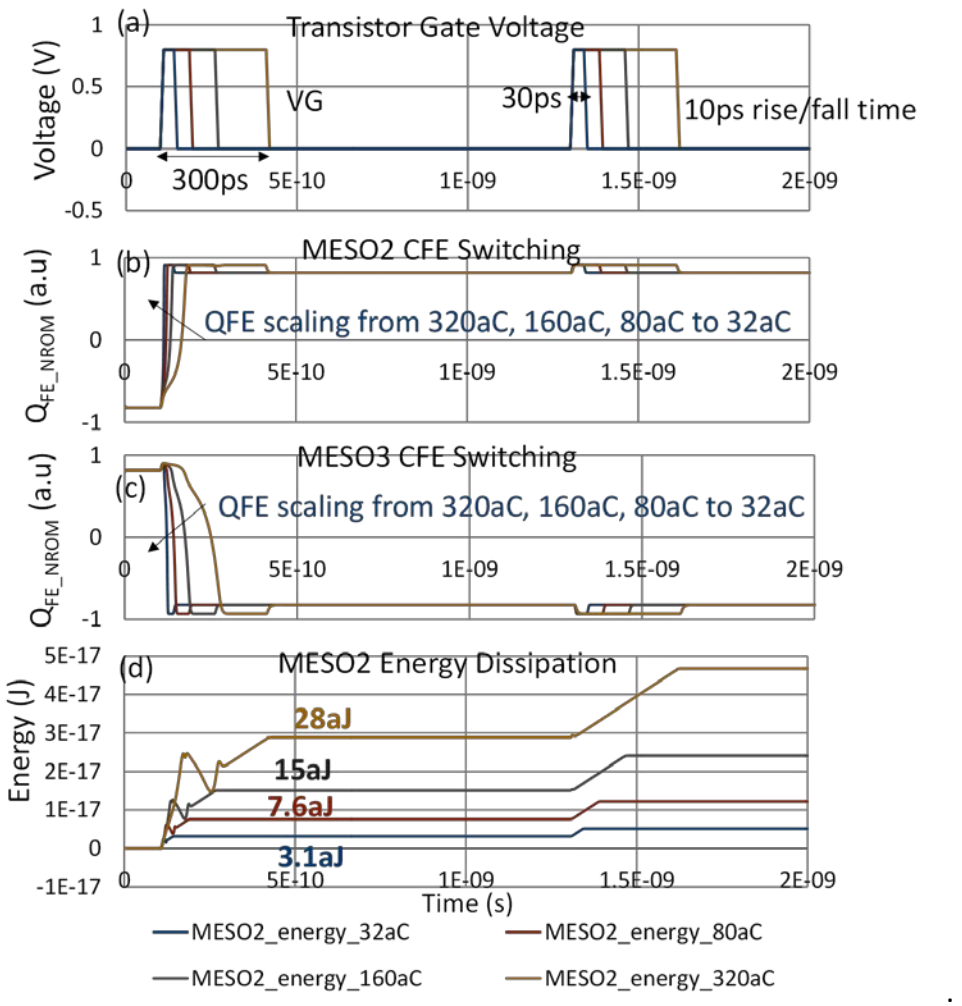


Figure S14. Scaling CFE from 320aC, 160aC, 80aC, 32aC at (a) VG duration of 300ps, 150ps, 75ps, 30ps, respectively. We show 2 periods of VG. At the 1st period when VG is ON, (b) MESO2 switches (driven by MESO1) and then (c) MESO2 also drives MESO3 switching. The energy measured with our described method is shown in (d).

We show the energy calculation and energy scaling to sub-10aJ of MESO2 in Figure S14. We scale Q_{FE} of all MESO devices from 320aC to 32aC and reducing the VG duration from 300ps to 30ps (rise/fall time of 10ps for all cases). Note that the energy calculation of MESO2 includes (1) MESO2 switching time and (2) MESO2 drives MESO3 time duration. Note that for simulated condition of Q_{FE} of 80aC and below, sub 10aJ switching can be achieved.

L. Bidirectional, logic "0" to "1" and "1" to "0" switching in cascaded MESO devices

The circuit simulation of the cascaded MESO devices for combinatorial operation is shown in Figure S15. 2 NMOS transistors are shared by all 6 stages of MESO for power-gating as well as current supply. The shaded background color illustrates the device boundary. We use the following MESO parameters in the circuit simulation: R_{FM}=1k Ohm, R_{S1}=R_{S2}=100 Ohm, R_{ISOC}=5k Ohm, R_{IC}=1k Ohm. Note that the R_{S1} and R_{S2} are smaller than single ended MESO devices due to the insertion of the footer transistor.

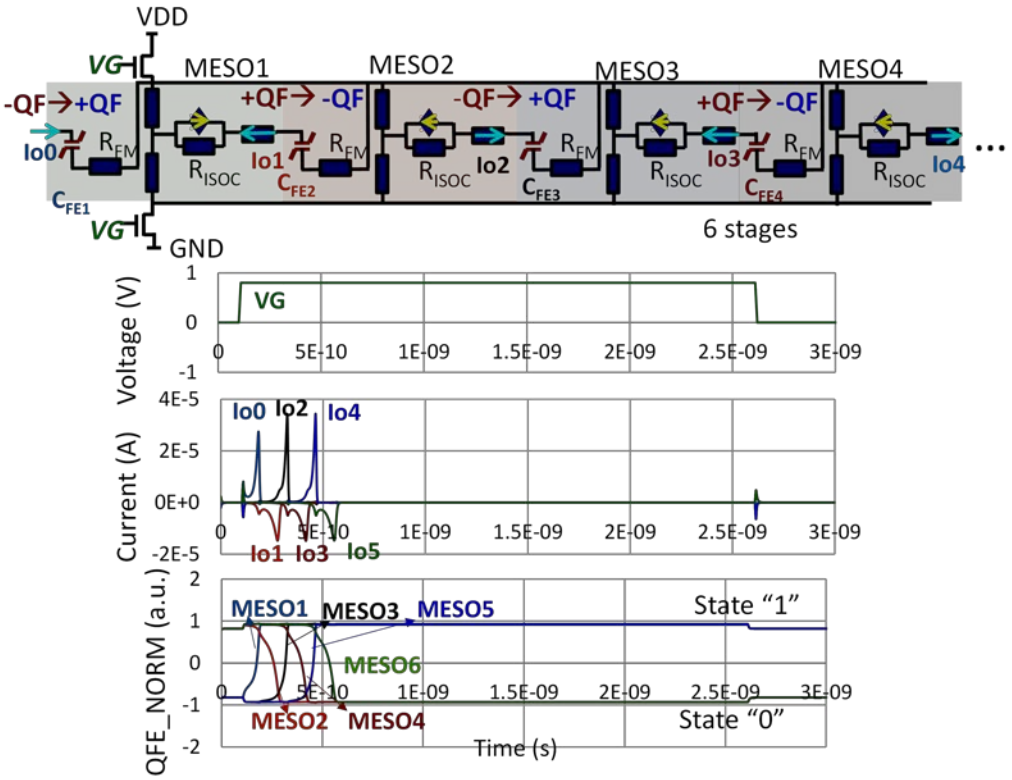


Figure S15. Cascaded 6-stage MESO devices for combinatorial operation (from top to bottom): circuit schematic, power-gating transistor gate voltage waveform, input current I_{O0} and output current of each MESO stage (I_{O1} to I_{O5}) waveform, and MESO "state" (normalized ferroelectric charge on C_{FE}) propagation showing bidirectional switching. V_G=0.8V, V_{DD}=100mV.

The baseline ferroelectric capacitor C_{FE} has coercive voltage V_c of 65mV and ferroelectric charge of 320aC modeled by Verilog-A. The transistor requires V_G=0.8V, V_{DD}=100mV. When Q_{FE}=320aC stored in MESO1's C_{FE1}, Q_{FE_NORM}="+1" and MESO1's is state "1"; when Q_{FE}=-320aC stored in CFE1 of MESO1, Q_{FE_NORM}="-1" and MESO1'state is "0". We will use Q_{FE_NORM} as MESO "state indicator" in the following explanation.

The initial state of the MESO devices are: MESO1, MESO3 and MESO5 are state "0" (negative Q_{FE} stored in the C_{FE}); MESO2, MESO4 and MESO6 are in state "1" (positive Q_{FE} stored in the C_{FE}). I_{O0} is input current to MESO1, I_{O1} is the output current of MESO1 and input current to MESO2, I_{O2} is the output current of MESO2 and input current to MESO3, and so on. When V_G is on and no input current, all MESOs are stable with no switching. (since cascaded MESOs are "0", "1", "0", "1", …). In the combinatorial operation, the cascaded MESO switching is only triggered by the input current I_{O0} from the previous stage.

The waveform of (1) the VG, (2) input currnet I_{O0} and output currents I_{O1} to I_{O5} of MESO1 to MESO5, respectively, and (3) Q_{FE_NORM} of MESO1 to MESO6 showing the MESO state propagation are illustrated in Figure S15. When a positive I_{O0} (from a driver MESO) injects to MESO1's input node at t=100ps, it triggers the switching of the MESO1 from "0" to "1". Once MESO1 switches to "1", it generates I_{O1} that drives and switches MESO2. The switching of the MESO2 cascades to the next MESO to trigger and switch the latter MESO3 (e.g. I_{O2} to I_{O3} and so on). Therefore, the input current I_{O0} triggers the inversion of the MESO1's state such that it can propagate from MESO1 to MESO6. When

V_G is OFF, all MESO states are held due to the non-volatility of the ME material and the ferromagnet (e.g. t > 2.65 ns).

M. Requirements for the resistivity of the spin-orbit coupling materials - Note on internal resistance of ISOC current controlled current source.

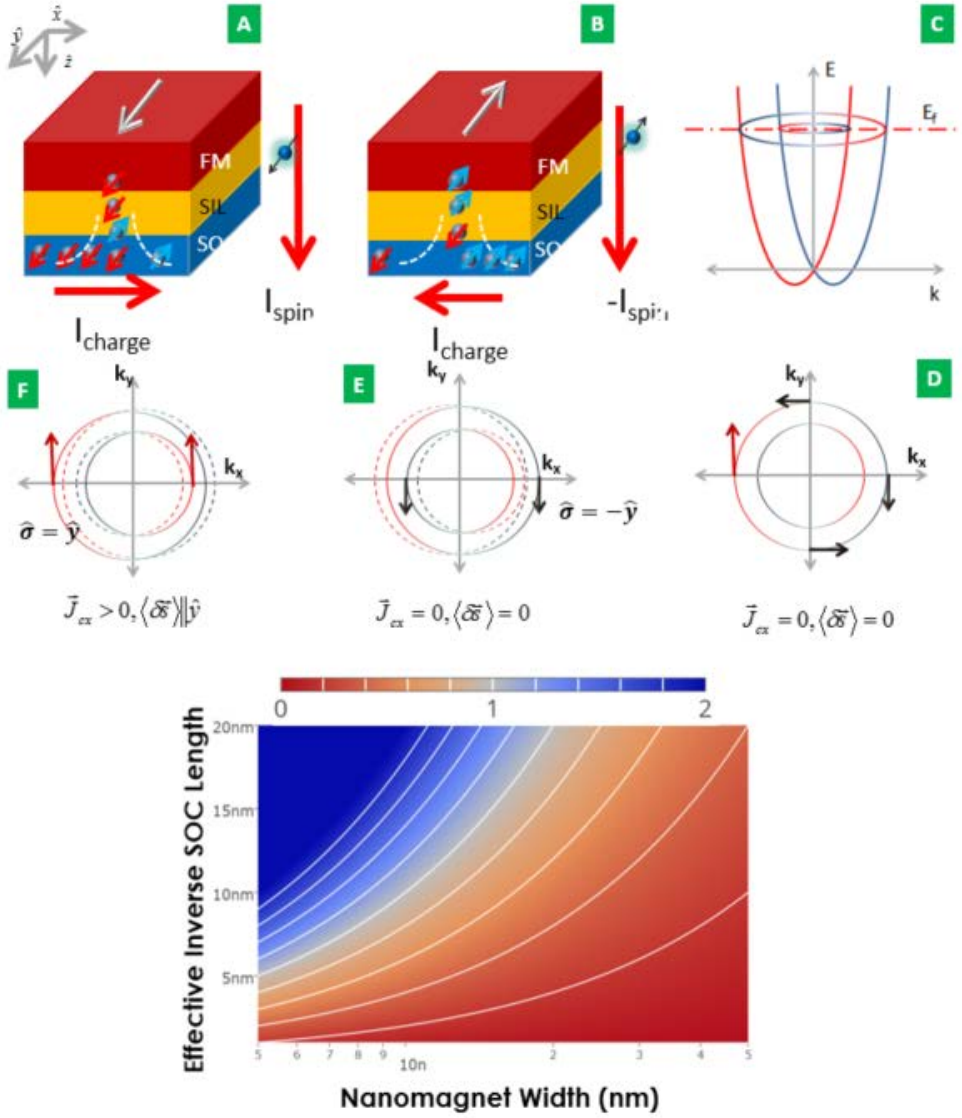


Figure S16. Operating Mechanism for the Spin to charge conversion

The output resistance of ISOC Current Controlled Current Source (CCCS) is obtained by dividing the open circuit voltage of the CCCS divided by the short circuit current [2,

3].The CCCS current source can also be converted to a current controlled voltage source (CCVS) by performing a Norton to Thevenin source conversion.

The ability of a current source to provide a current under resistive loading condition is improved as the internal resistance is increased. Research in spin-orbit coupling materials is opening up the possibility of high spin-orbit coupling materials with high intrinsic resistivity [28, 29], approaching 4-10 mΩ.cm. For example, a resistivity of 10 mΩ.cm [30] will provide an internal resistance of 5 kΩ - 20 kΩ for an ISOC spin to charge conversion layer with dimensions of 20 nm X 10-20 nm X 10-20 nm.

N. Interconnect modeling for MESO

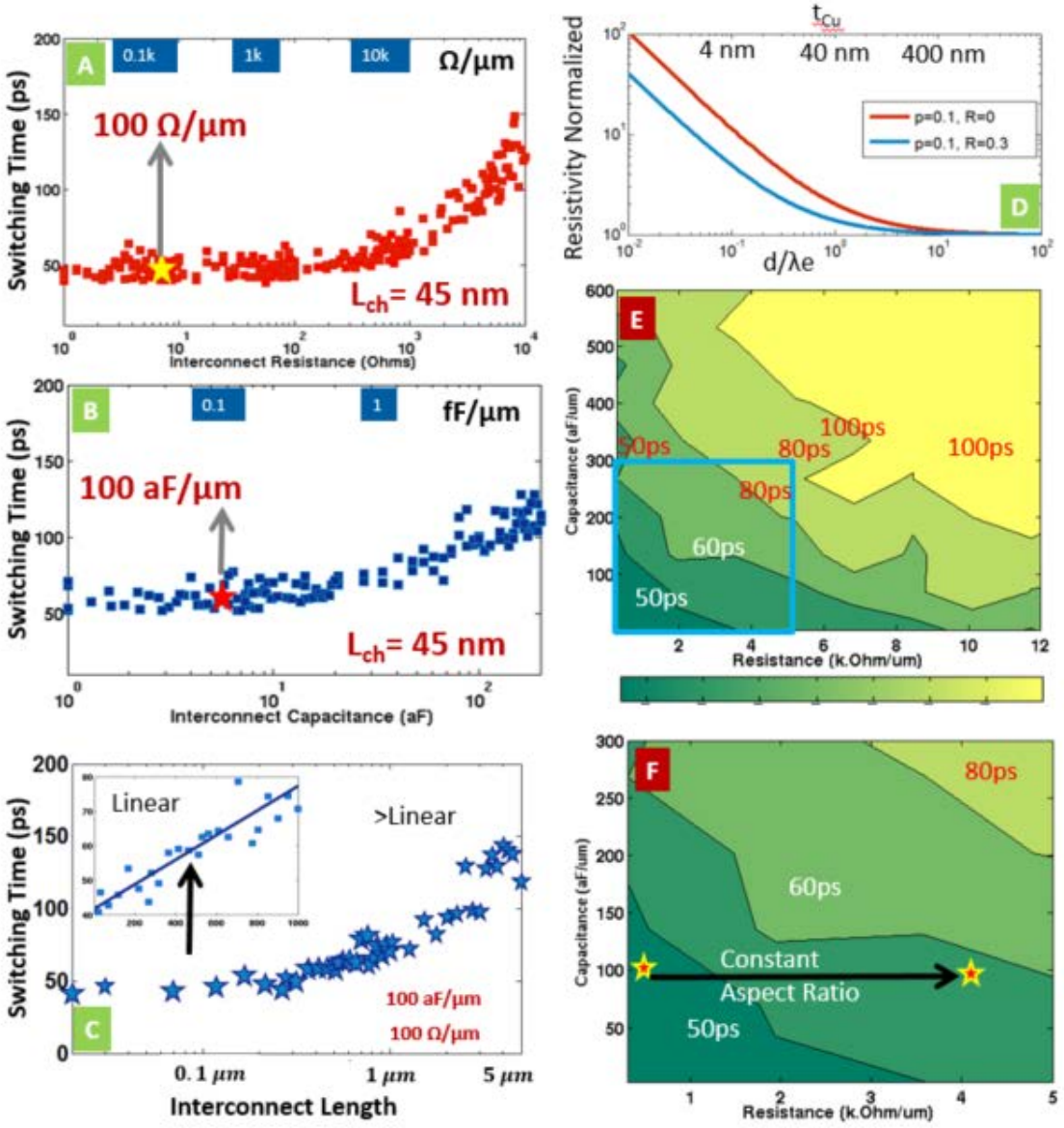


Figure S17. **Interconnect scalability for MESO Logic.** A) Switching delay scaling with interconnect resistance for a 45 nm interconnect (also expressed in resistance per unit length). B) Delay scaling with interconnect capacitance per unit length. C) Switching delay vs interconnect length showing linear delay increase with length. D) Linear delay scaling with length of interconnect (nm). E) Scaling of resistivity of electrical

interconnects showing the impending problem with nanometallic wires scaled to < 10 nm width. F) Combined sensitivity of MESO performance to interconnect capacitance and delay showing minimal performance impact G) Impact on delay with constant aspect ratio scaling from 100 Ω/µm to 4 kΩ/µm interconnects.

MESO uses charge based interconnects which allows us to use the standard technique for IC interconnect models [e.g 31-32]. Here a long RC line is modeled as a Π/T network. The Π/T network is generated for a given length of the interconnect. The key parameters for modeling scaled nanowire interconnects are the resistivity and capacitance on modern nanoscale charge interconnects [33-34].

O. Stochasticity (Dynamic switching error) of magneto-electric switching logic

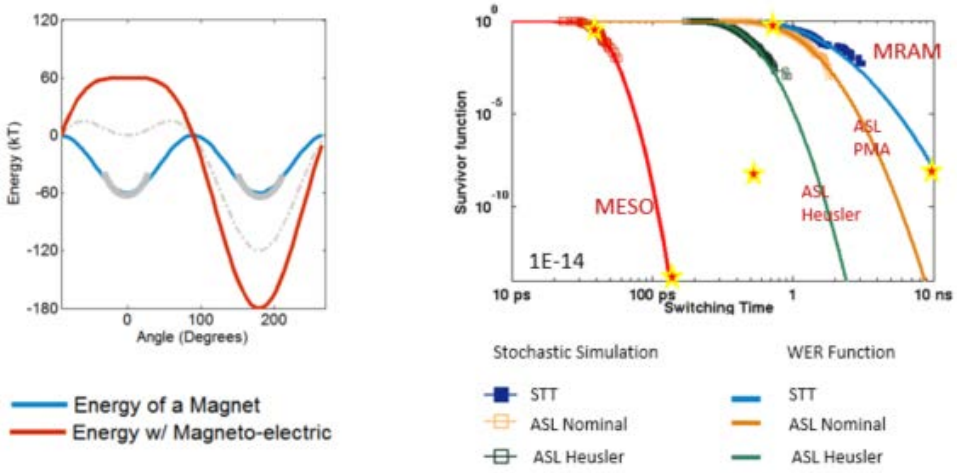


Figure S18. Shaping of the energy barrier in magneto-electric vs spin torque switching. D) Write error rate statistics of MESO logic vs ASL and STT_MRAM.

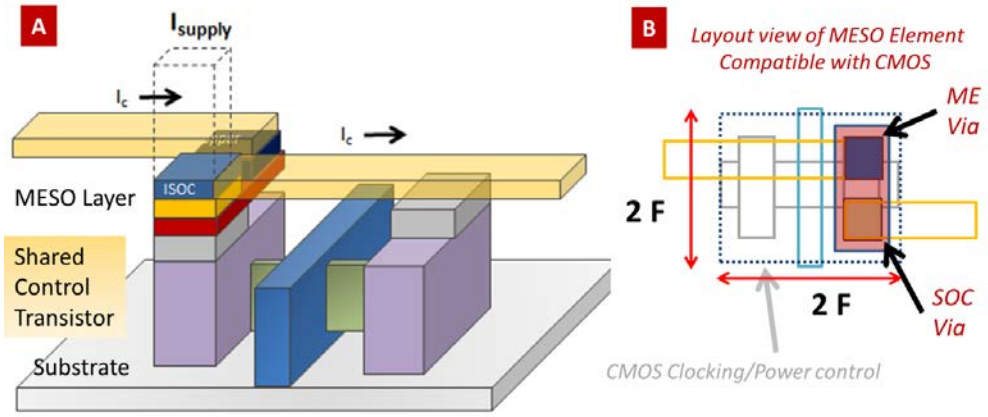


Figure S19 Structural compatibility of the MESO logic with nanoelectronic CMOS. One possible integration scheme of CMOS with MESO logic is shown where scaled 3D FinFETs are monolithically integrated with MESO. MESO materials are formed near the 'Front End' transistors where higher temperature processing is permitted. Each transistor acts as a clock/power source for a number of MESO devices due to the low drive current/voltage needs of MESO. A) CMOS + MESO logic integration with MESO devices integrated into the interconnect layer of scaled CMOS. B) A top view of a compact cell comprising of a control/power transistor and MESO logic. Control transistor is shared among several MESO devices.

P. Spin-orbit transduction devices:

Device shown in Fig 5 is a Pt/$Co_{0.9}Fe_{0.1}$ local spin injection spin-orbit device. Device was fabricated by e-beam lithography, followed by PVD metal deposition method and lift-off process.

We are providing the process flow for reproducibility by other researchers. Detailed process flow is described in Fig. S20. Pt with 15nm thick serving as a spin-orbit material was 1st and bottom layer. Due to poor adhesion of Pt on SiO_2, there is a 3nm Ti adhesion layer between them. Prior to CoFe deposition, Pt surface was cleaned by Ar ion-milling. CoFe with 20nm thick serving as a ferromagnet was 2nd and top layer. There is a Cu capping layer on top of CoFe which prevents CoFe oxidized in air.

Fig. S21 are shown the device structure. By applying charge current (I_C) from Lead 1 to GND, the spin-polarized current generated in CoFe is vertically injected into Pt. Due to the spin orbit coupling effect in Pt, a transverse charge voltage output (V_{SO}) can be measured between Lead 2 and 3. The amplitude of spin-to-charge conversion is $Ri_{SOC}=V_{SO}/I_C$ (see in Fig. 5). Note that this output signal, V_{SO}, is a cascadable voltage source for the next input stage in a closed-loop spintronic logic circuit [35]. Besides, the contribution from the anomalous Hall effect in CoFe is negligible based on calculations [36, 37].

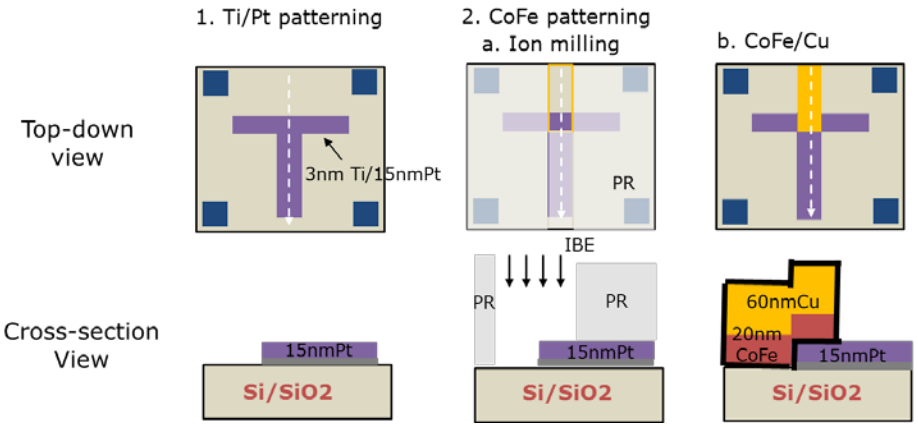


Figure S20. Process flow for local spin injection spin-orbit device

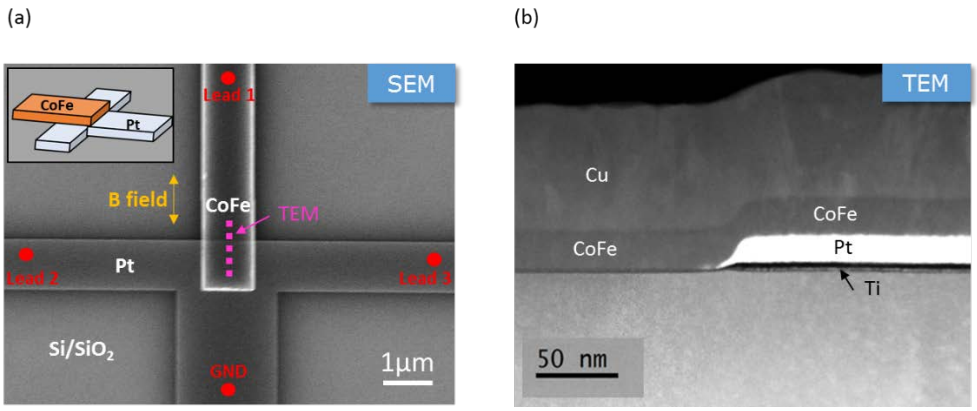


Figure S21. SEM image of Pt/CoFe local spin injection spin-orbit device; (b) Cross-section TEM image in the purple line as shown in (a).

Q. Magnetoelectric coupling devices:

The PLD and sputtering process:

Thin-film heterostructures of $SrRuO_3$ (20 nm)/La-doped $BiFeO_3$ (20 nm)/$SrRuO_3$ (20 nm) were grown by pulsed laser deposition on single crystal $DyScO_3$ $(110)_o$ substrates. The growth of BFO and SRO layer was performed at 700℃ under 100 mTorr oxygen pressure with a laser fluence of ~1 J/cm^2 and repetition rate of 5 Hz. After growth, the films were cooled to room temperature in 500 Torr of oxygen at a rate of 5 ℃/min to optimize the oxidation level. The spin valve heterostructure, Pt (2 nm)/$Co_{0.9}Fe_{0.1}$ (2.5 nm)/Cu (3 nm)/$Co_{0.9}Fe_{0.1}$ (2.5 nm), were sputtered on the top of as-grown $BiFeO_3$/$La_{0.7}Sr_{0.3}MnO_3$ heterostructures at 0.3 mTorr Ar pressure under a 200 Oe growth field.

PFM measurements:

The switching hysteresis loops of $SrRuO_3$ (20 nm)/La-doped $BiFeO_3$ (20 nm)/$SrRuO_3$ (20 nm) were measured by Piezo-force Microscopy (PFM) using a Digital Instruments Nanoscope III in ambient conditions with driving AC frequency 2 kHz and amplitude 30

mV on the conducting cantilever (Micromesh, contact resonance: 150-250 kHz) under a cycling frequency 2×10^{-3} Hz.

MOKE measurements:

The magnetic hysteresis loops of the spin valves were also characterized by longitudinal magneto-optic Kerr effect (MOKE), in which the magnetic field was applied in the easy axis ($[001]_o$). The wavelength of the laser diode for MOKE measurement is 670 nm with the beam diameter ~0.2 mm.

Fabrication and measurements of spin valve devices:

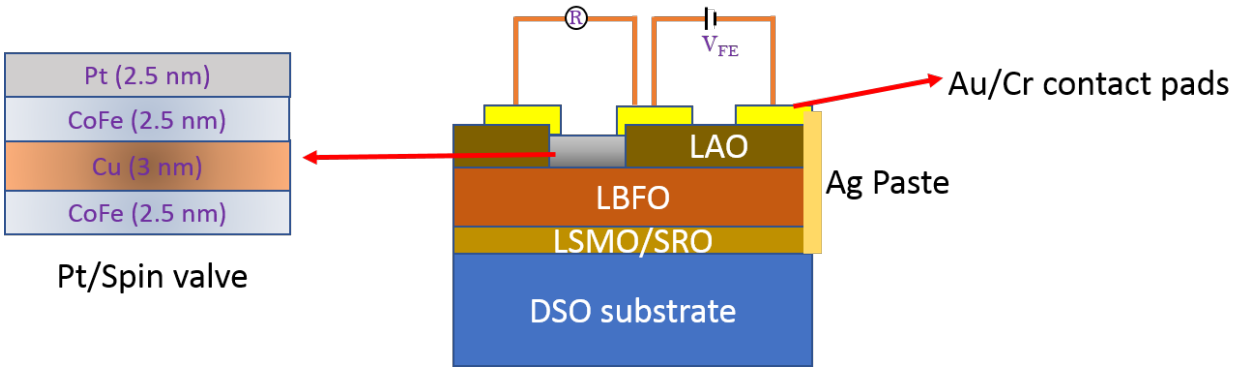


Fig S22: Schematic of the multiferroic (LBFO) - spin valve device. The voltage (VFE) is applied across the LBFO thin film. The resistance of spin valve device is measured in current-in-plane (CIP) configuration.

As shown in the schematics above, after the growth of CoFe/Cu/CoFe/Pt, the spin valves were patterned into 15X5 μm^2 rectangular bars using conventional photolithography and Ar ion milling. In order to isolate the contact lines and pads from LBFO, the milled area was covered by an insulating material, $LaAlO_3$ (LAO). A photolithographic lift-off process was used to create the Cr/Au electric contacts to the spin valves for the current-in-plane configuration measurements. The magnetoresistance of the spin valve devices

was measured in two probe configurations at constant current with varying magnetic field. The two resistance states in spin valves devices was achieved by cycling the applied voltage across the LBFO between -2 to + 1.2 V. The magnetoelectric switching voltages matches well with the ferroelectric switching of LBFO films.

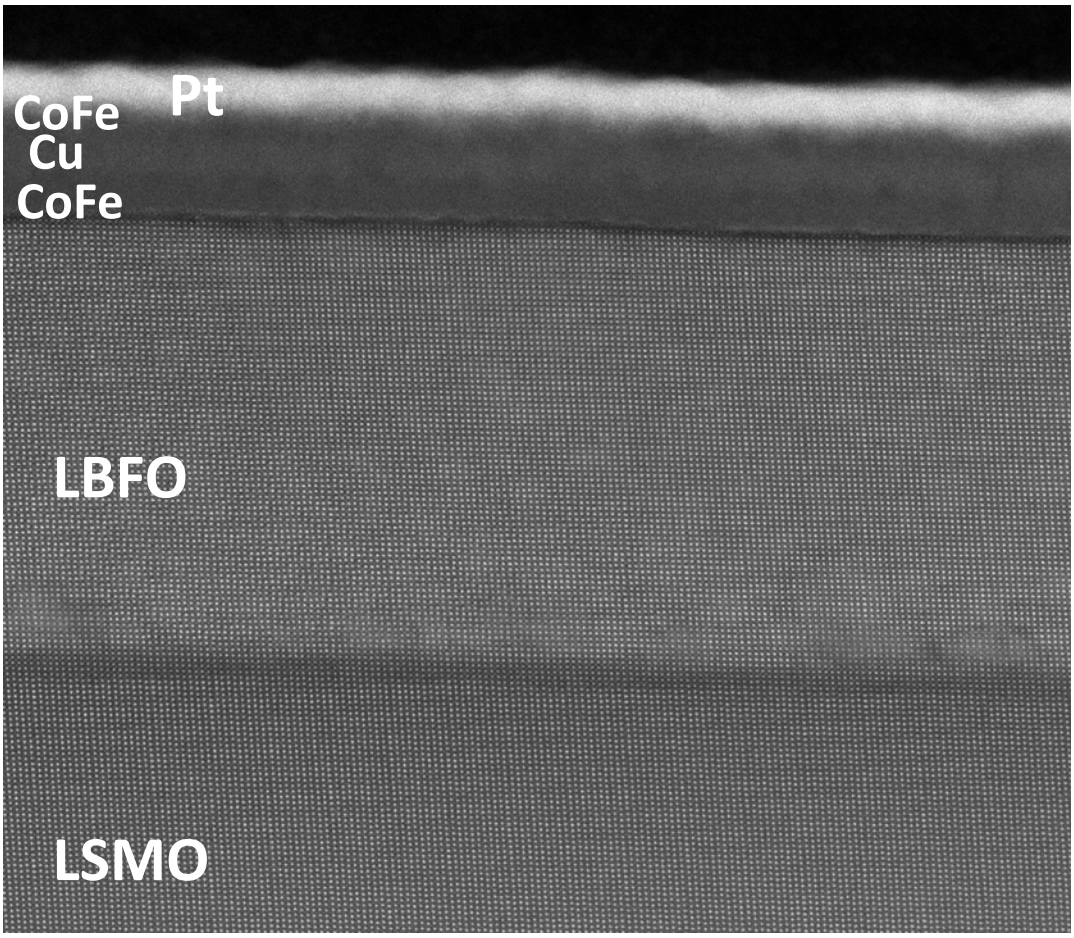


Fig S23: Cross section HRTEM image of LBFO/CoFe/Pt film showing the various interfaces.

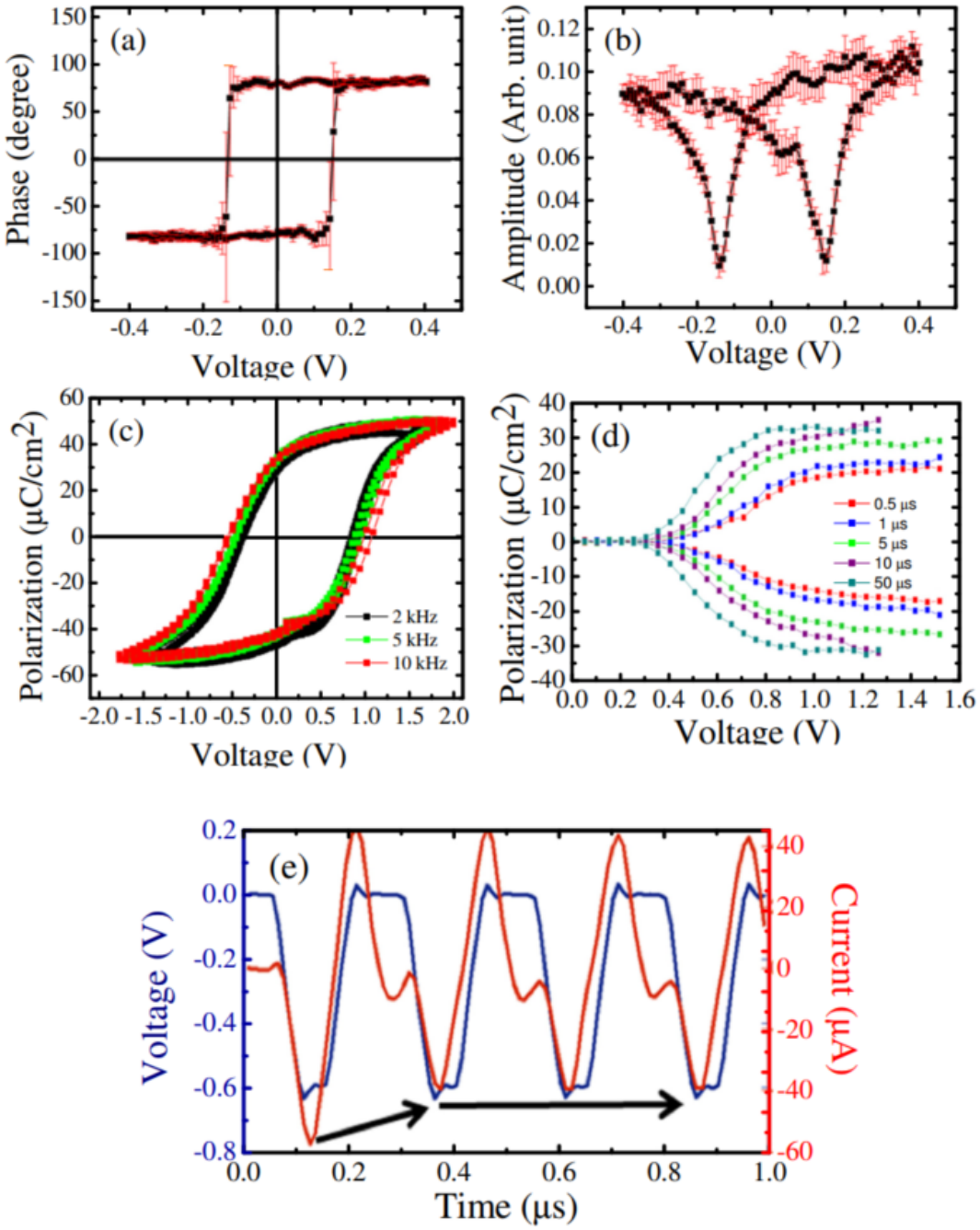


Fig S24: Ferroelectric characterization of SRO/20nmLBFO/SRO heterostructure. a, b, Averaged hysteresis phase and amplitude loops acquired on top of SRO electrode (8 um in diameter) by PFM. c, P-V loops measured by ferroelectric tester (Radiant Precision Premier II) under different frequencies. d, Remnant polarization measurements with different pulse width. e, 50 ns voltage pulse measurement.

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