
Supplementary information

Three-dimensional integration of two-dimensional field-effect transistors

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Three-dimensional integration of two-dimensional field-effect transistors

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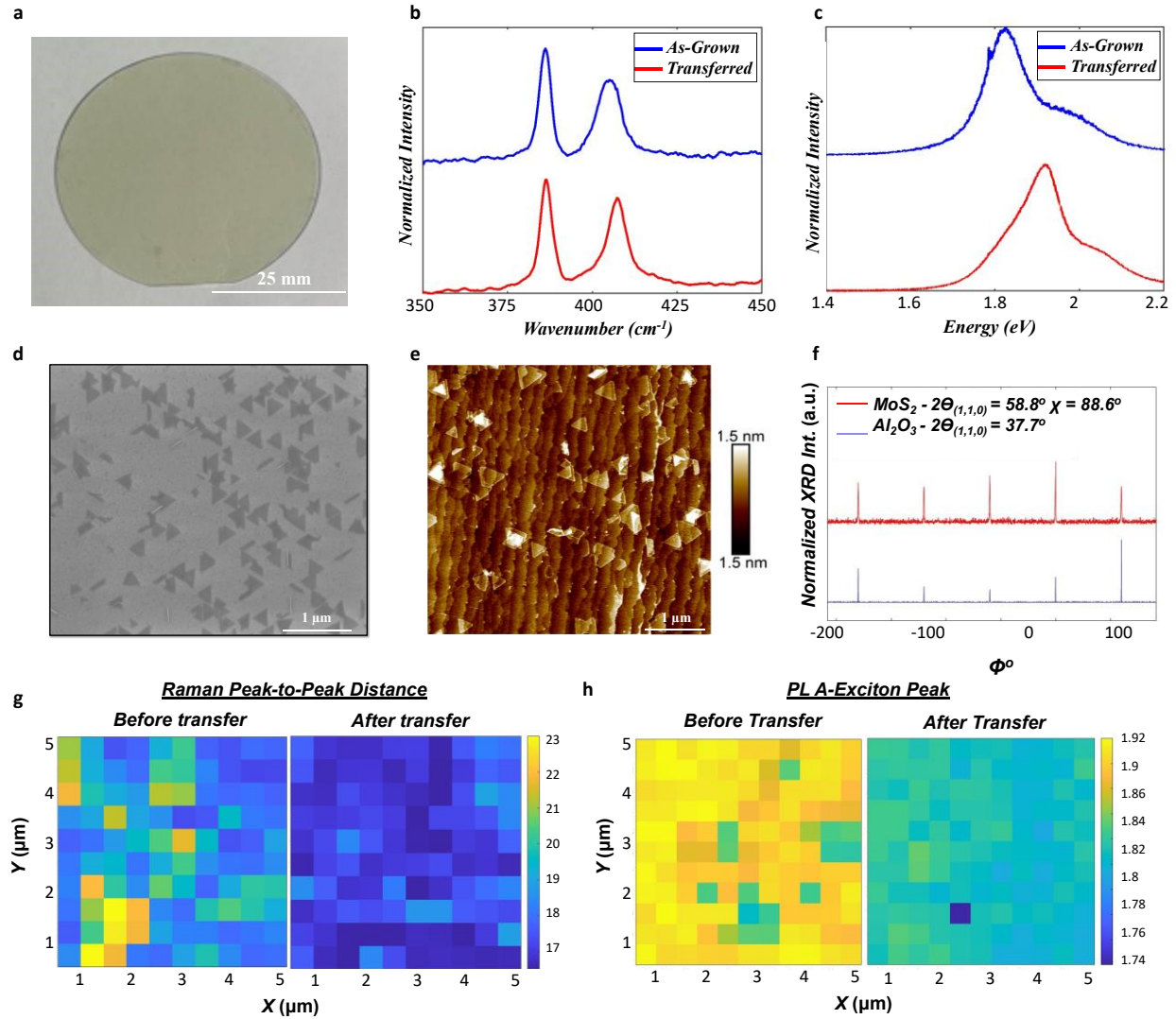
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Supplementary Information 1



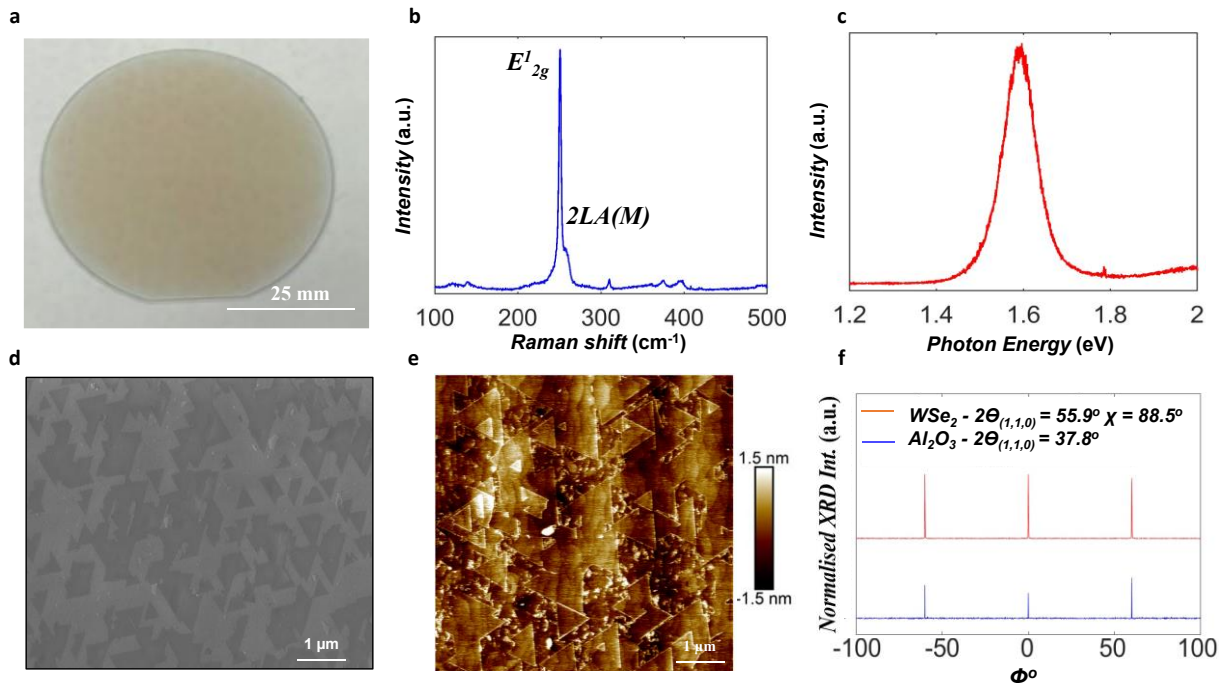
Supplementary Fig. 1. Material characterization for MOCVD grown MoS₂. a) Optical image of the as grown MoS₂ on a 2-inch c-plane sapphire wafer. b) Raman and c) PL spectra for as-grown and post-transfer MoS₂ film. d) SEM image and e) AFM image of the grown MoS₂ film. Formation of multilayer islands on top of a largely monolayer film is observed. f) In-plane XRD Φ -scan of MoS₂ on c-plane sapphire, showing the epitaxial relationship between the MoS₂ monolayer and the sapphire substrate. g) Colormaps of peak-to-peak distance between the Raman modes for as grown and transferred MoS₂ film. h) PL maps of A-exciton peak for as-grown and transferred MoS₂.

Supplementary Fig. 1a shows the optical image of an MoS₂ film grown on 2-inch sapphire substrate. The post-transfer material quality was assessed using Raman and photoluminescence (PL) spectroscopy. While supplementary Fig. 1g shows Raman spectra for as-grown and post-

transfer MoS₂ film and supplementary Fig. 1j shows PL spectra for as-grown and post-transfer MoS₂ film. Supplementary Fig. 1b shows the scanning electron microscope (SEM) image of the MoS₂ film. Formation of bilayer islands on top of a largely monolayer epitaxial film is observed. This is further evidenced by the atomic force microscopy (AFM), given in Supplementary Fig. 1c, in which triangular bilayer islands, on the order of 100-300 nm in size, are observed. Supplementary Fig. 1d shows the in-plane XRD ϕ -scan of MoS₂ on c-plane sapphire, confirming the epitaxial relationship between monolayer MoS₂ and the sapphire substrate.

Colormaps of peak-to-peak distance between the Raman modes for as grown (Supplementary Fig. 1h) and transferred MoS₂ film (Supplementary Fig. 1i) are shown. The separation of the in-plane E_{2g}¹ and out-of-plane A_{1g} Raman modes decreased from 19.1 cm⁻¹ (standard deviation: 1.4 cm⁻¹) in the as-grown film to 17.2 cm⁻¹ (standard deviation: 0.6 cm⁻¹) after transfer. Colormaps of A exciton peak of the as-grown (Supplementary Fig. 1k) and transferred MoS₂ film (Supplementary Fig. 1l) are shown. The A exciton PL peak position redshifted and became more uniform after transfer, going from 1.90 eV (standard deviation = 20 meV) to 1.83 eV (standard deviation = 10 meV), while the peak width decreased from 140 meV (standard deviation = 20 meV) to 90 meV (standard deviation = 10 meV), indicating that the transfer helped alleviate strain in the film.

Supplementary Information 2



Supplementary Fig. 2. Material Characterization for MOCVD grown WSe₂. a) Optical image of the as grown WSe₂ on a 2-inch c-plane sapphire wafer. b) Raman spectra of the WSe₂ film used in this study has been shown. The in-plane E_{2g}^1 and out-of-plane 2LA(M) active modes are labelled. c) PL spectra with an exciton peak ~1.6 eV is shown. d) SEM of as the grown WSe₂ film was done and formation of multilayer islands on top of a largely monolayer film was observed. This is further evidenced by the atomic force microscopy (AFM), given in e). f) In-plane XRD Φ -scan of WSe₂ on c-plane sapphire, showing the epitaxial relationship between WSe₂ and the sapphire substrate.

An optical image of the 2-inch WSe₂ wafer is shown in Supplementary Fig. 2a. Raman and PL spectra of WSe₂ film are shown in Supplementary Fig. 2b-c, respectively. The in-plane E_{2g}^1 (249 cm⁻¹) and out-of-plane 2LA(M) (258 cm⁻¹) Raman active vibrational modes, characteristic to WSe₂, is labeled inside Supplementary Fig. 2b. The PL peak position for WSe₂ is found to be ~1.6 eV. These spectroscopy measurements confirm the monolayer synthesis of WSe₂. Similar to the case of MoS₂, the presence of bilayer islands on monolayer WSe₂ is confirmed with SEM and AFM scans as given in Supplementary Fig. 2d-e, respectively. Finally, the epitaxial relationship between WSe₂ and the sapphire substrate is shown with in-plane XRD ϕ -scan, as given in Supplementary Fig. 2f.

Supplementary Information 3

To the best of our knowledge, the first attempt towards 3D integration with 2D materials involved the fabrication of an inverter by mechanically exfoliating n-type MoS₂ on top of p-type layered transition-metal oxide, Bi₂Sr₂Co₂O₈ [1]. In 2015, Kang et. al. proposed the idea of stacked 2D FETs by utilizing direct growth of 2D materials on SiO₂ [2]. Even though they grew MoS₂ twice to stack FETs, both of them shared the same global back-gate and not much focus was given on 3D integration. The first attempt in utilizing 2D semiconductors as a sensing layer in a 3D-integrated chip was done by Yang *et. al.* in 2016, where they fabricated a 5 × 5 phototransistor array based on CVD grown MoS₂ on top of poly-Si nanowire based FETs [3]. This demonstration clearly shows the benefits associated with sequentially fabricating tiers of devices including flexibility towards choosing different materials/devices/functionalities in each tier, in addition to reducing the active device/circuit area footprint. In the same year, Sachid et. al. demonstrated monolithic 3D complementary-metal-oxide-semiconductor (CMOS) including inverter, NOR, NAND, amplifiers, and mixers using exfoliated MoS₂ and WSe₂ [4]. While exfoliation is generally considered an impractical technique from the perspective of industrializing the technology, the demonstration of low-power circuits with relatively high-performance n-type and ambipolar FETs is certainly impressive. In 2018, Wang et. al., fabricated 3D monolithic stacked 1T1R cells using CVD-grown monolayer MoS₂ and h-BN RRAM [5]. Even though these cells were not stacked right on top of each other due to topography considerations, they successfully demonstrated that their fabrication steps can be repeated to achieve any number of desired levels owing to their low thermal budget < 150 °C. While the above demonstrations showed integration of sensing and logic, 3D CMOS circuits, and integration of logic and memory, 2D materials, in principle, can also be stacked to explore their capability as an alternative nanosheet channel material in currently

explored GAAFET and multi-bridge-channel field-effect transistor (MBCFETs) nano-sheet device structures. This was first explored by R. Zhou and J. Appenzeller where they showed a 2-channel FET based on exfoliated MoS₂ flakes with source-to-drain current, $I_{DS} = 55 \mu\text{A}/\mu\text{m}$ at V_{OV} (over-drive voltage) = V_{DS} (drain-to-source voltage) = 1 V, which was a two-fold increase in comparison to their single channel device [6]. Huang et. al. also fabricated a 2-channel FET with gate-all-around structure using exfoliated MoS₂ and h-BN (gate-oxide) [7]. In another notable achievement, Tang et. al. showed layer-by-layer stacking of 2D materials such as exfoliated graphene and hexagonal boron nitride (h-BN) along with CVD-grown MoS₂. They demonstrated both 3-channel FET for high drive current, as well as the integration of sense-logic-memory across 3-tiers [8]. In 2021, Xiong et. al. fabricated MoS₂-based GAAFETs and complementary FETs based on MoS₂ and WSe₂ [9]. Recently, Xia et. al. demonstrated 2-channel FETs using CVD-grown n-type MoS₂ and stacked complementary FETs using CVD-grown p-type MoTe₂ and n-type MoS₂ [10]. They showed NAND and NOR circuits based on n-type MoS₂ in addition to an inverter based on p-type MoTe₂ and n-type MoS₂. While this demonstration is certainly a step ahead in stacking 2D materials, owing to the use of large area-grown n-type and p-type materials, their device dimensions were relatively large ($L_{CH} > 10 \mu\text{m}$) in all cases. In another demonstration, Liu et. al. fabricated and characterized 22 CVD-grown WSe₂-based p-FETs on top of CVD-grown MoS₂ based n-FETs with 5 μm long channels [11]. Similarly, Jia et. al. fabricated an inverter array using CVD-grown MoS₂ and MoTe₂ [12]. In addition to stacked 2D FETs, there also have been various attempts on integrating 2D materials/devices with silicon logic [13-16].

Supplementary Information 4

We have pursued enhancements and refinements in both synthesis and transfer procedures on a 2-inch wafer scale, leading to a yield of 50-60% on both tiers, which we believe is relatively satisfactory for the 1st generation of 3D ICs. In our observations, the extent of coverage of the as-grown material on the sapphire substrate, along with the influence of the PMMA-assisted wet transfer process, significantly shapes the outcome of device yield. We have noticed that additional factors, such as automated measurements in academic environments, can occasionally hinder yield due to probe misalignment with small contact pads. Thus, the ultimate yield figure might not purely signify material quality, as it becomes intertwined with diverse variables.

Notably, for the three-tier MoS₂ samples, tier 1 exhibited an approximate yield of 90%, tier 2 experienced a yield reduction to around 40% due to incomplete material coverage, and tier 3 achieved a yield of 65%. Similarly, the three-tier WSe₂ sample yields were 67%, 56%, and 45% for tiers 1 to 3 respectively. Even though we were able to demonstrate a large number of devices in multiple tiers, we also acknowledge the fact that device yield must be improved, and further optimizations are required for the same. In terms of the transfer process of 2D materials, there have been several notable demonstrations that happened in the last few years. A discussion on these is provided in Supplementary Information 5.

Supplementary Information 5

The transfer process has undergone significant innovations and indigenous modifications in recent times. Moreover, it has found widespread adoption not only for transferring 2D materials but also for gate dielectric [17], metal contacts [18, 19], and other thin film semiconductors [19]. Even though a more reliable method is indeed desirable and should be actively pursued, it might be premature at the moment to completely discard the transfer approach. In this context, we would like to highlight some of the recent strategies developed by Gurarslan *et al.* [20] and Xu *et al.* [21] based on the hydrophilicity of the sapphire substrate, utilizing capillary forces to facilitate clean transfer of 2D TMDs using PMMA. In fact, using similar approaches, Seol *et al.* [22] and Yang *et al.* [23] have demonstrated high-throughput transfer of 6-inch wafer-scale films of monolayer MoS₂ and WS₂ utilizing PMMA. In addition, minimizing human intervention in the transfer process has the potential to significantly enhance its reliability. An impressive advancement in this realm is showcased by Mannix *et al.*, who introduced a robotic four-dimensional pixel assembly method to achieve reproducible and ultra-clean transfer of van der Waals 2D materials [24]. Finally, complete elimination of the transfer process would require the direct growth of high-quality 2D materials onto preferred gate stacks at low temperatures. Along these directions, synthesis of 2D materials on arbitrary substrates as described in [25] and [26] at temperatures compatible with back-end-of-line CMOS process flow are noteworthy and can be adopted for the 3D integration with limited modification of the process flow described in our manuscript.

Supplementary Information 6

Some of the challenges that must be addressed before pursuing very-large-scale-integration (VLSI) of 2D FETs in a 3D CMOS architecture, are given below.

1) Controllable and reliable approaches to threshold voltage engineering:

Threshold voltage (V_{TH}) engineering is of paramount importance for both n-type and p-type FETs in the context of CMOS circuit design. CMOS circuits rely on the synergistic operation of both n-type and p-type FETs to achieve efficient logic operations, low power consumption, and optimal performance. For example, lowering the V_{TH} of n-type FETs allows them to switch on at lower supply voltages, enabling faster operation and reducing power consumption. Similarly, for p-type FETs, the V_{TH} needs to be raised to ensure proper complementary behavior with n-type counterparts. This helps in preventing unintended device conduction in the off state. In other words, V_{TH} engineering enables accurate voltage level shifting, essential for signal propagation in CMOS circuits. In Si-based CMOS technology, precise control of V_{TH} for both n-type and p-type FETs is achieved through various techniques: a) by tailoring the doping concentration in the semiconductor material, b) by adjusting the material composition or dimensions of the channel region, and c) by modifying the work function of the gate electrode material. Collectively, effective V_{TH} engineering in n- and p-type FETs is pivotal for achieving balanced and optimized CMOS circuit performance ensuring low power consumption and high speed. In the above context, while notable progress has been made in achieving high-quality synthesis of both n- and p-type 2D TMDs at wafer scale, as exemplified in the manuscript, comparable advancements in the realm of V_{TH} engineering remain scarce. Various avenues can be explored to accomplish this objective, as given below.

a) Substitutional doping: Within TMDs, a feasible avenue involves the substitutional replacement of both cationic and anionic elements with foreign atoms possessing similar radii [27]. Cationic elements can be replaced by elements such as Nb, Ta, and V to achieve *p*-type doping and Re, Hf, and Zr for *n*-type doping, respectively [28-32]. For example, Kozhakmetov *et. al.* showcased the modulation of V_{TH} in *p*-type WSe₂ FETs by varying the doping percentages of vanadium atoms, which were introduced during the synthesis process using the metal organic chemical vapor deposition (MOCVD) technique [30]. Similar results were obtained for *n*-type FETs using substitutional Re doping of MoS₂ monolayers with controllable concentrations down to 500 ppm using MOCVD [32]. This substitutional approach extends to anionic replacement as well, achievable through plasma exposure to elements like carbon [33], nitrogen [34], helium [35], and others.

b) Surface charge transfer doping (SCTD): A different approach to doping involves SCTD, in which the nature and degree of doping in the underlying 2D channel are influenced by factors such as the work function, electron affinity, and concentration of the adsorbed or deposited interfacial species. SCTD has been exhibited in numerous TMD materials, allowing for the achievement of both *n*- and *p*-type doping with differing degrees of efficacy [36]. Doping can also be induced by depositing a sub-stoichiometric insulator such as aluminum oxide [37], amorphous titanium suboxide [38], molybdenum trioxide [39-41], and silicon nitride [42]. An additional method involves subjecting TMDs to ozone or oxygen plasma treatment, which transforms the outermost layer of TMDs into their corresponding sub-stoichiometric oxides. This process leads to significant *p*-type doping effects in the underlying layers [39, 40]. In FETs that rely on multilayer 2D materials, the space between layers has been utilized for doping purposes through the introduction

of external ions, atoms, and even diminutive molecules. However, ensuring stability, compatibility with fabrication processes, and the ability to create patterns present significant challenges associated with this technique.

2) Improving yield and reducing variability of 2D FETs:

In addition to V_{TH} engineering, high device yield and low device-to-device variability are some of the other key requirements for the design and demonstration of large scale CMOS circuits. Whereas yield impacts efficient design of the integrated circuits (such as the footprint), uniformity in device performance is the key for proper functioning of the CMOS circuits (achieving correct voltage levels). Despite notable advancements, further endeavors are required to enhance both yield and uniformity in 2D FETs, particularly on a wafer scale [43]. In addition to fine-tuning or eliminating the transfer process (discussed in Supplementary Information 5), enhancing yield, and reducing variability in 2D FETs mandates comprehensive optimizations in both 2D material synthesis and process integration. This involves addressing issues such as vacancy reduction, impurity mitigation, crack and wrinkle prevention, and strain uniformity while upholding crystallinity. Moreover, process integration necessitates optimizing gate-dielectric integration, refining contact formation, and incorporating effective post-fabrication device treatments or annealing steps. Along these lines, Walzl *et. al.* [44] have performed a thorough evaluation of the influence of non-idealities in individual FETs on the 2D-based electronic circuits. They point out how electrically active traps formed due to defects at the channel, dielectric and/or channel-dielectric interface can lead to variability in the threshold voltage of individual devices. Consequently, prior to showcasing high-density 3D CMOS circuits built upon 2D FETs, it is imperative to enhance yield via optimization of synthesis, transfer, and fabrication processes.

Equally crucial is the identification of a 2D material-dielectric combination that offers acceptable device-to-device variability.

Supplementary Information 7

It is important to investigate and optimize the dielectric/2D semiconductor/ILD interface quality [44] for achieving 3D CMOS with 2D FETs. This research area, when complemented with defect-free material synthesis and ultra-clean automated transfer techniques, can lead to a considerable reduction in device-to-device as well as tier-to-tier variations. It was observed that the use of Al_2O_3 as the ILD causes the introduction of interface traps leading to a shift in V_{TH} , requiring further exploration into other material choices for ILD. Also, Al_2O_3 has a high dielectric constant. A key requirement for ILD is ultra-low dielectric constant with adequate thermal and mechanical stability [45]. The semiconductor industry has seen the evolution from silicon dioxide, silsesquioxane-based materials, to silica-based and porous silica materials to reduce the dielectric constant of ILD from 4.5 to as low as 1.5 [46]. However, porous ILDs are thermally unstable, mechanically weak, and often incompatible with other materials and processes necessitating innovation in ILDs [47].

Supplementary Information 8

Planarization is an inevitable fabrication step in the semiconductor industry [48]. Among several strategies, chemical mechanical planarization (CMP) is the most commonly adopted one that involves simultaneously applying a chemical slurry along with mechanical abrasion to remove material from the surface of a wafer. From the perspective of the 3D stack mentioned in this work, the CMP process can be implemented on insulating layers, specifically the inter-tier dielectric, which function to separate distinct tiers of 2D FETs. This arrangement can safeguard the 2D film from any potential adverse effects induced by the CMP process. Nonetheless, CMP must be optimized to encompass the inter-tier dielectric material selection, the chemicals employed, and the precise calibration of the temperature changes and mechanical forces associated with the process [49]. These considerations are pivotal to ensure that the CMP process effectively planarizes the inter-tier dielectric while maintaining the integrity of the 2D film and overall semiconductor structure.

Supplementary Information 9

The starting step to design a 3D chip is to understand the final application. While increasing the device integration density and scaling is certainly the major goal of 2D-based 3D integration, it also offers the capability to incorporate various functionalities across different tiers. Thus it is important to analyze the compatibility and integration strategies of various materials and devices that are required to achieve the final goal. Detailed modeling can also help analyze the potential parasitic capacitance and electrostatic coupling in a 3D chip in addition to possible strategies to perform efficient thermal management. For example, Jiang *et. al.* have previously evaluated the benefits associated with 3D integration of 2D materials along with analysis of electrical performance, thermal issues, and electromagnetic interference [50]. Moreover, VLSI demonstration of 3D CMOS will also require a thorough understanding and analysis of current 3D integration steps such as tier partitioning [51], placement [52] and clock-delivery networks [53] as well as tuning them appropriately for accommodating 2D FETs. Finally, the impact of various defects on 3D circuits can only be studied with appropriate test structures. Thus, 3D test structures must also be considered during the design of a 3D chip [54].

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