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Supplementary information

Monolithic three-dimensional integration of silicon transistors

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Monolithic three-dimensional integration of silicon transistors (Online Supplementary Information)

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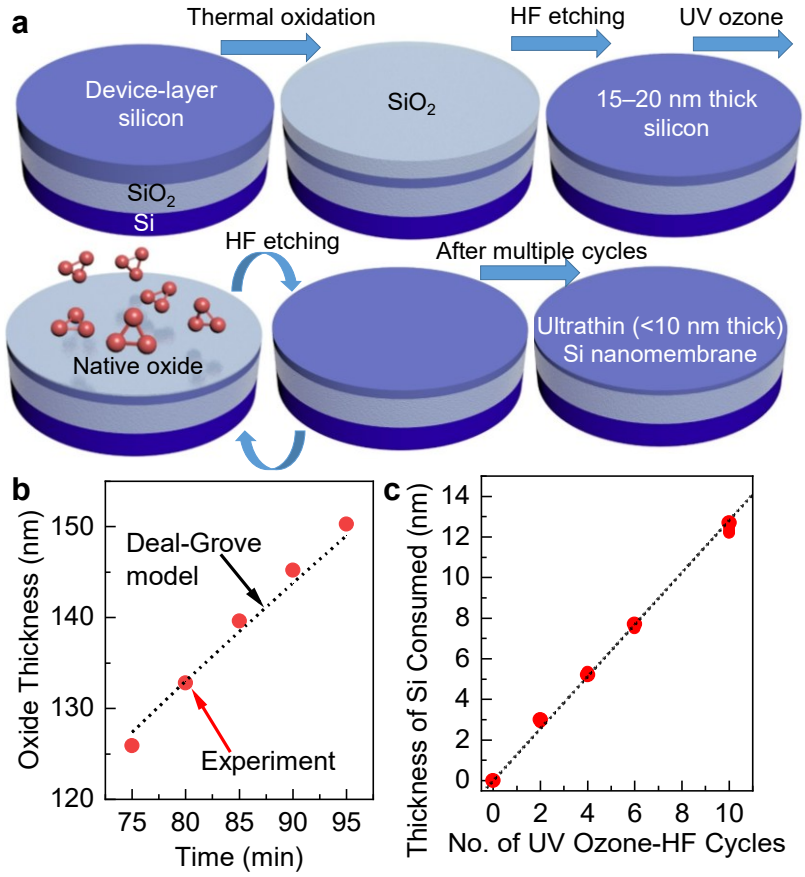
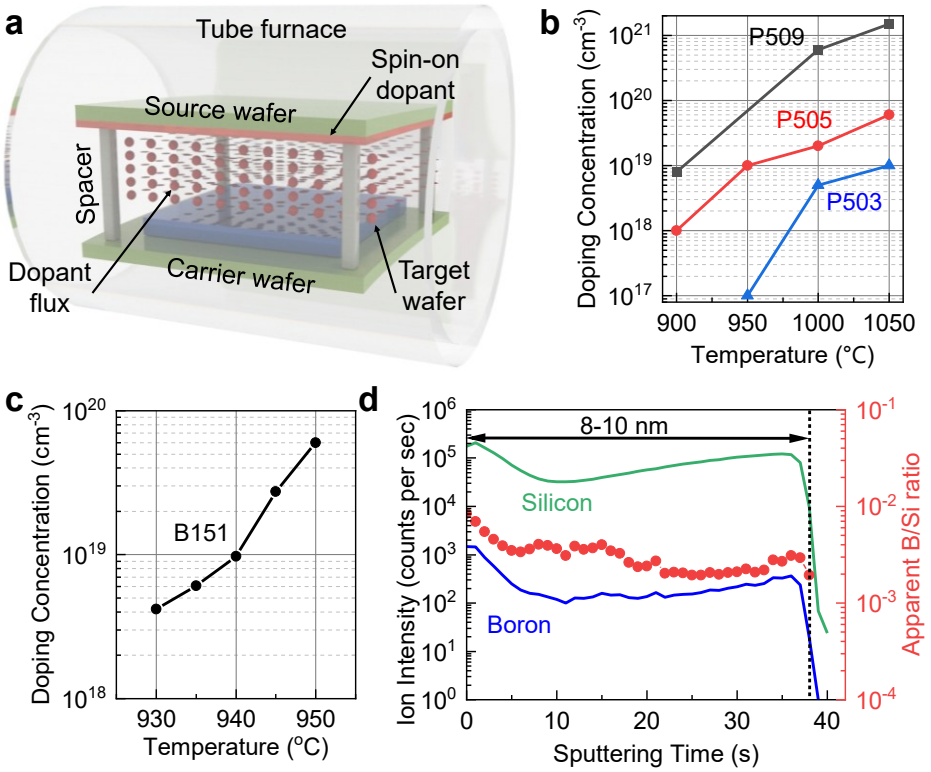
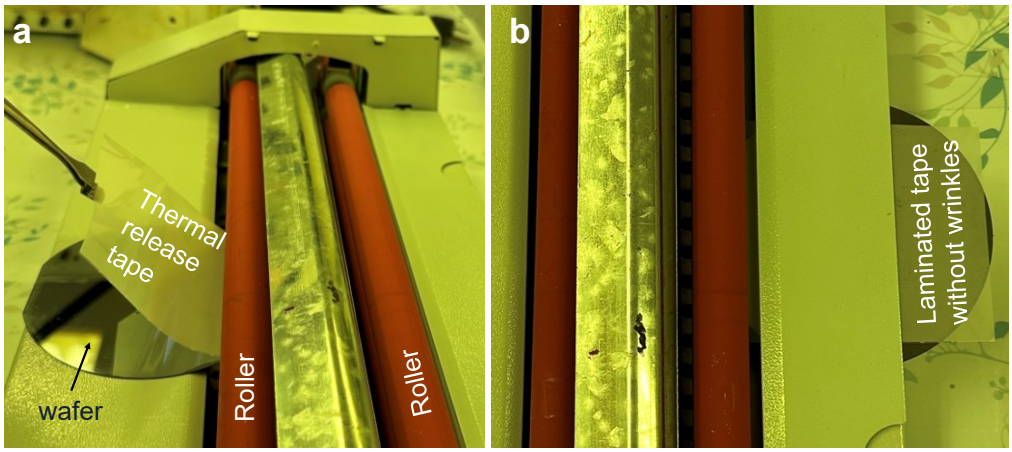


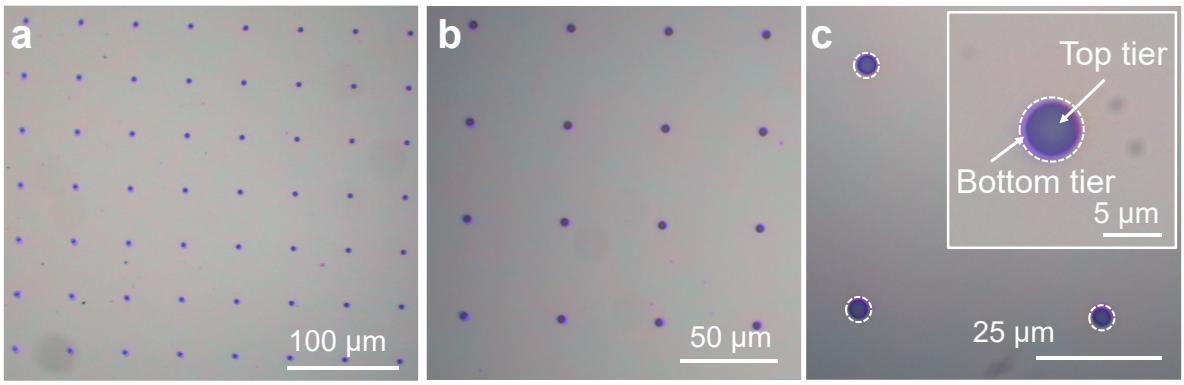
Supplementary Figure 1| Oxidation to form single-crystalline silicon nanomembranes with precisely controlled sub-10 nm thickness. **a,** Schematic showing our process involving thermal oxidation and repeated surface-oxidation and oxide-etching cycles. **b**, Growth of silicon dioxide from the device-layer silicon of SOI wafers by dry oxidation at a processing temperature of 1100 °C. Black dashed line represents the growth kinetics predicted by the Deal-Grove model. **c**, Thickness of silicon consumed as a function of the number of UV-ozone surface-oxidation and HF-etching cycles performed to precisely control the silicon film thickness with nanometre resolution. Black dashed line represents linear fitting to the data.



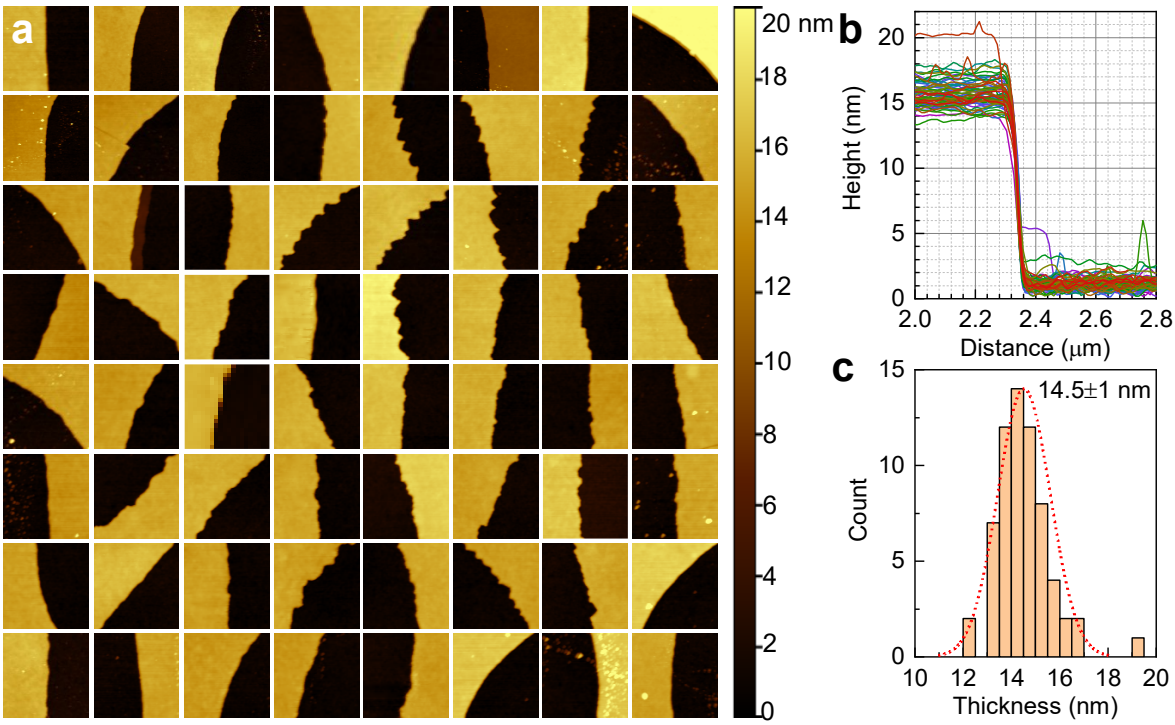
Supplementary Figure 2| Silicon doping from spin-on dopant sources in proximity rapid thermal diffusion. a, Schematic showing the source and target wafers are stacked in proximity during thermal annealing. **b-c**, Dependence of phosphorous (part **b**) and boron (part **c**) concentrations in the target wafer after doping, as determined from silicon resistivity on diffusion temperature, using different types of spin-on dopants. **d**, The ion intensities of silicon (green, left axis) and boron (blue, left axis) as determined by secondary ion mass spectroscopy (SIMS), as well as their relative ratio (red dots, right axis), are plotted as a function of the sputtering time to show the doping profile across the 8–10 nm thick silicon nanomembrane with a decreasing gradient from its top surface.



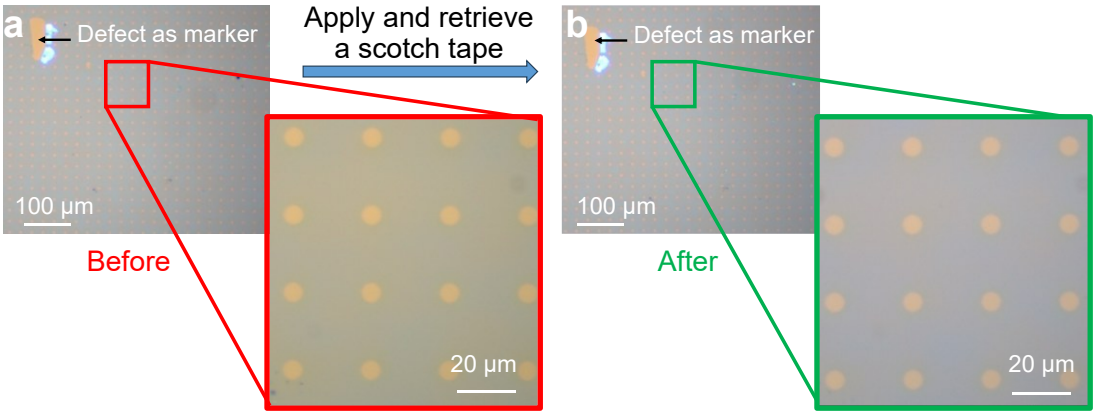
Supplementary Figure 3| Roll transfer of ultrathin silicon nanomembranes using a laminator. **a,** Optical picture showing feeding the wafer and the thermal release tape into a desk-top hot-roll laminator. **b**, The wafer exiting from the laminator with the tape applied without wrinkles or bubbles.



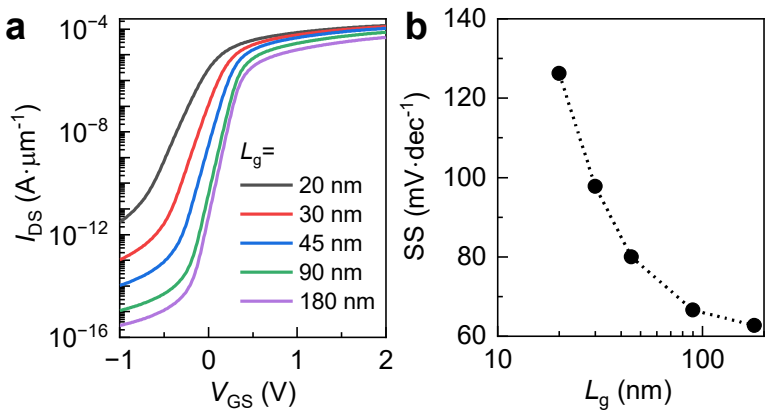
Supplementary Figure 4| Alignment of sacrificial access patterns between different tiers of transferred single-crystalline silicon nanomembranes. Optical images showing the misalignment less than 1 μm under low (part **a**, scale bar: 100 μm), medium (part **b**, scale bar: 50 μm), and high (part **c**, scale bar: 25 μm) magnifications. Inset: zoom-in view of the access patterns, scale bar: 5 μm. The white dashed circles as visual guide highlight the boundary of keep-out regions as part of the design rule in the PDK to avoid these holes.



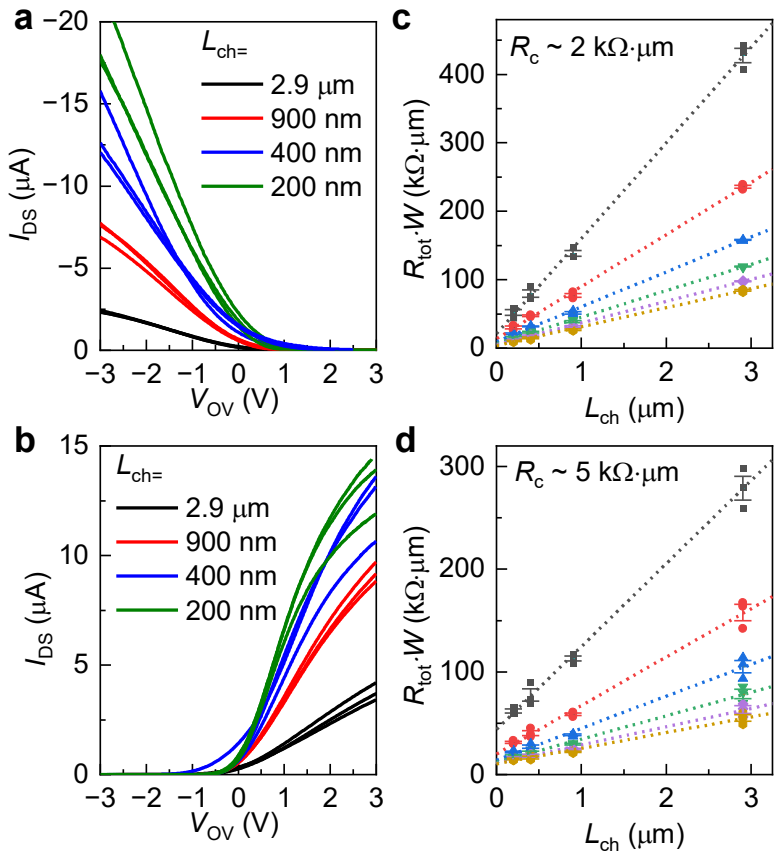
Supplementary Figure 5| AFM mapping of the thickness of a transferred single-crystalline silicon nanomembrane over a 70 × 70 mm^2 area on a four-inch wafer. a, Collection of 8×8 AFM micrographs (500 nm by 500 nm), each taken from an 8×8 mm^2 area cut from the transferred silicon nanomembrane with a dicing saw (Advanced Dicing Technologies Ltd.). **b**, Collection of all 64 line-cut profiles to extract the film thickness. **c**, Histogram showing the thickness distribution with a standard deviation of ± 1 nm. The film thickness includes ~ 2 nm native oxides on both top and bottom surfaces of the silicon nanomembrane as shown in Fig. 1f, giving the silicon-layer thickness ~ 10 nm. Red dashed line represents a Gaussian fitting to the data.



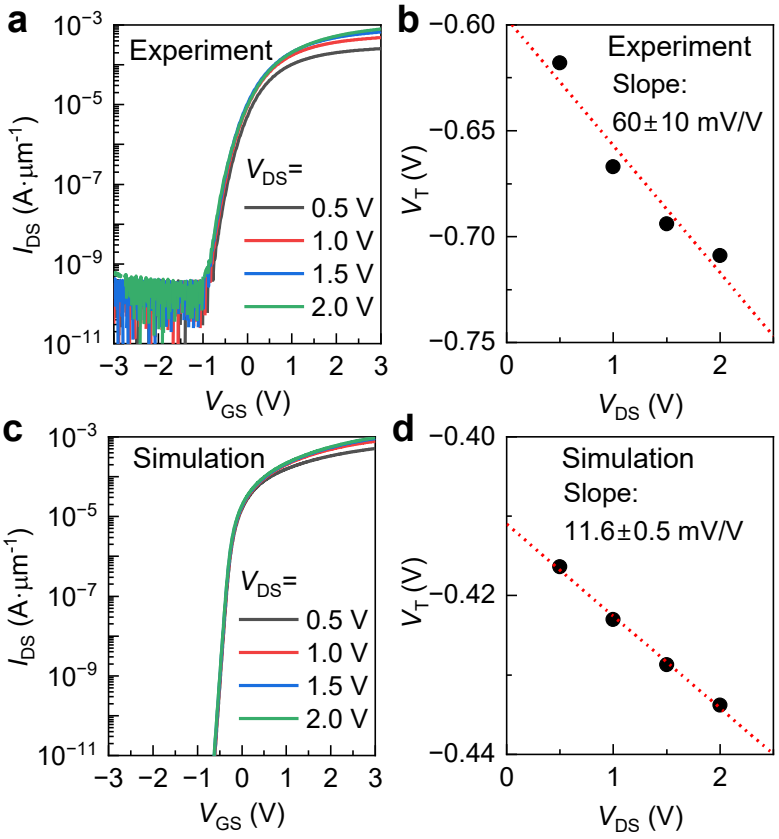
Supplementary Figure 6| Strong adhesion between the transferred silicon nanomembrane and the receiving substrate as verified with scotch-tape test. a-b, Optical micrographs (scale bars: 100 μm) showing the ultrathin, single-crystalline silicon nanomembrane transferred onto a SiO_2/Si substrate before (part **a**) and after (part **b**) being subjected to a scotch-tape test, with zoom-in views (scale bars: 20 μm). The structural defect was intentionally created and utilized as a marker for us to locate the exact same region for comparison.



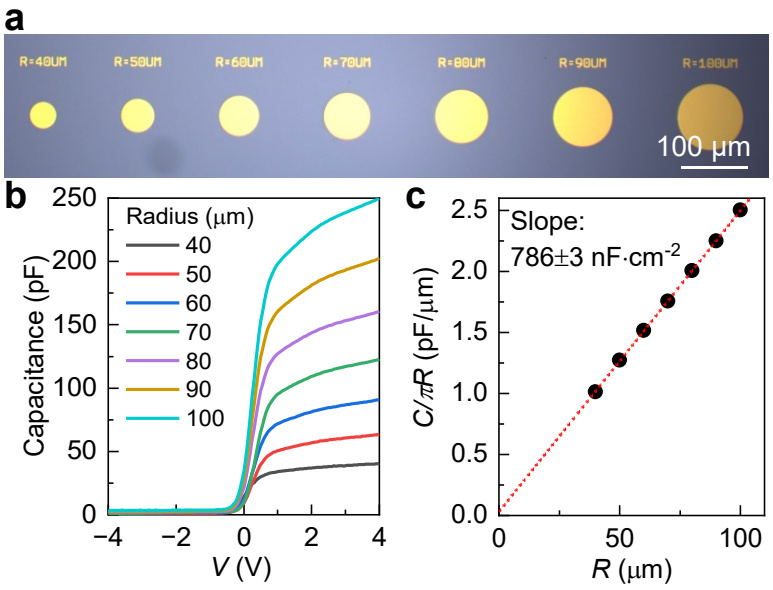
Supplementary Figure 7| TCAD simulation of BEOL-compatible junctionless transistors. a, Simulated transfer curves of planar junctionless transistors with a uniform channel phosphorus doping concentration of 10^{19} cm^{-3}, for gate length L_g scaled from 180 nm to 20 nm. The silicon channel thickness is 8 nm, and the gate oxide is 10 nm HfO_2. Applied V_{DS} is 50 mV. **b**, SS as a function of L_g.



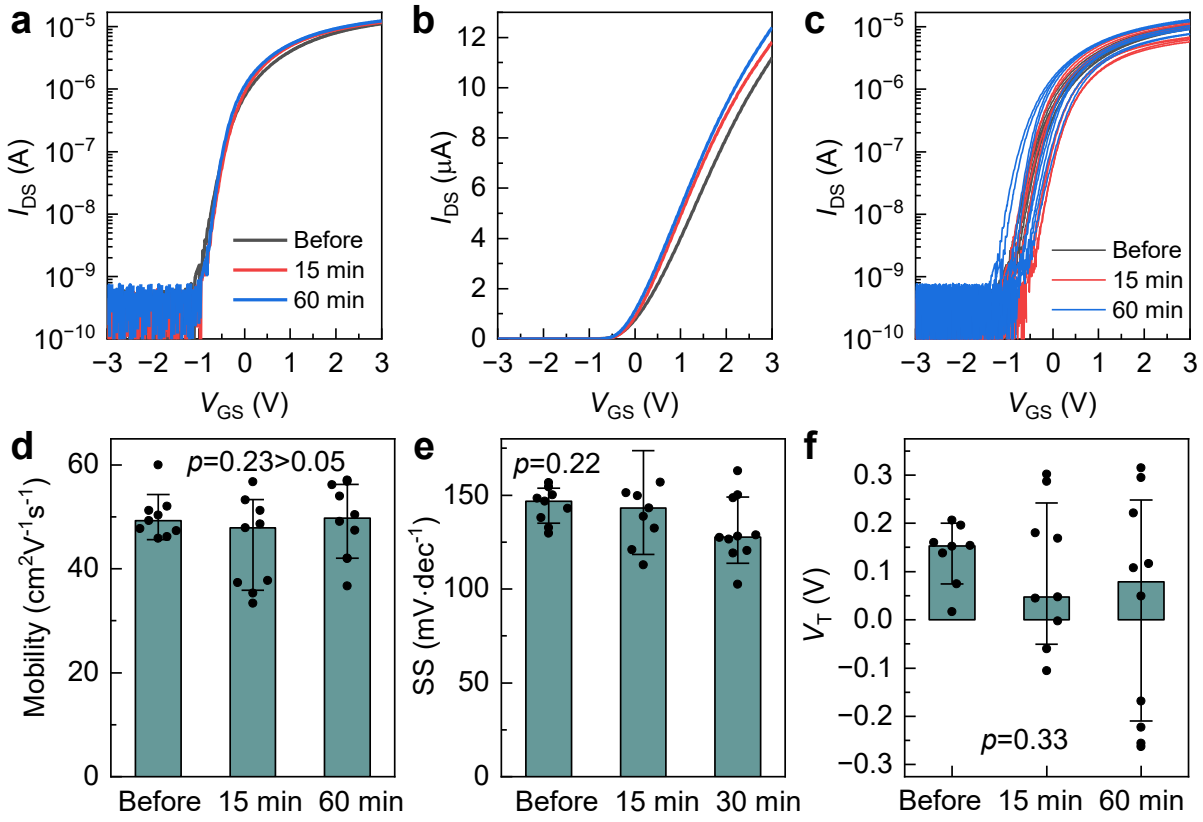
Supplementary Figure 8| Contact resistance of low-temperature fabricated silicon junctionless transistors. a-b, Transfer characteristics of *p*-FETs (part **a**) with platinum contact and *n*-FETs (part **b**) with Sb/Ti contact, with L_{ch} of 2.9 μm (black), 900 nm (red), 400 nm (blue), and 200 nm (green), respectively. **c-d**, Width-normalized device total resistance ($R_{tot}\cdot W$) as a function of L_{ch} at varied gate overdrive ($V_{OV}=V_G-V_T$) from ±1 V to ±2.5 V from top to bottom for *p*-FETs (part **c**) and *n*-FETs (pard **d**), respectively. The *y*-axis intercepts give the parasitic contact resistance $2R_C$ as extracted based on the transmission-line method. Dashed lines represent linear fittings to the data. Error bars represent standard deviations and n=3.



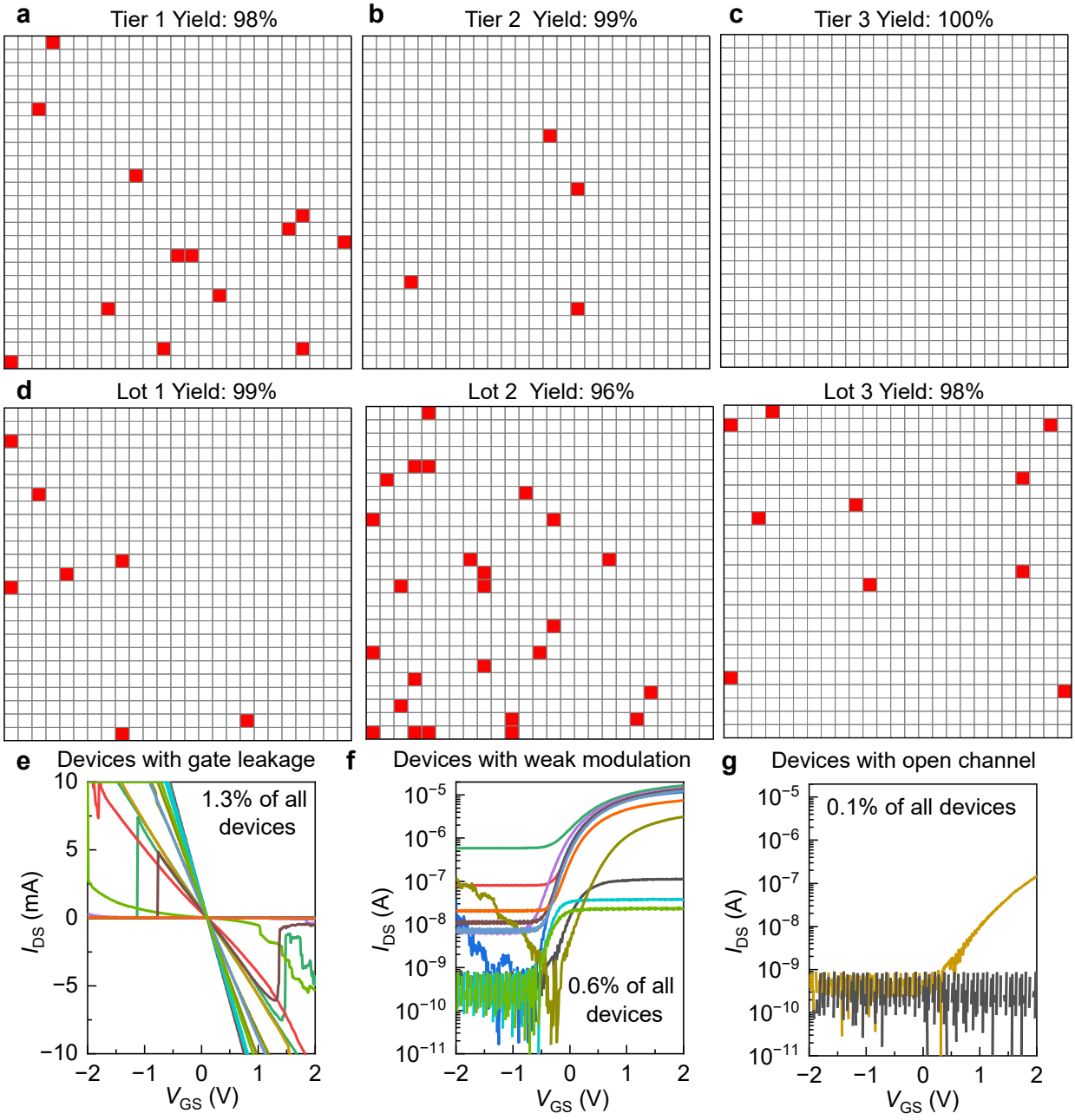
Supplementary Figure 9| DIBL in scaled junctionless transistors. **a,** Experimentally measured transfer characteristics of a junctionless transistor with L_{ch} of ~ 200 nm under applied V_{DS} of 0.5 V (black), 1.0 V (red), 1.5 V (blue), and 2.0 V (green), respectively. **b**, Device V_T extracted using the constant off-current method at 10^{-8} A·μm^{-1} as a function of applied V_{DS}. The red dashed line represents a linear fit to the data used to extract DIBL from the slope. **c,** Simulated transfer characteristics of a junctionless transistor with L_{ch} of 180 nm, under the same set of applied V_{DS} values. **d**, Simulated V_T as a function of applied V_{DS}. The red dashed line represents the linear fit used to extract DIBL.



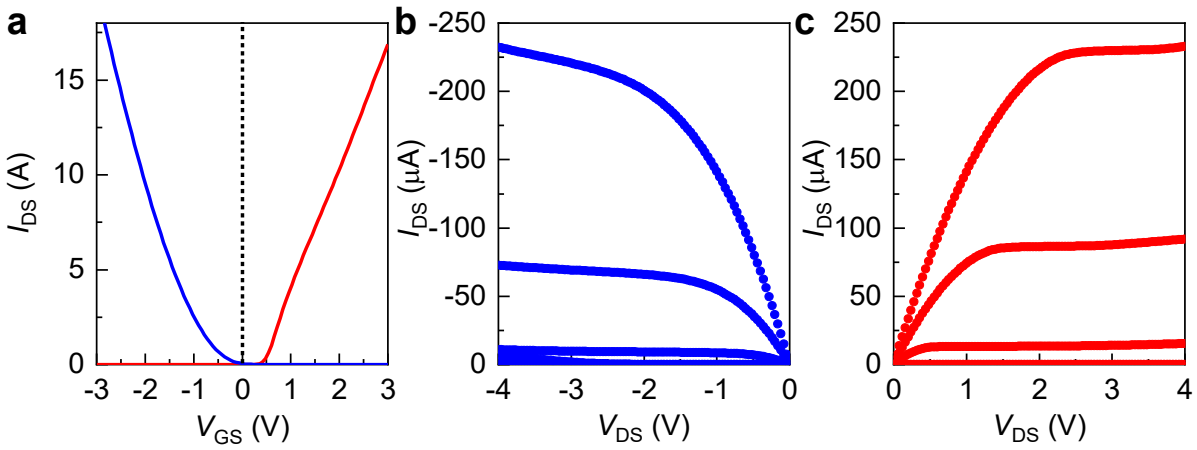
Supplementary Figure 10| Gate capacitance of fabricated junctionless transistors. **a,** Optical image of an array of circular *n*-doped silicon nanomembrane/HfO_2/Cr/Au capacitors with their radii (R) varied from 40 to 200 μm. Scale bar: 100 μm. **b**, Measured capacitance-voltage characteristics of the capacitors shown in part **a**. **c**, Capacitance (C) to πR ratio as a function of R. The red dashed line represents a linear fit to the data (black dots) to extract the capacitance per area of the native oxide (Fig. 1f inset) plus 10 nm HfO_2 stack from its slope. The y-axis intercept gives the capacitance caused by the fringing field from the edge of electrodes.



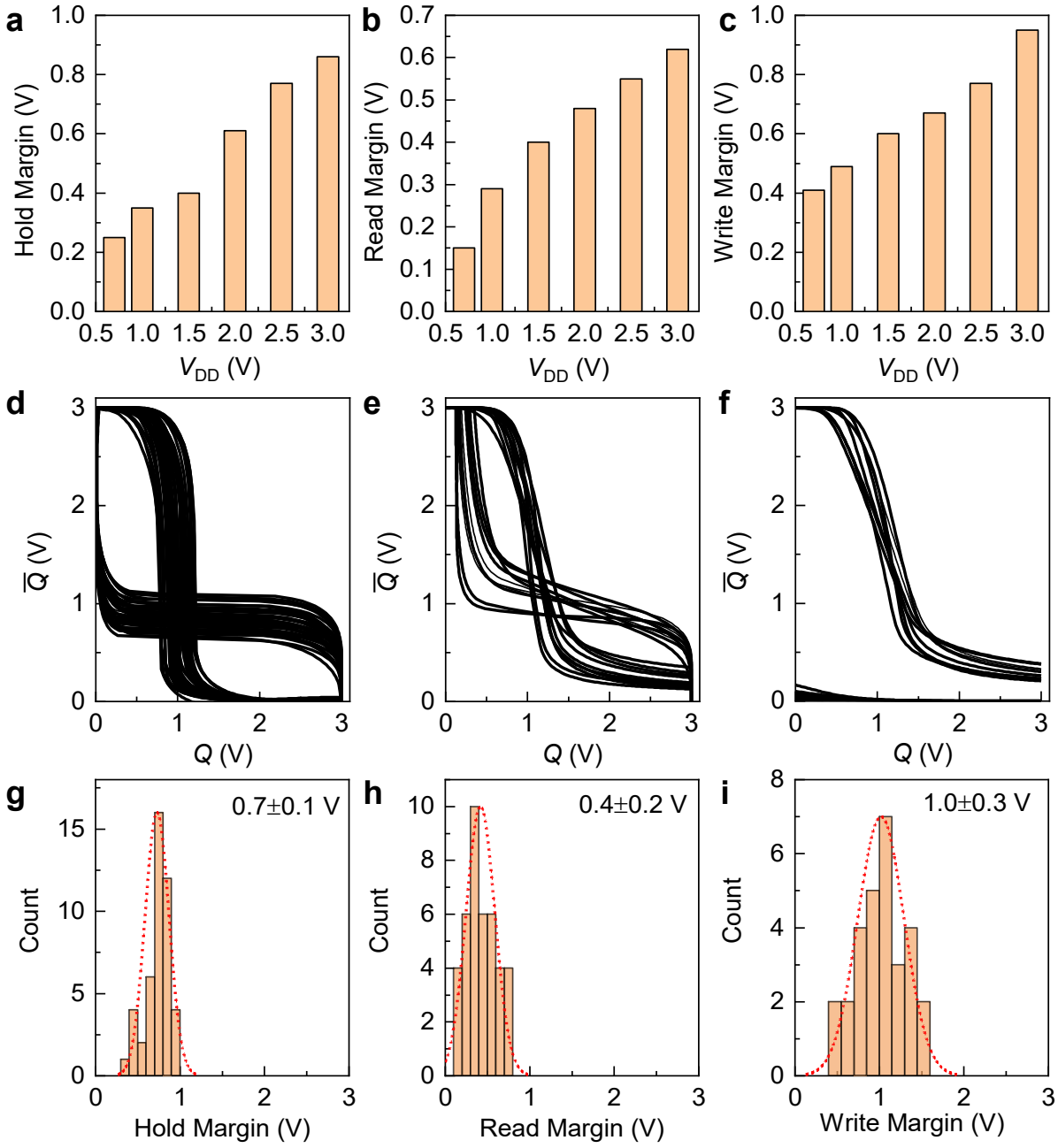
Supplementary Figure 11| Thermal stability of BEOL-compatible junctionless transistors built on transferred silicon nanomembranes. a-b, Transfer characteristics of a representative transistor measured before (black) and after forming-gas annealing at 400 °C for 15 min (red) and 60 min (blue) plotted on logarithmic (part **a**) and linear (part **b**) scales, respectively. Applied V_{DS} is 0.1 V. **c-f**, Statistical comparisons of transfer characteristics (part **c**) and their extracted effective mobility (part **d**), SS (part **e**), and V_T (part **f**) for a group of transistors measured before and after annealing. *p* values for one-way ANOVA are 0.23, 0.22, and 0.33, respectively, indicating no statistically significant difference.



Supplementary Figure 12| Yield mapping of devices across different tiers and from lot to lot. **a-c,** Maps of failed devices in tier 1 (part **a**), tier 2 (part **b**), and tier 3 (part **c**) of the wafer shown in Fig. 3. **d**, Maps of failed devices from three independent lots, each fabricated on a transferred silicon nanomembrane. Failed devices are marked in red. **e-g**, Collections of transfer curves of all failed devices because of gate leakage likely caused by surface particle contamination (part **e**), weak or ambipolar modulation (part **f**), and open devices likely resulting from lithography defects (part **g**). Each colour represents a different device.



Supplementary Figure 13| Electrical characteristics of the *p*- and *n*-FETs in a 3D vertical inverter. a, Transfer characteristics of the top-tier *p*-FET (blue) and the bottom-tier *n*-FET (red). Applied V_{DS} is 0.1 V. **b-c**, Current-voltage characteristics of the top-tier *p*-FET (part **b**) and the bottom-tier *n*-FET (part **c**). V_{GS} varied from ±3 V to 0 V from top to bottom in a step of 1 V.



Supplementary Figure 14| Noise margins of monolithic 3D SRAM cells. **a-c,** Hold (part **a**), read (part **b**), and write (part **c**) noise margins as a function of V_{DD} of the 3D SRAM cell shown in Fig. 4. **d-i,** Collections of butterfly curves (part **d–f**) and the associated statistical distributions (part **g–i**) of hold (part **d** and part **g**), read (part **e** and part **h**), and write (part **f** and part **i**) noise margins from ~30 3D SRAM cells. Red dashed lines represent Gaussian fittings to the data.