Supplementary Information

Flexible, high mobility short-channel organic thin film transistors and logic circuits based on 4H-21DNTT

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Figure S1 Absorption spectra of solution sheared thin film of 4H-21DNTT

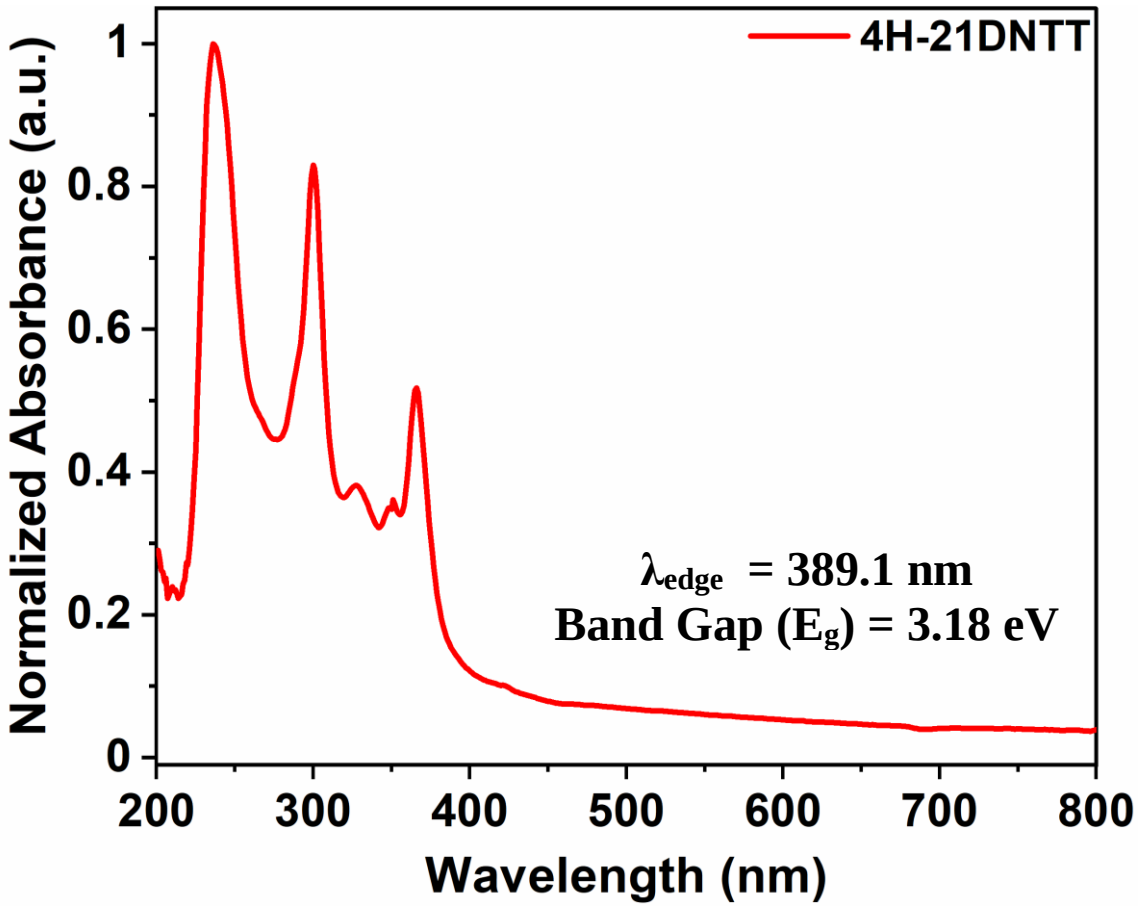

Figure S2 Transfer characteristics of 4H-21DNTT bottom-gate, bottom-contact OTFT with Parylene C as gate dielectric for different depostition conditions of 4H-21DNTT: a) v_{scan} = 32 μms^{-1} & Conc.: 0.1 wt%, b) v_{scan} = 20.5 μms^{-1} & Conc.: 0.1 wt%, c) v_{scan} = 12.5 μms^{-1} & Conc.: 0.1 wt%, d) v_{scan} = 32 μms^{-1} & Conc.: 0.09 wt%, e) v_{scan} = 20.5 μms^{-1} & Conc.: 0.09 wt% , f) v_{scan} = 12.5 μms^{-1} & Conc.: 0.09 wt%.

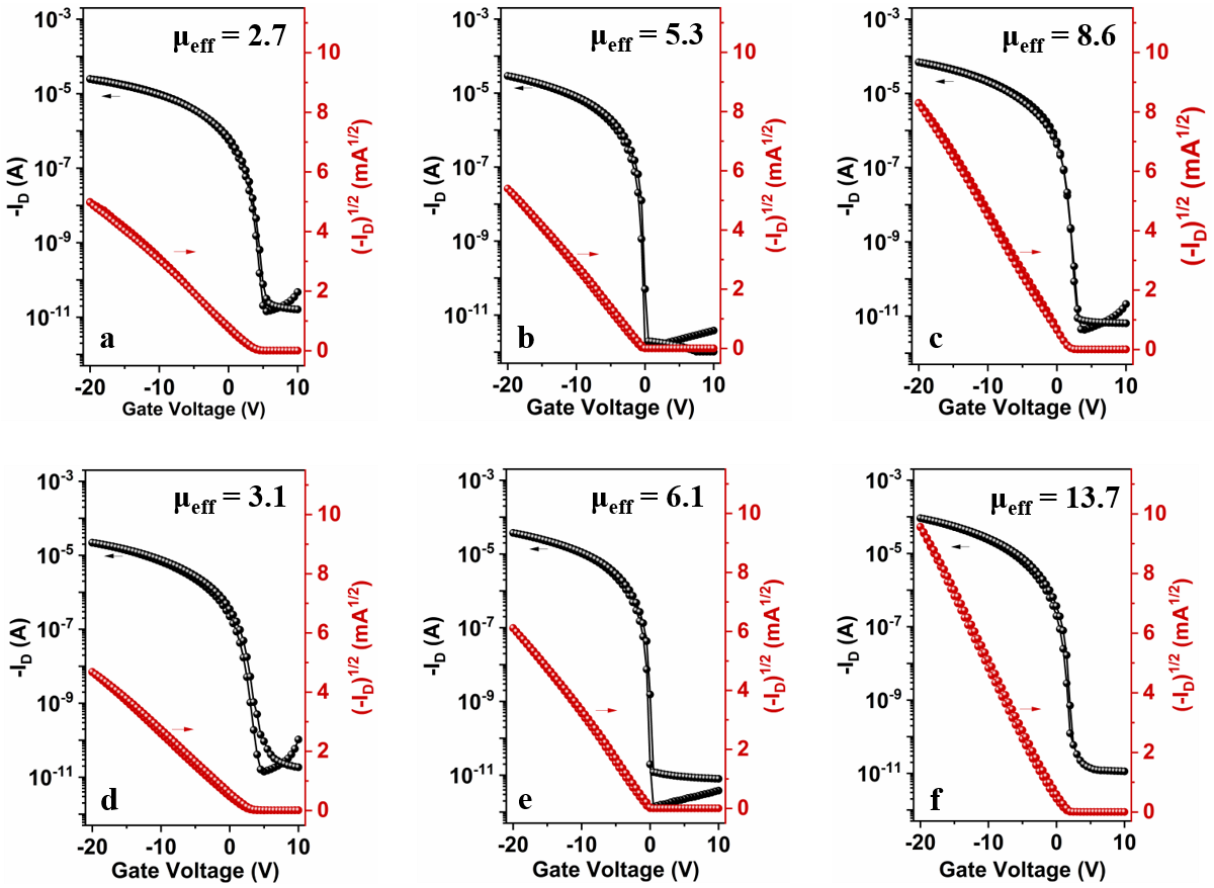

Figure S3 AFM images of 4H-21DNTT deposited by solution shearing (blade scanning speed 12.5 μms^{-1}) for two 4H-21DNTT concentrations a) 0.09 wt% film thickness was around 9 nm coreesponding to 3 monolayers. b) 0.1 wt % thick crystals upto 50 nm wwere observed.

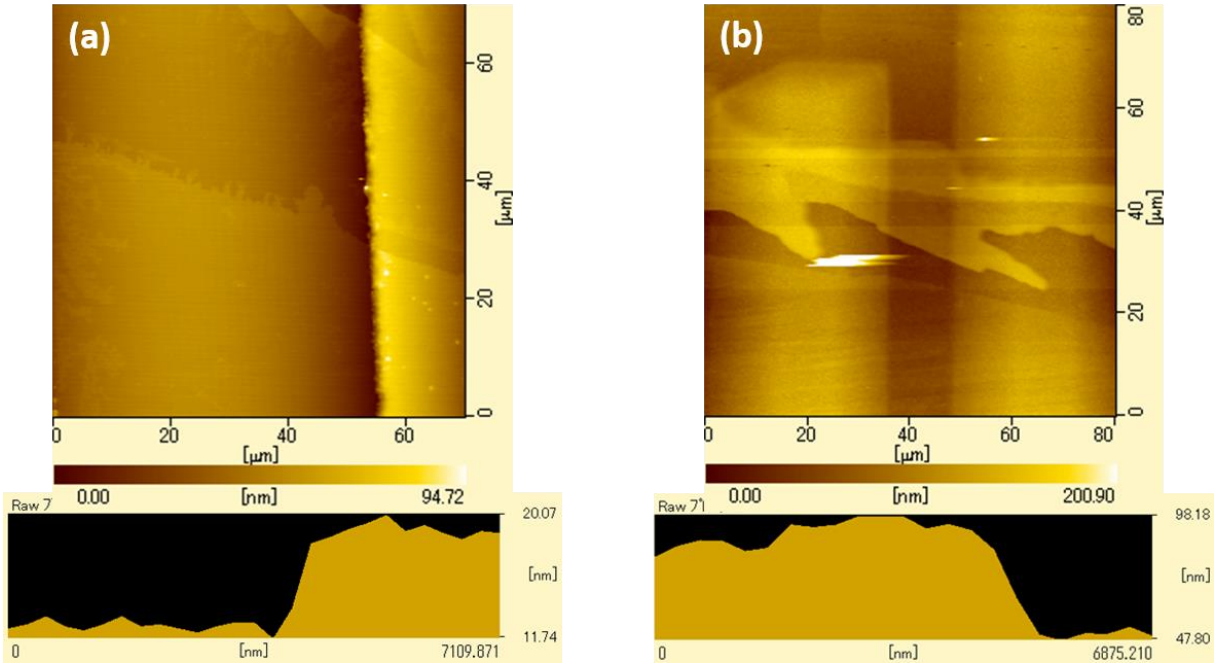

Figure S4 Transfer characteristics of 4H-21DNTT bottom-gate, bottom-contact OTFT with Parylene C as gate dielectric for channel length ranging from 10 - 120 μm.

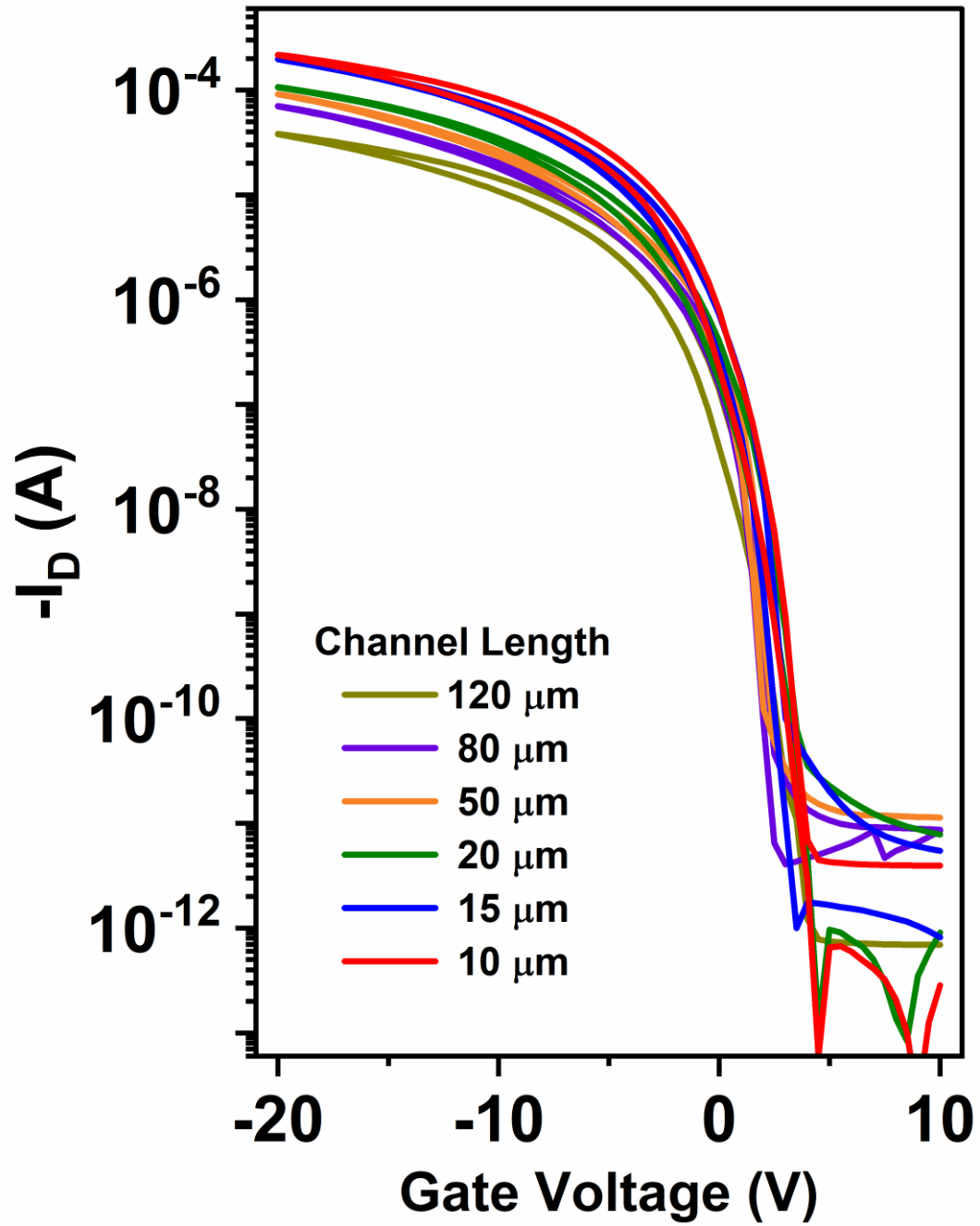

Figure S5 Statistical Variation of saturation mobility (μ_{sat}) for 4H-21DNTT OTFTs.

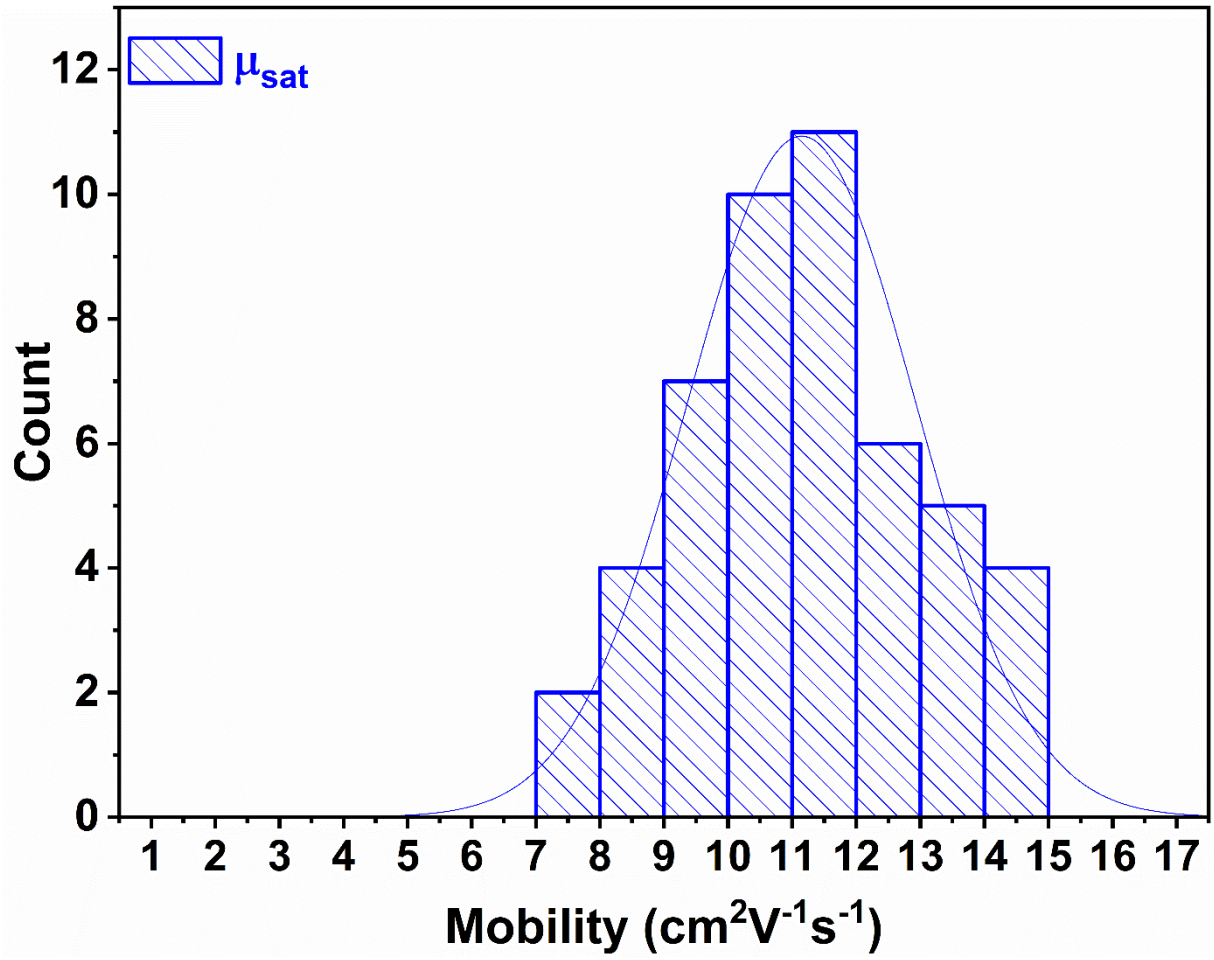

Figure S6 Literature Overview: (a) Comparision of the reported width-normalized contact resistance (R_CW) in coplanar OTFTs. (References: [1-18] in supporting information) (b) Comparision of the reported intrinsic mobility (μ_o) normalized by squared channel length (L^2) (as OTFT transit frequencies ($f_T \propto \mu_o / L^2$) for OTFTs. (References: [12-18, 39-59] in main manuscript.)

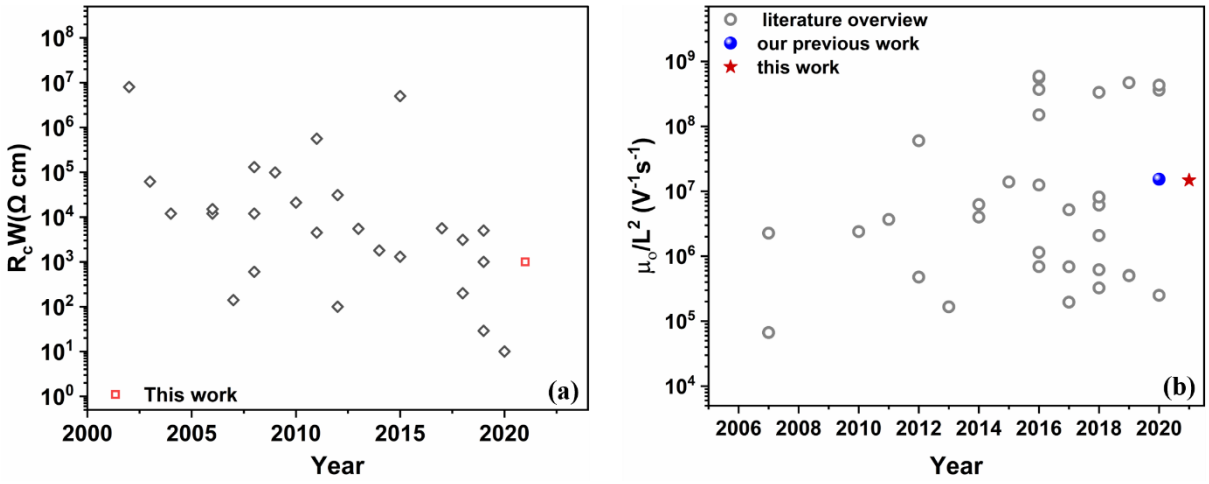

Figure S7 4H-21DNTT OTFT Contact resistance analysis for contacts without PFBT treatment: (a) Total device resistance ($R_{TOTAL}W$) plotted as a function of the channel length for OTFT for various gate overdrive voltages ($V_G - V_{TH}$). (b) Contact resistance calculated using the transmission line method (TLM) plotted as a function of gate overdrive voltages ($V_G - V_{TH}$).

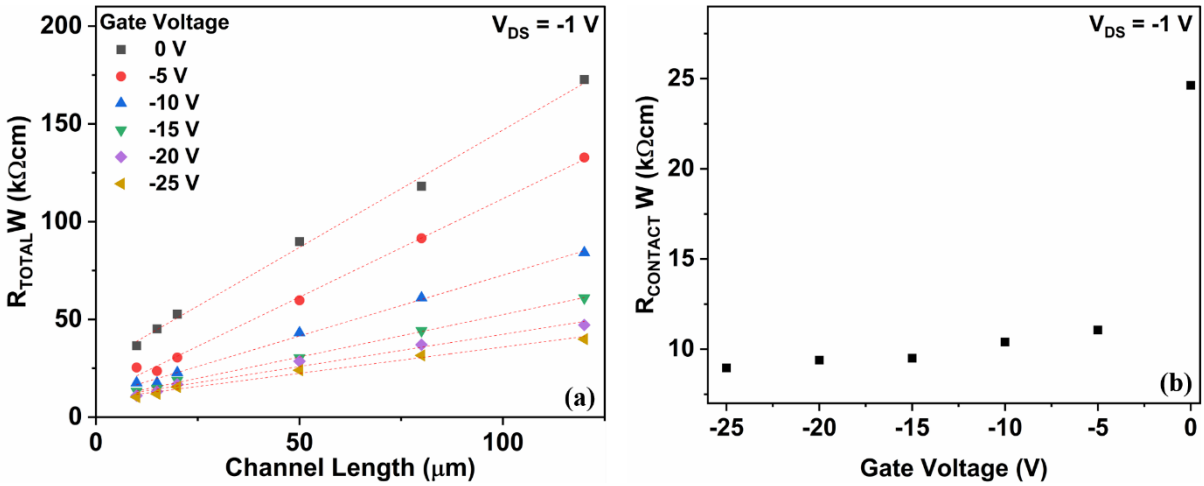

Figure S8 Stability Analysis: Transfer characteristics of 4H-21DNTT OTFTs on the Parylene C/glass substrate: black traces, freshly fabricated device; blue traces, after 30 days storage in ambient conditions (relative humidity 65% and with controlled temperature ranging from 25 ℃ to 27 ℃).

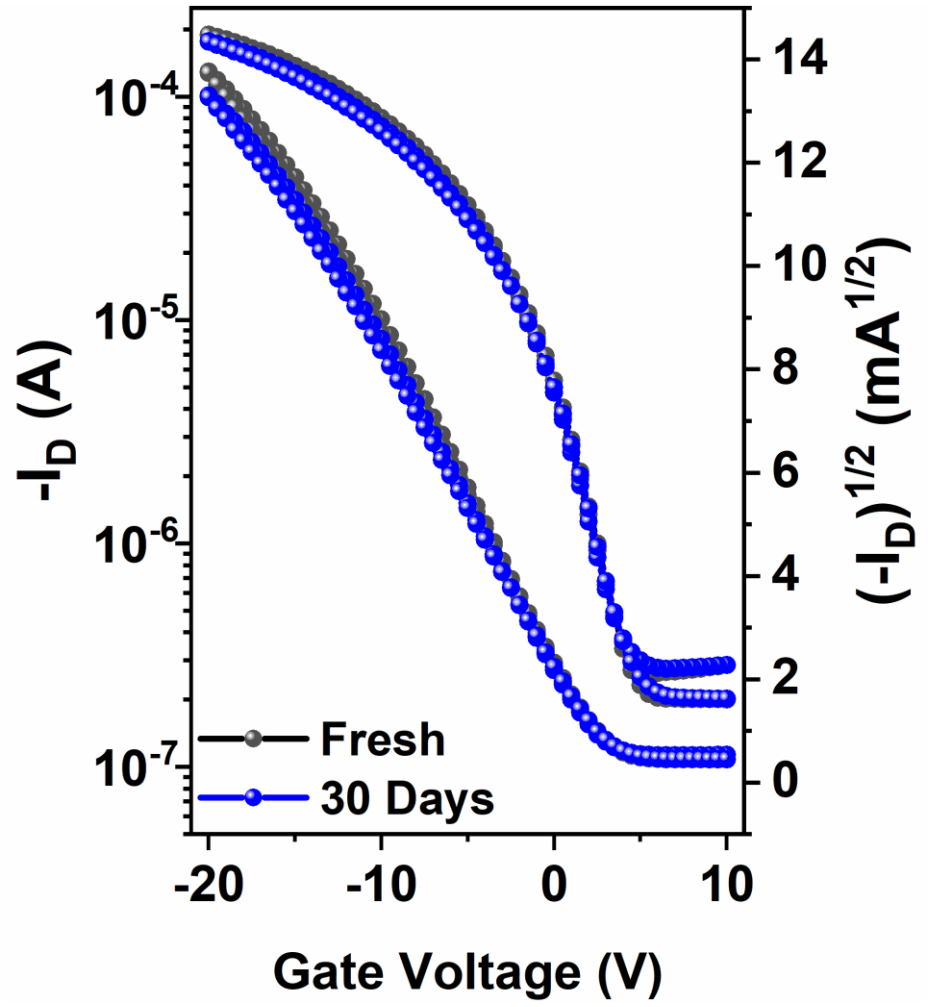

Figure S9 Zero-V_{GS}-load p-type pseudo-CMOS inverter (glass substrate) dynamic output characteristics: Calculation of rise time (τ_r i.e., when output signal changes from low to high) and fall time (τ_f i.e., when output signal changes from high to low)

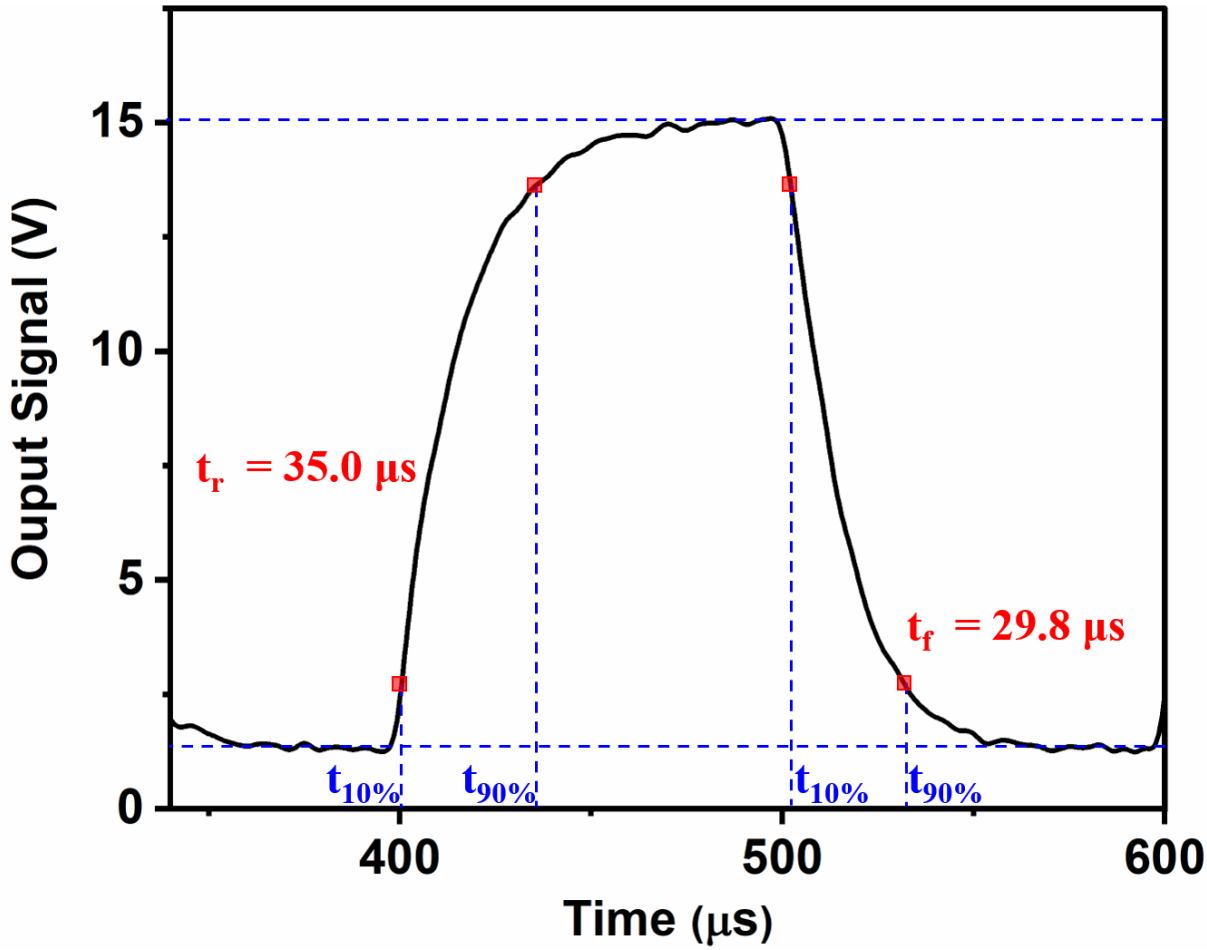

Figure S10 Zero-V_{GS}-load p-type pseudo-CMOS inverter (glass substrate) dynamic output characteristics: Calculation of propagation delay (τ)

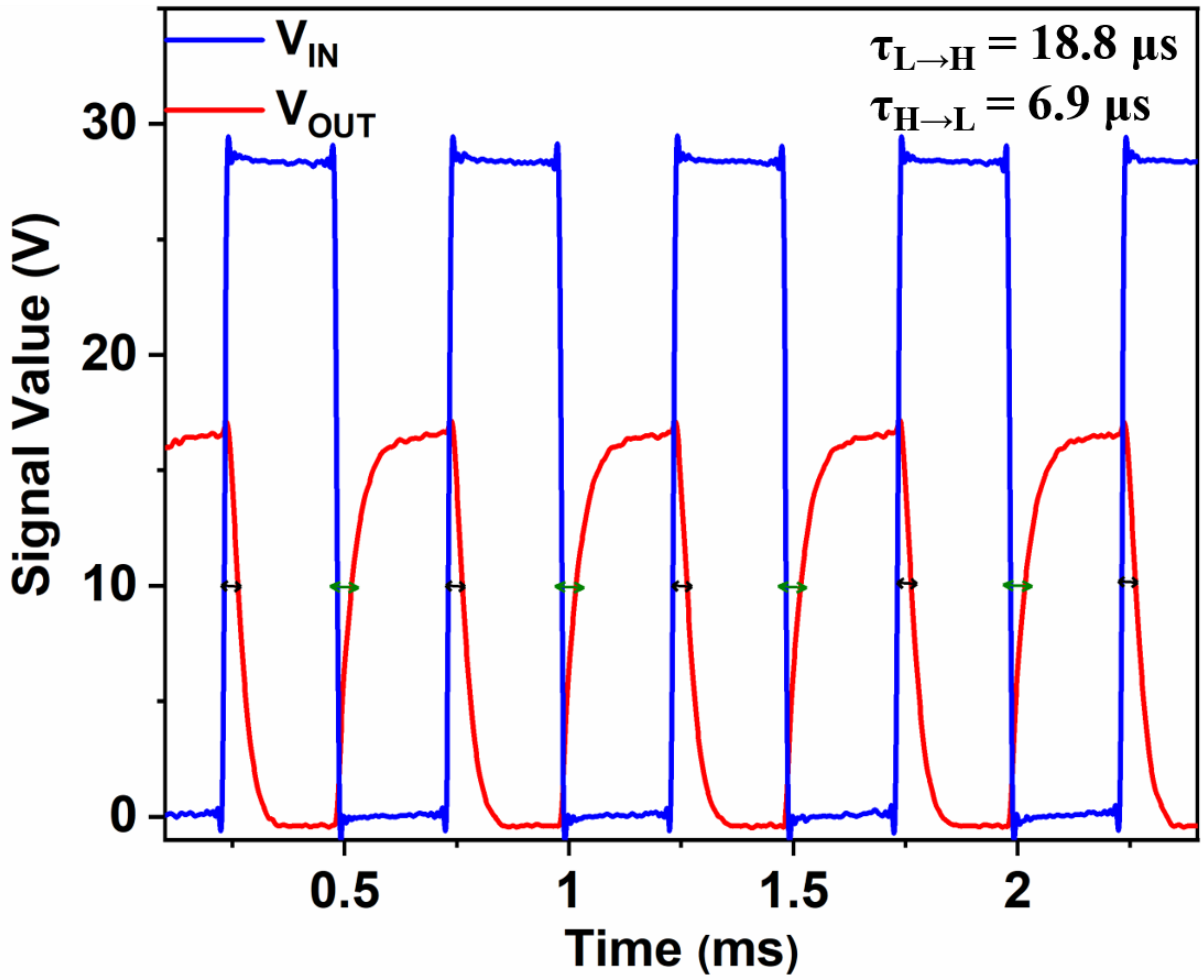

Figure S11 Zero-V_{GS}-load p-type pseudo-CMOS inverter (flexible PEN substrate) output characteristics (a) Measured output voltage (V_{OUT}) and small-signal gain as a function of input voltage (V_{IN}) for supply voltages (V_{DD}) between -10 and -20 V. (b) Dynamic response of zero-V_{GS}-load p-type pseudo-CMOS inverter with input signal frequency of 1 kHz

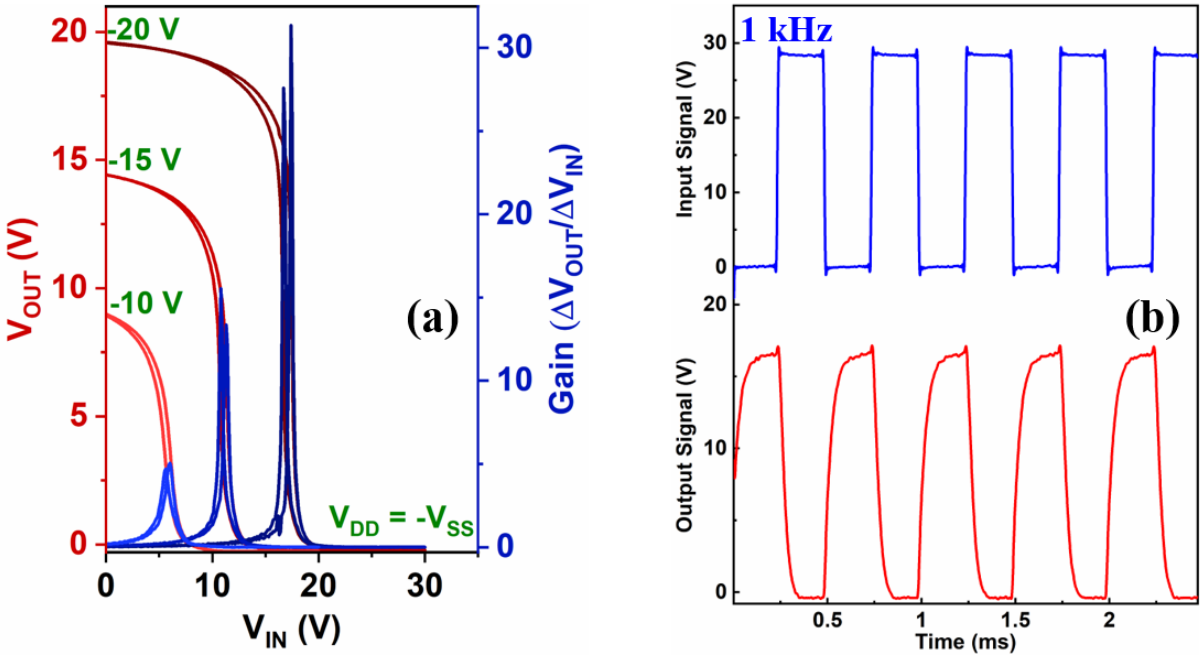

Figure S12 Zero-V_{GS}-load p-type pseudo-CMOS inverter (flexible PEN substrate) dynamic output characteristics: Calculation of rise time (τ_r i.e., when output signal changes from low to high) and fall time (τ_f i.e., when output signal changes from high to low)

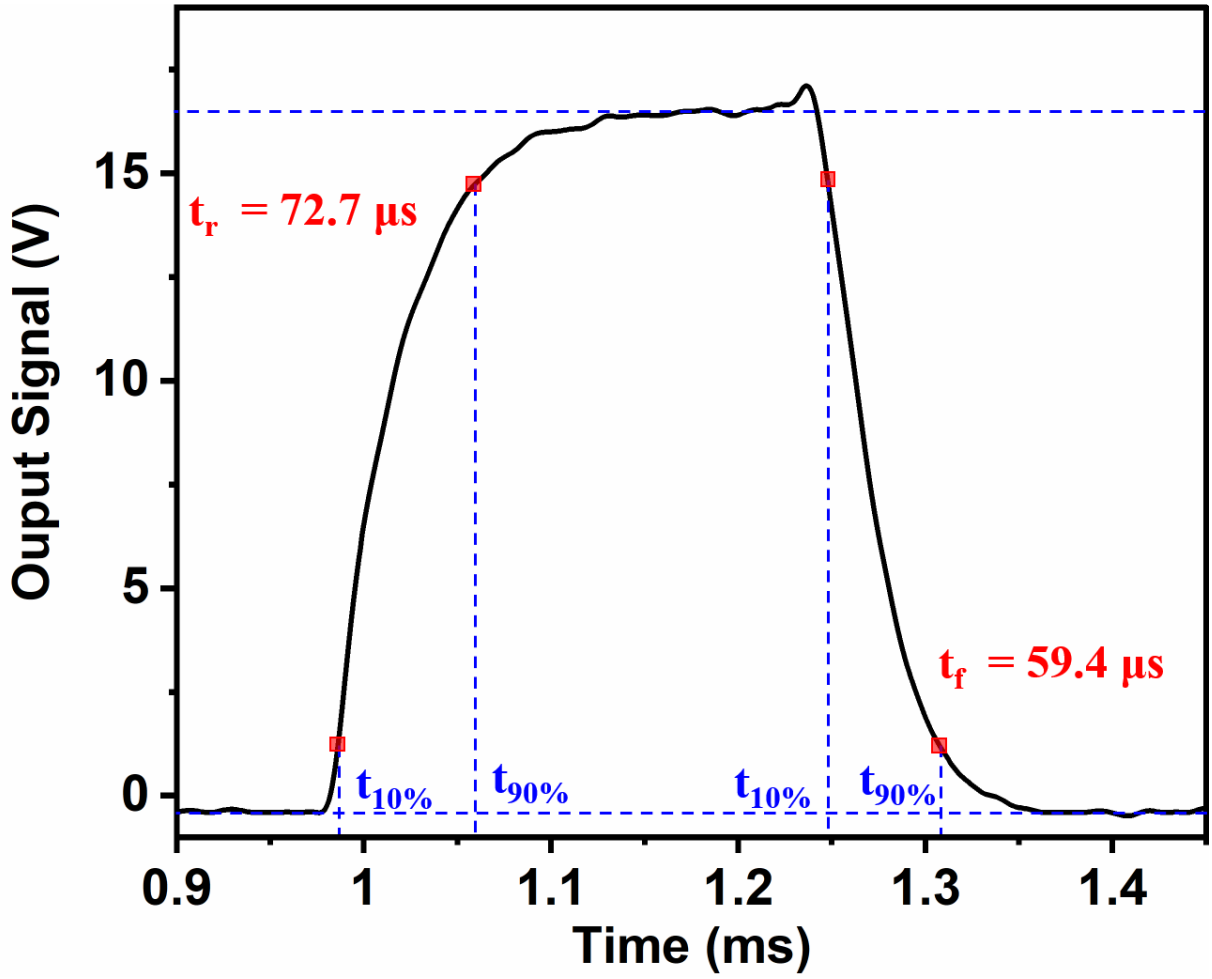

Figure S13 Zero-V_{GS}-load p-type pseudo-CMOS inverter (flexible PEN substrate) dynamic output characteristics: Calculation of propagation delay (τ).

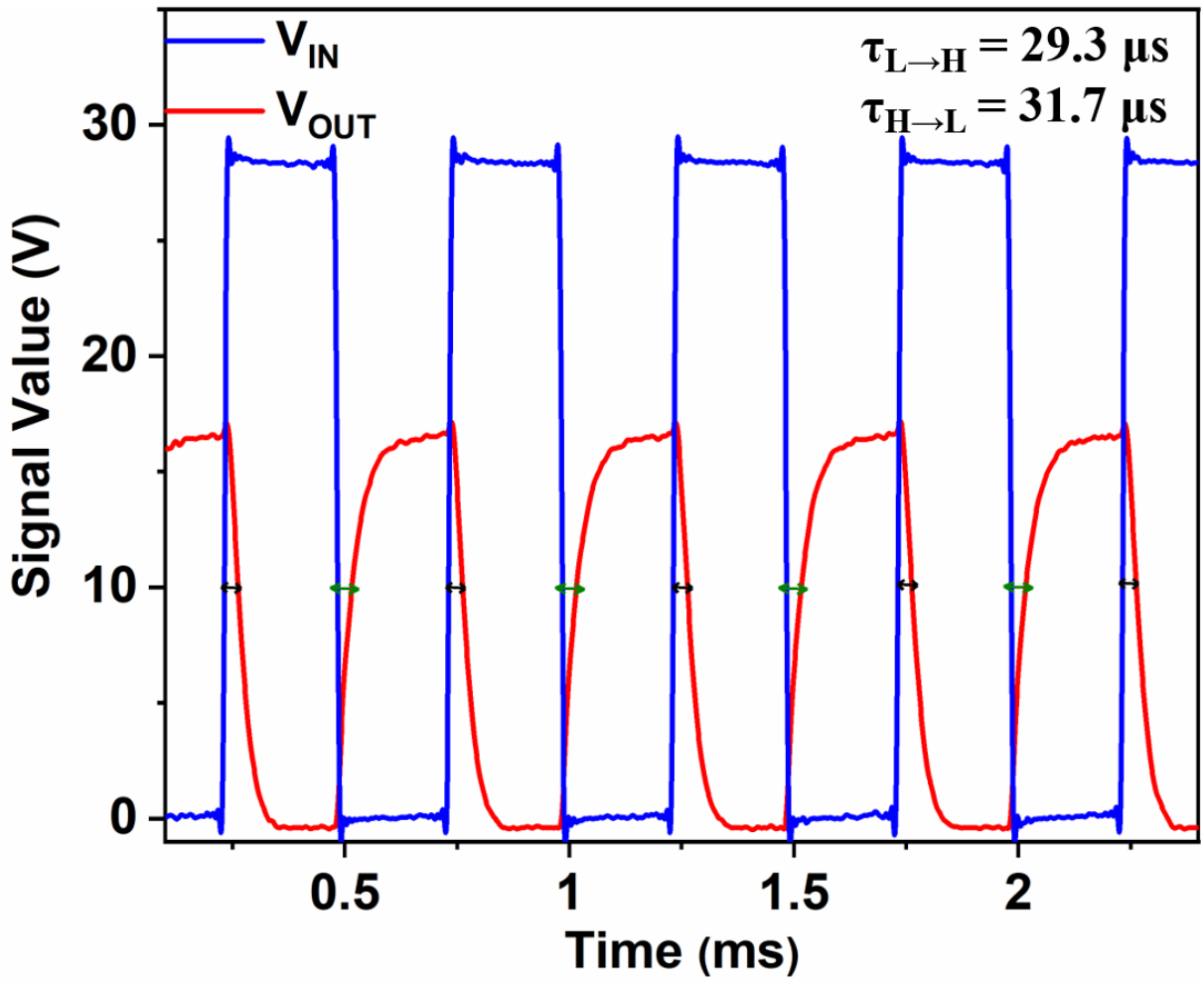

Figure S14 NAND logic circuit based on zero-V_{GS}-load p-type pseudo-CMOS design (glass substrate) dynamic output characteristics: Calculation of rise time (τ_r i.e., when output signal changes from low to high) and fall time (τ_f i.e., when output signal changes from high to low)

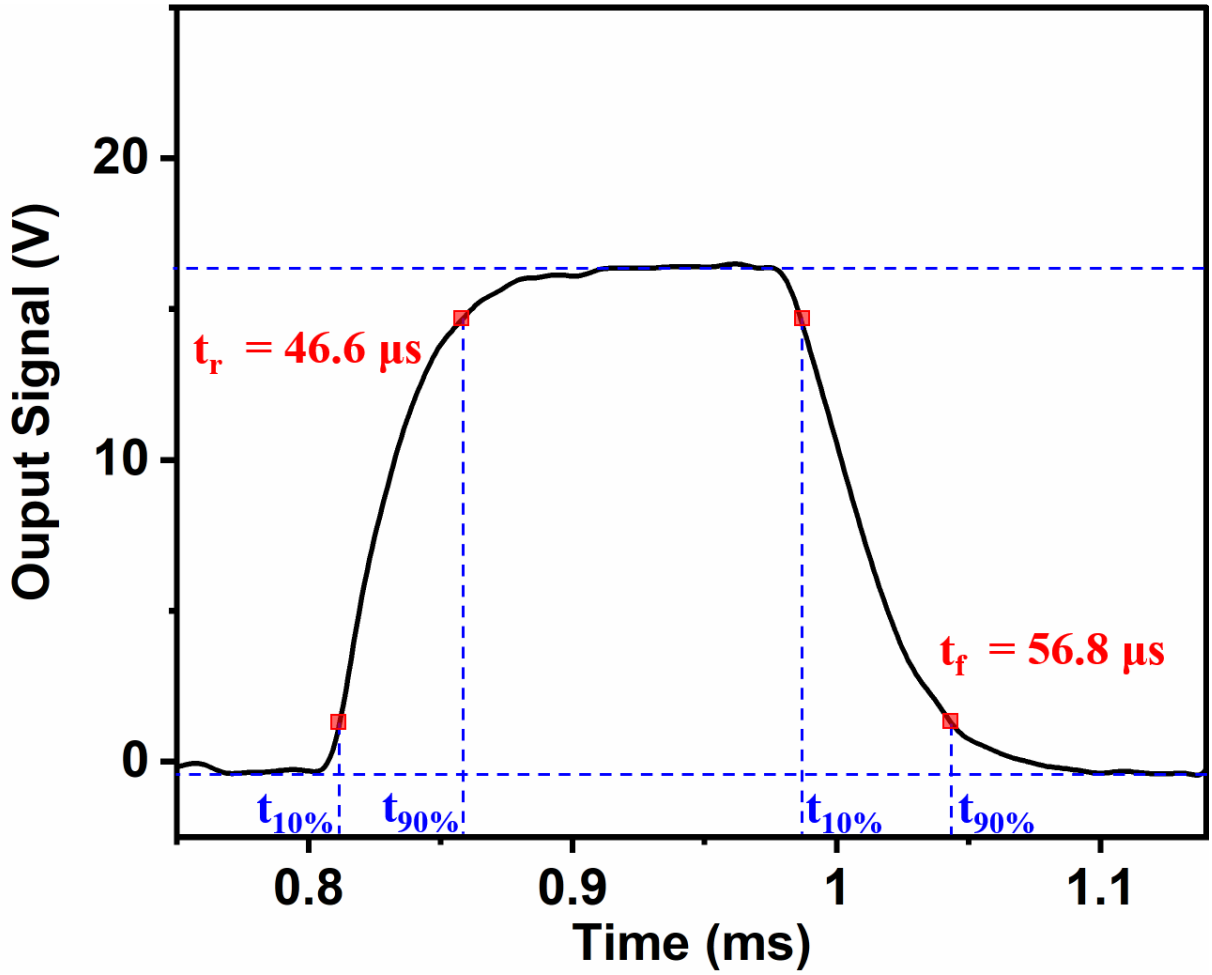

Figure S15 NAND logic circuit based on zero-V_{GS}-load p-type pseudo-CMOS design (glass substrate) dynamic output characteristics: Calculation of propagation delay (τ).

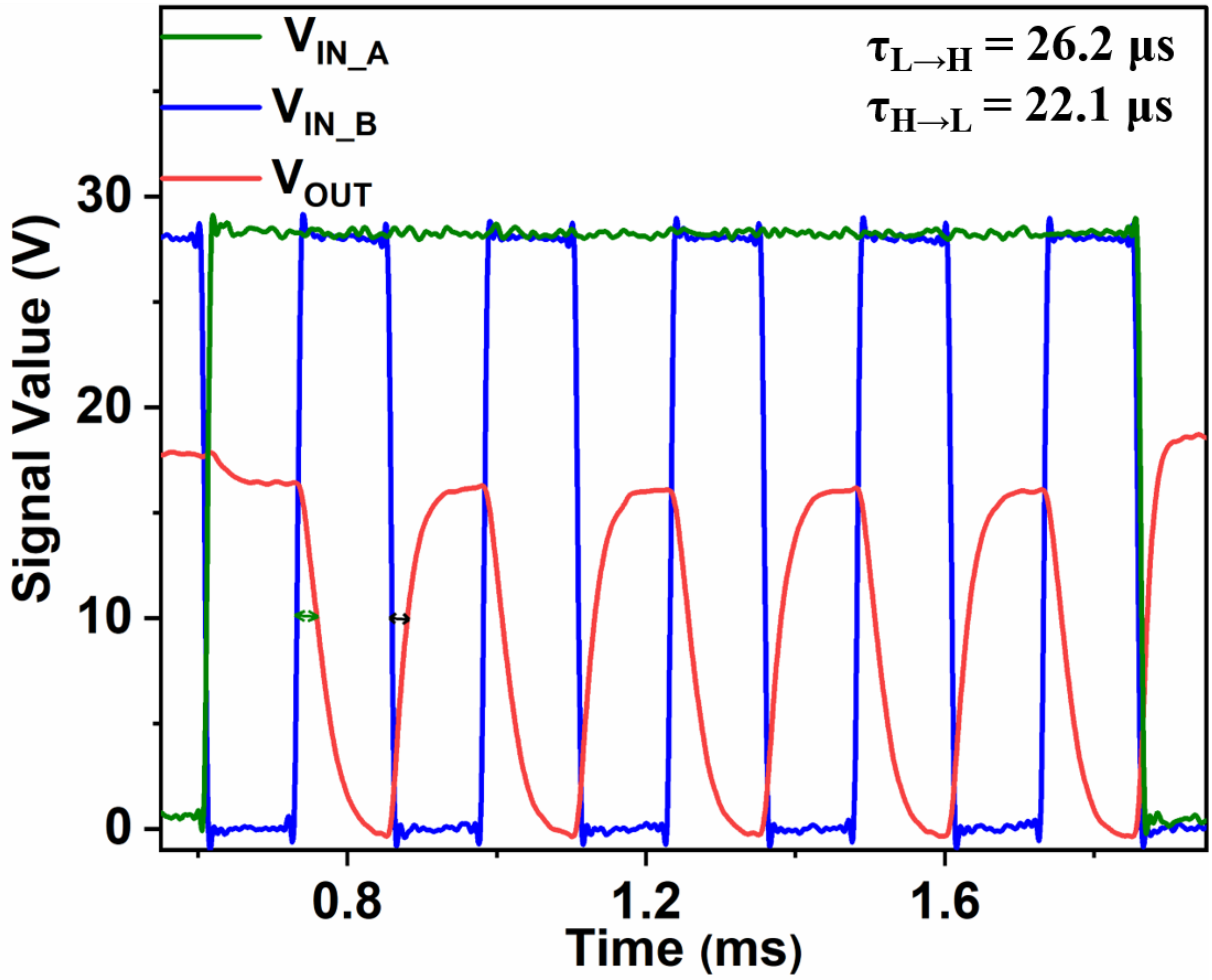

Figure S16 NAND logic circuit based on zero-V_{GS}-load p-type pseudo-CMOS design (flexible PEN substrate) output characteristics (a) Measured output voltage (V_{OUT}) and small-signal gain as a function of input voltage (V_{IN}) for supply voltages (V_{DD}) between -10 and -20 V. (b) Dynamic response of NAND logic circuit with input signals of frequencies V_{IN_A} = 150 Hz and V_{IN_B} = 1.5 kHz.

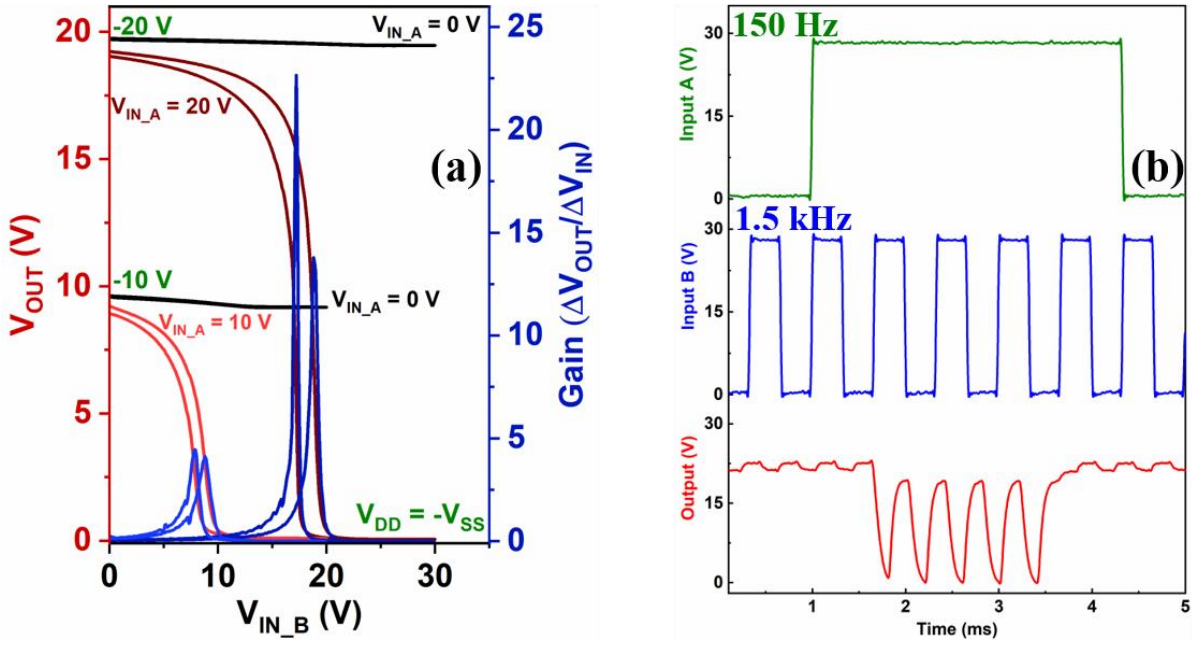

Figure S17 NAND logic circuit based on zero-V_{GS}-load p-type pseudo-CMOS design (glass substrate) dynamic output characteristics: Calculation of rise time (τ_r i.e., when output signal changes from low to high) and fall time (τ_f i.e., when output signal changes from high to low)

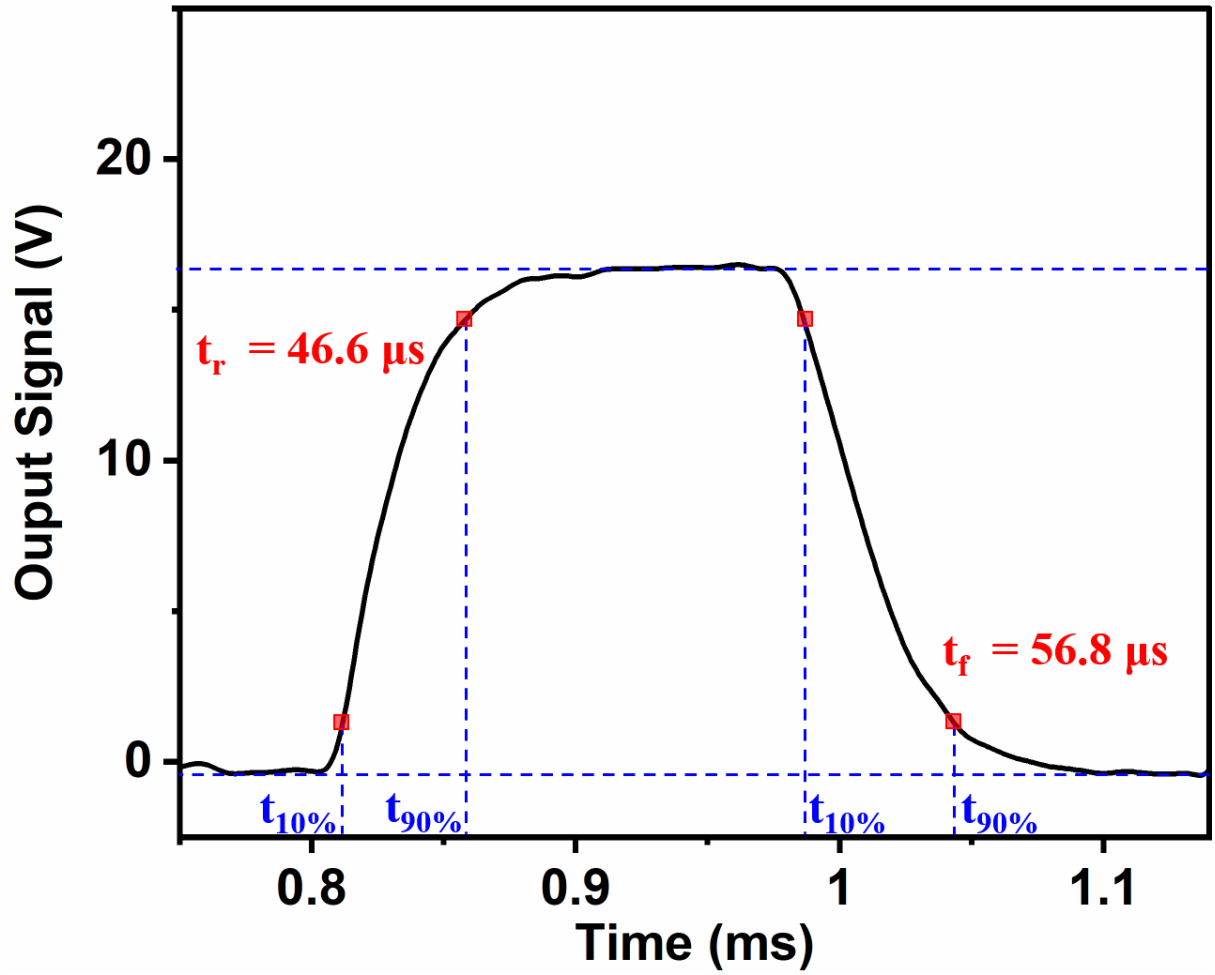

Figure S18 NAND logic circuit based on zero-V_{GS}-load p-type pseudo-CMOS design (flex PEN substrate) dynamic output characteristics: Calculation of propagation delay (τ).

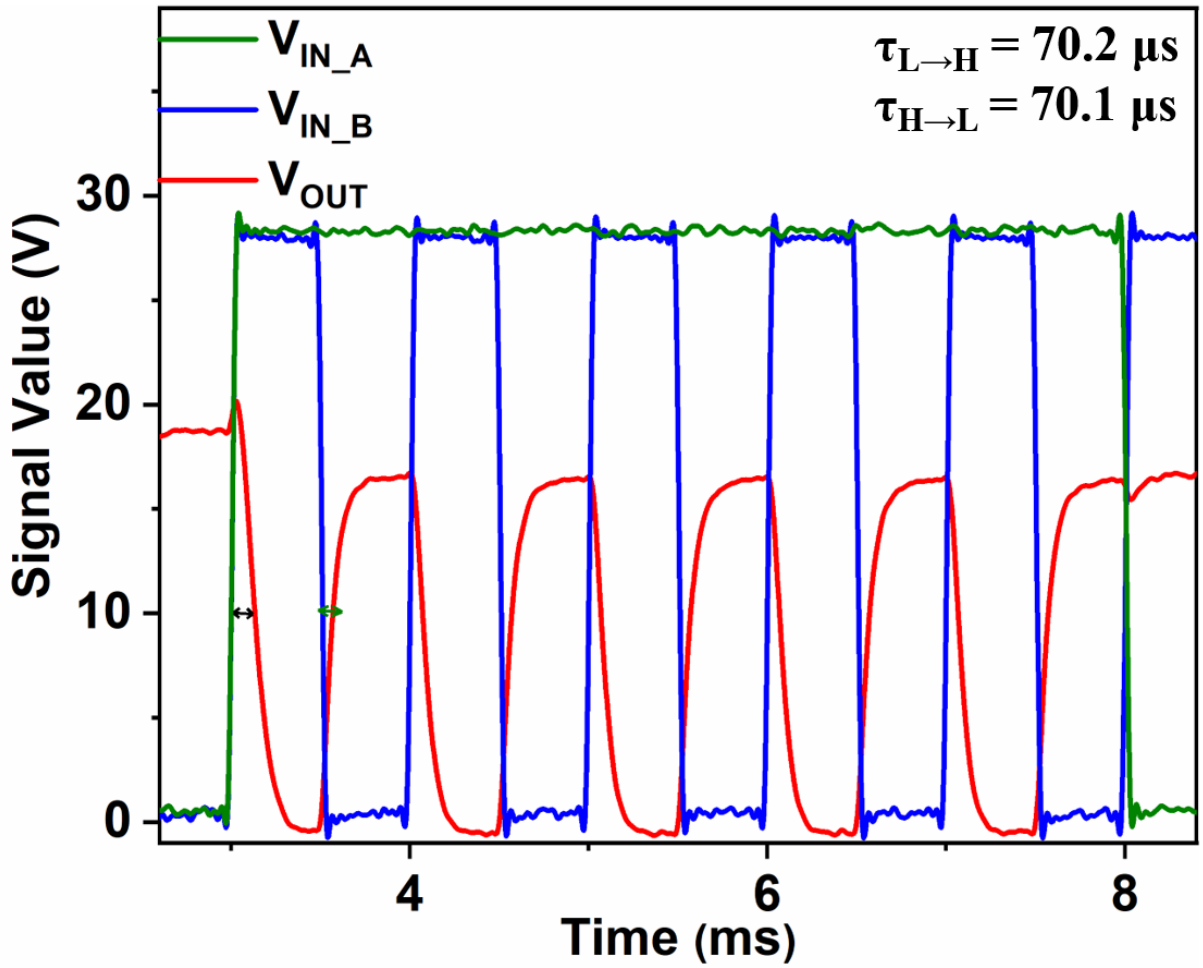

Table S1 OTFT circuit dynamic performance: Comparision of propgation delay for inverter based circuits with solution processed OTFT.

Parameters	[1]	[2]	[3]	[4]	[5]	This work
L (μm)	NA	21	5	29	5	15
OSC Deposition Method	Edge casting	Inkjet & Dispenser	Inkjet	Inkjet & Dispenser	Zone casting	Solution shearing
Circuit design schematic	CMOS	CMOS	Pseudo-CMOS	CMOS	Pseudo-CMOS	Pseudo-CMOS
H→L Propagation Delay (ms)	0.025 (D Flip Flop)	1.9 (Inverter) 2.7 (NAND)	0.16 (Inverter) 1.5 (NAND)	0.34 (Inverter)	0.042 (Inverter)	0.028 (Inverter) 0.068 (NAND)
L→H Propagation Delay (ms)	NA	1.2 (Inverter) 1.3 (NAND)	0.11 (Inverter) 0.1 (NAND)	NA	NA	0.023 (Inverter) 0.063 (NAND)

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