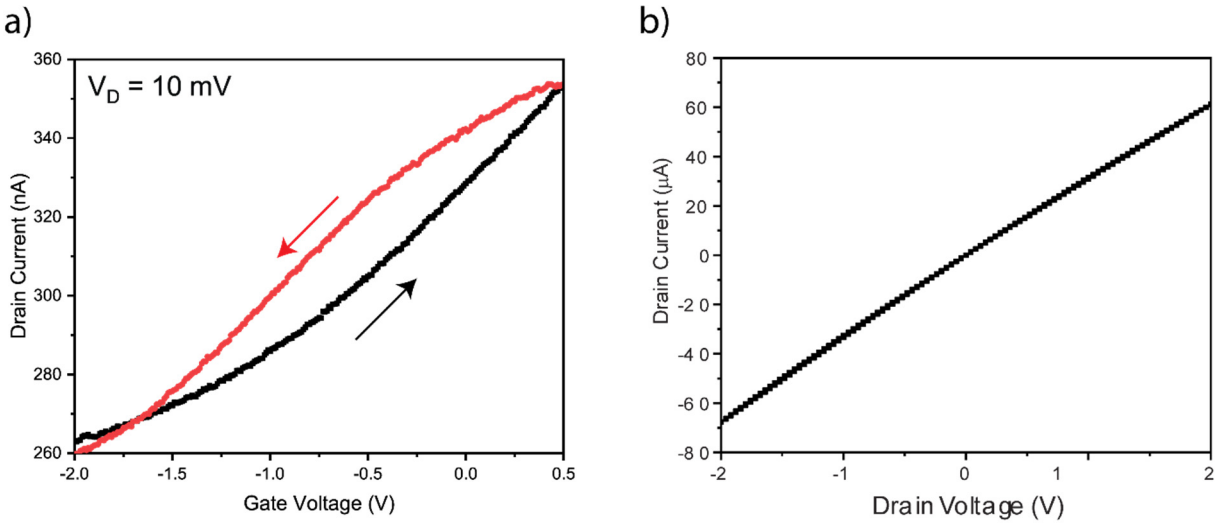
Supplementary Information

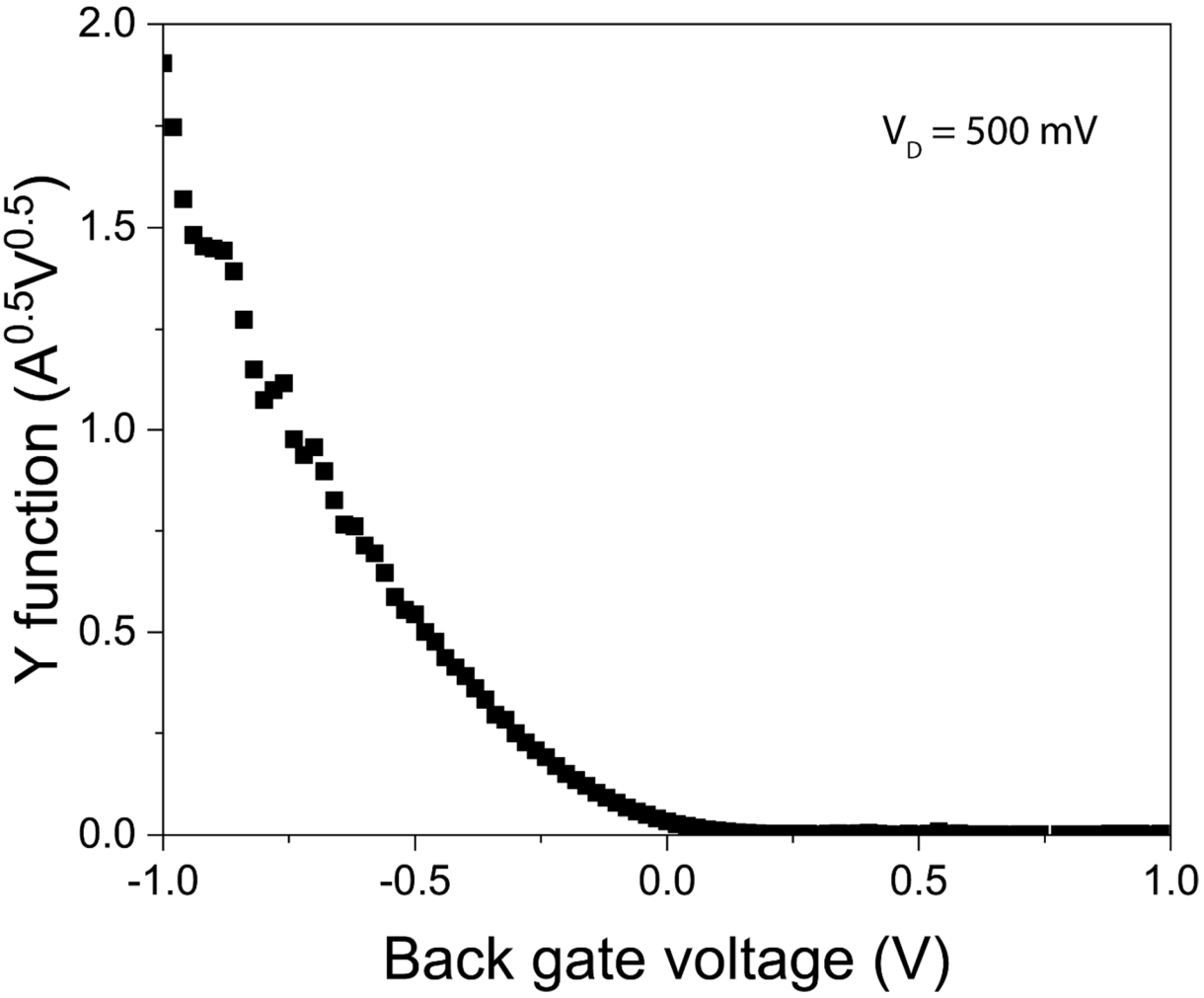
1. $SnSe_2$ FET electrical characterization.

The double sweep transfer characteristic of a representative $SnSe_2$ FET measured applying a drain to source bias of 10 mV is shown in Supplementary Figure 1a. As expected, given the degenerate n doping typical of this material, the gate has a very limited capability of modulating the conduction in the channel[1,2], that cannot be depleted of electrons in the investigated gate bias window resulting in a ON/OFF current ratio smaller than two. Supplementary Figure 1b reports the output characteristic of the $SnSe_2$ FET under zero gate bias: a linear ohmic contact is achieved between the Pd contacts and the multilayer $SnSe_2$ flake.



Supplementary Figure 1. a $SnSe_2$ FET double sweep transfer characteristic in linear scale, showing a very limited control of the gate bias on the channel conductance. The drain bias is 10 mV. **b** Output characteristic, demonstrating how a ohmic contact is achieved between $SnSe_2$ and the Pd electrodes. In this measurement the gate bias is set at zero volt.

2. WSe_2 low field mobility estimation through Y function method



Supplementary Figure 2. Y function obtained from the WSe_2 FET discussed in the main manuscript whose transfer characteristic has been measured at V_{DS} = 500 mV. From the fitting of the linear part of the curve it is possible to estimate the hole mobility.

The low field hole mobility of the WSe_2 discussed in the main text can be estimated applying the Y-function method to at least partially remove the effect of the series resistance introduced by the metal electrodes[3,4]. Assuming that the contact resistance is not strongly dependent on the gate bias, the Y function expression reduces to:

$$Y = \frac{I_{\mathrm{D}}}{\sqrt{g_{\mathrm{m}}}} = \sqrt{\frac{\mu_{0,eff} C_{\mathrm{ox}} |V_{\mathrm{DS}}| W}{L}} (V_{\mathrm{G}} - V_{\mathrm{T}})$$

where C_{ox} is the gate capacitance per unit area and V_T is the WSe_2 threshold voltage. The resulting Y function as a function of the back gate bias for the WSe_2 FET discussed in the main manuscript measured at V_D = 500 mV is shown in Supplementary Figure 2. The carrier mobility is then given by:

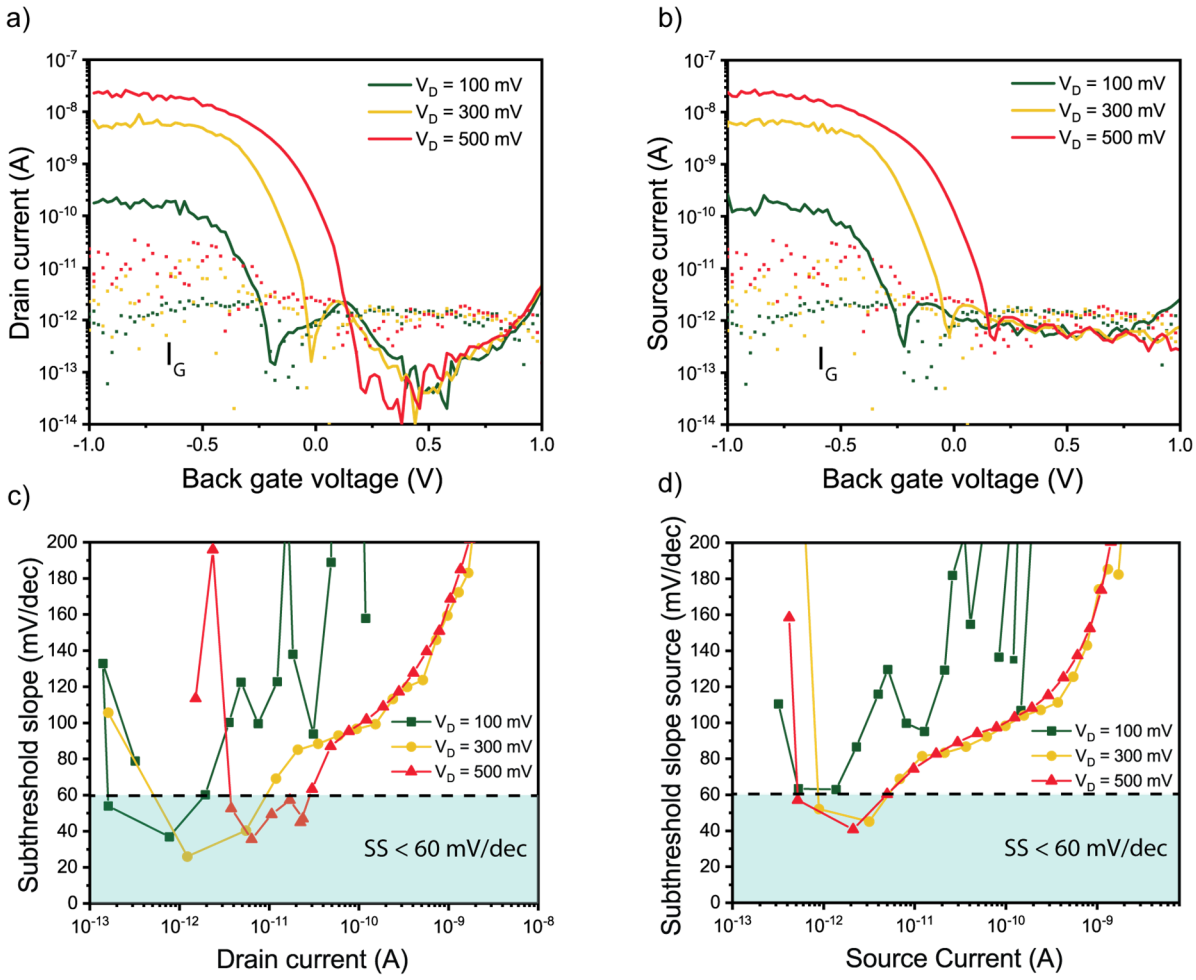
$$\mu_{0,eff} = \frac{L}{C_{ox} |V_{DS}| W} \left(\frac{\partial Y}{\partial V_G}\right)^2$$

Replacing the derivative with the slope of the linear part of the Y function in Supplementary Figure 3 it is possible to estimate the carrier mobility. The oxide capacitance per unit area was accurately estimated by characterizing MIM capacitors fabricated on the same substrate and with the same

process as for our final device. The estimated dielectric constant is equal to 12[5]. We obtained a hole mobility of 1.8 $cm^2V^{-1}s^{-1}$, comparable to results shown in in literature for similar device structures[6–8].

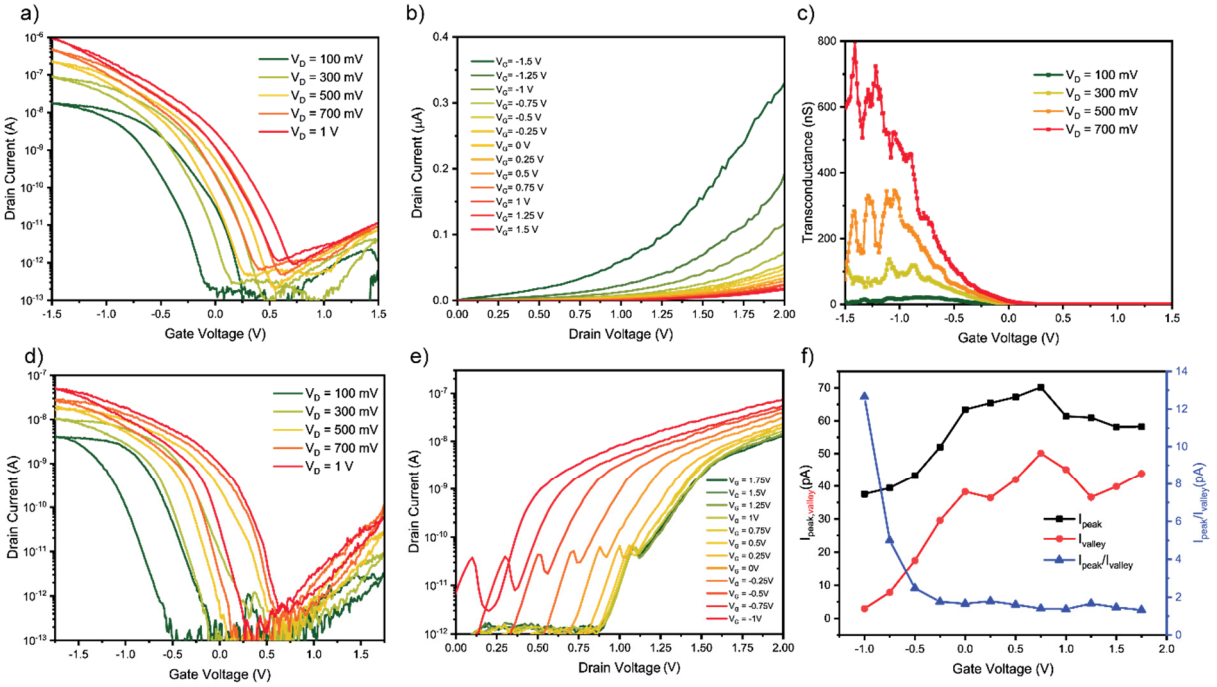
3. $WSe_2/SnSe_2$ TFET: source and drain current subthreshold slopes.

Supplementary Figure 3 collects the $WSe_2/SnSe_2$ TFET transfer characteristic for both the drain (a) and source currents (b). The resulting subthreshold slopes are shown respectively in Supplementary Figure 2c and 2d. It is important to underline that both drain and source currents reach subthreshold point swing below the 60 mV/dec room temperature Boltzmann limit, providing a strong indication of the onset of a robust BTBT process.



Supplementary Figure 3. **a** Drain and **b** source transfer characteristics of the $WSe_2/SnSe_2$ TFET discussed in the main manuscript. The dotted line is the gate leakage current. Both the subthreshold slope curves (**c** and **d**) achieve subthermionic point swings for similar ranges of the output current, providing further proof of the onset of a robust BTBT current conduction.

4. WSe_2 FET and $WSe_2/SnSe_2$ FET electrical characterization.



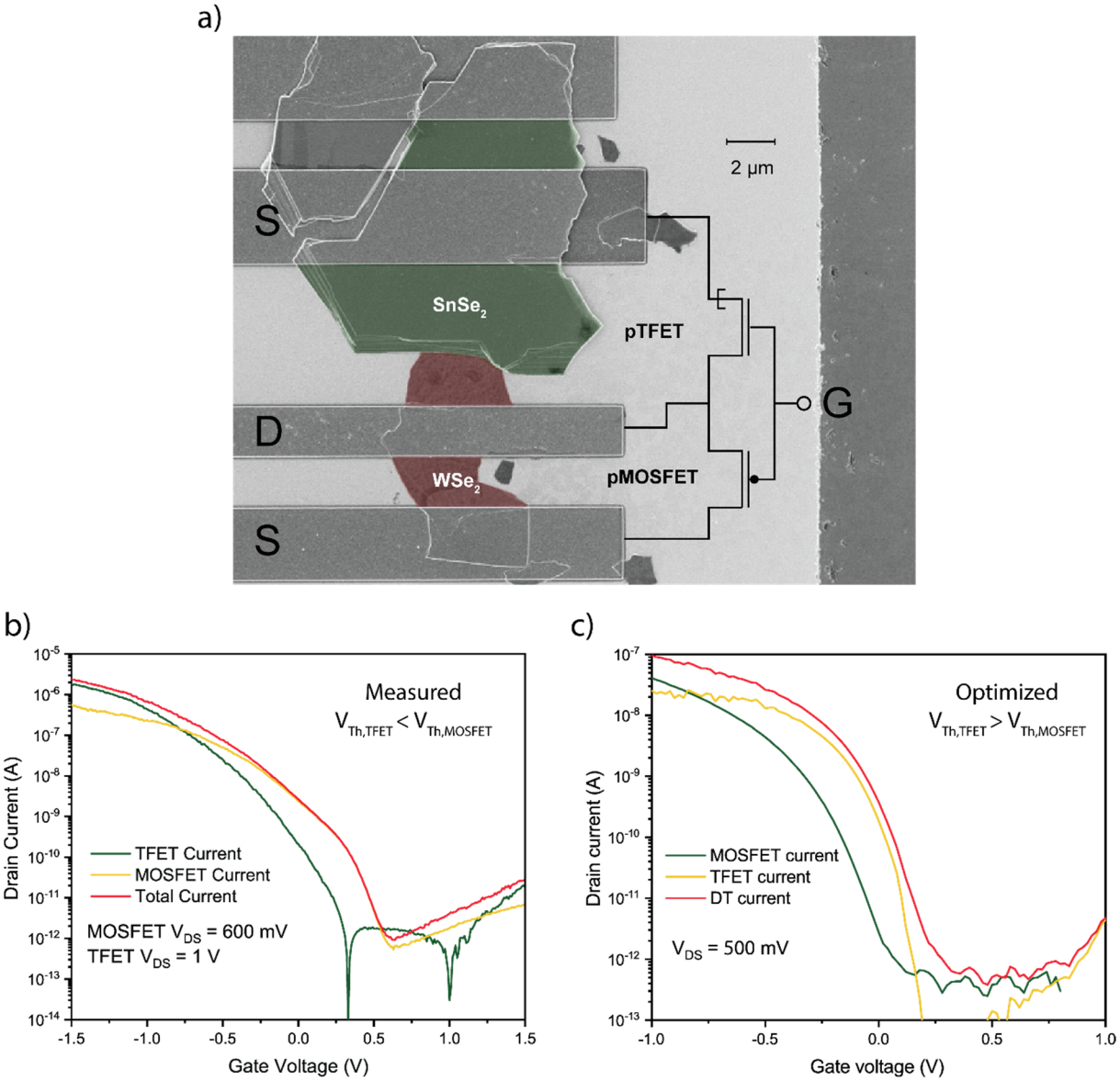
Supplementary Figure 4. Electrical characterization of a second WSe_2 FET and the $WSe_2/SnSe_2$ heterojunction device fabricated on the very same flake. **a** Transfer characteristic in semilogarithmic scale of the WSe_2 FET for increasing values of the drain bias. The ON/OFF current ratio is larger than 10^6 and the average subthreshold slope ranges from 90 to 110 mV/dec. **b** WSe_2 FET output characteristic in linear scale, showing a non-saturating behavior attributable to the Schottky nature of the Pd/WSe_2 contact. **c** Transconductance of the WSe_2 FET, saturating in the -0.5 V/-1 V gate bias range. **d** Transfer characteristic in semilogarithmic scale of the same flake $WSe_2/SnSe_2$ TFET for increasing values of the drain bias. The threshold voltage is shifted to more negative values with respect to the WSe_2 FET, while the turn-on slope is improved. **e** Output characteristic in semilogarithmic scale of the TFET at different values of the gate bias in the -1 V/1.75 V range. A clear negative differential resistance region is observed. **f** Evolution of peak, valley and peak to valley current ratio as a function of the gate voltage. These images are based on the data presented at IEDM 2019[9].

Supplementary Figure 4a shows the double sweep transfer characteristic of a second WSe_2 FET for different values of the drain bias. The device exhibits p-type polarity, with ON/OFF current ratio larger than 10^6 and hysteresis below 250 mV for a drain voltage as little as 100 mV. The average subthreshold slope ranges from 90 to 110 mV/dec. The output characteristic in Supplementary Figure 4b shows the Schottky nature of the Pd/WSe_2 contact, resulting in a non saturating drain current in the considered range of gate biases. Finally, the FET gate transconductance g_m is shown in Supplementary Figure 4c: the peak and saturation is reached in the -0.5 V and -1 V gate bias window.

The double sweep transfer characteristic of the same flake $WSe_2/SnSe_2$ TFET for increasing values of the drain voltage is reported in Supplementary Figure 4d. With respect to the WSe_2 FET, the heterojunction device exhibits a threshold voltage shifted by 250 mV to more negative values, with comparable hysteresis. Its subthreshold slope appears to be significantly improved, suggesting the onset of the discussed BTBT mechanism. The output characteristic in Supplementary Figure 4e shows a clear NDR region, whose amplitude and position is efficiently modulated by means of the applied bottom gate bias. Indeed, sweeping the gate voltage from negative to positive values determines a right shift of the peak and valley positions. Moreover, as clearly shown in Supplementary Figure 4f, the peak to valley current ratio decreases with the increase of V_G: from a maximum value larger than 10 for V_G = -1 V to 1 for V_G = 1.75 V. In the particular device reported in this work, the NDR persists even under positive gate bias, with the gate modulation effect saturating for V_{TG} > 1 V. The positive gate bias

determines a decrease of the energy overlap between $SnSe_2$ conduction band and WSe_2 valence band, so it should inhibit the onset of BTBT. The residual observed NDR is likely due to Fermi level pinning effects at the heterojunction interface[10,11].

5. Hybrid TFET-MOSFET devices.



Supplementary Figure 5. a. SEM image of a final device with the equivalent electrical circuit. **b.** Measured transfer characteristic of the hybrid TFET-MOSFET device realized connecting in parallel the $WSe_2/SnSe_2$ heterojunction and the built-in WSe_2 MOSFET whose characteristics are presented in Supplementary Figure 4. **c.** Optimized transfer characteristic of the hybrid TFET-MOSFET device, obtained considering the characteristics of the TFET and MOSFET devices discussed in the main text and shifting the heterojunction threshold voltage so to achieve $V_{Th,TFET} > V_{Th,MOSFET}$. In this optimal case, the total current follows the steep turn-on of the TFET and it reaches the high thermionic ON current granted by the MOSFET.

Supplementary Figure 5a shows a colored SEM image of one of our fabricated heterojunction devices together with the schematic of a proposed hybrid TFET-MOSFET device obtained connecting in parallel the $WSe_2/SnSe_2$ heterojunction and its built-in WSe_2 FET presented in Supplementary Figure 4. The measured transfer characteristic of the hybrid is shown in Supplementary Figure 5b together with the current components of each device. In this case, since the TFET threshold voltage is smaller than the MOSFET one, the current of the hybrid FET follows the MOSFET turn-on curve and only for large currents it coincides with the TFET characteristic. It is important to notice the difference in MOSFET and TFET drain to source biases applied in this case so to reduce the mismatch between the threshold voltages of the two devices. Supplementary Figure 5c reports the transfer characteristic expected for an optimized device and obtained starting from the measured $I_D(V_G)$ curves of the $WSe_2/SnSe_2$ TFET

and WSe_2 MOSFET discussed in the main manuscript and shifting the heterojunction transfer characteristic so to obtain $|V_{Th,TFET}| < |V_{Th,MOSFET}|$. In this optimal scenario, the total current follows the steep-turn on curve of the TFET while reaching the high I_{ON} current granted by the thermionic injection mechanism at the base of the MOSFET working principle. Therefore, the proposed hybrid device offers the opportunity of harvesting the advantages of both the devices, while not requiring any additional lithography step.

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