# SUPPLEMENTARY INFORMATION for

## Multilevel Artificial Electronic Synaptic Device of Direct Grown Robust $MoS_2$ Based Memristor Array for In-Memory Deep Neural Network

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**KEYWORDS**: Transition metal dichalcogenides, $MoS_2$, convolution neural networks, synaptic devices, memristor, long/short-term memory

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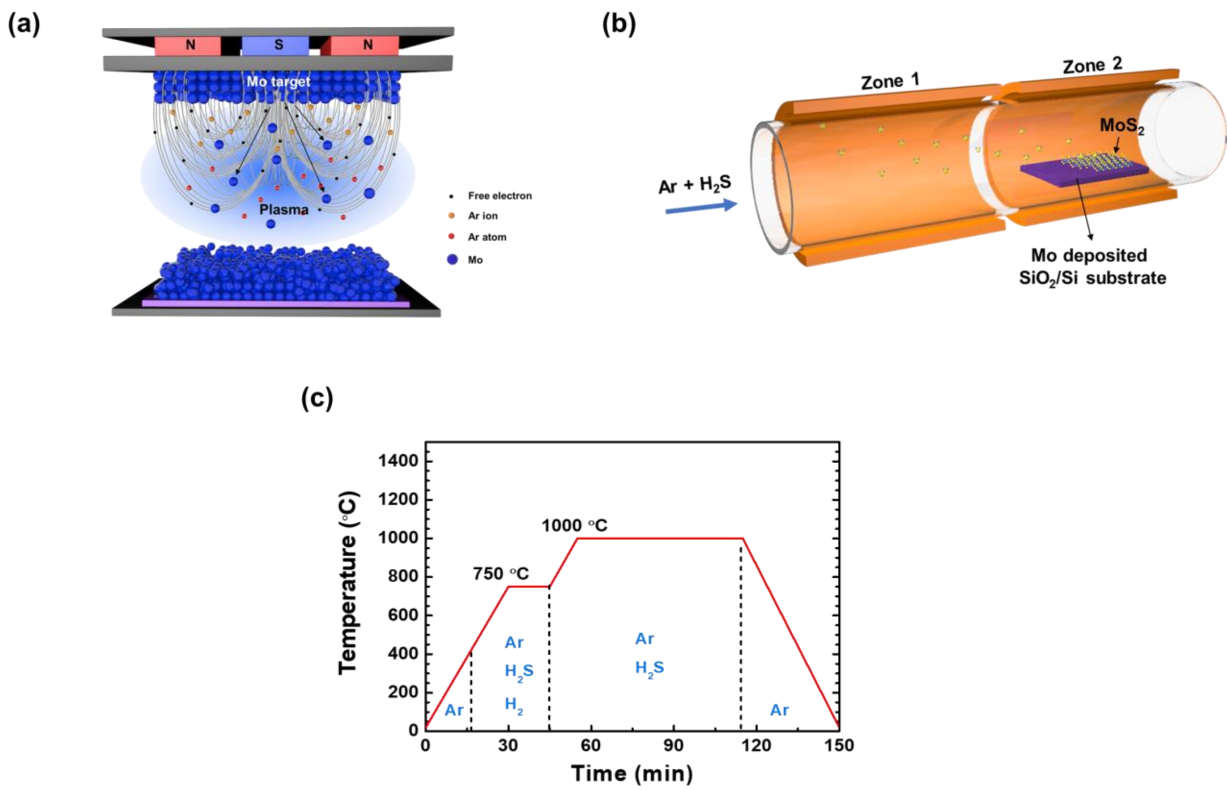
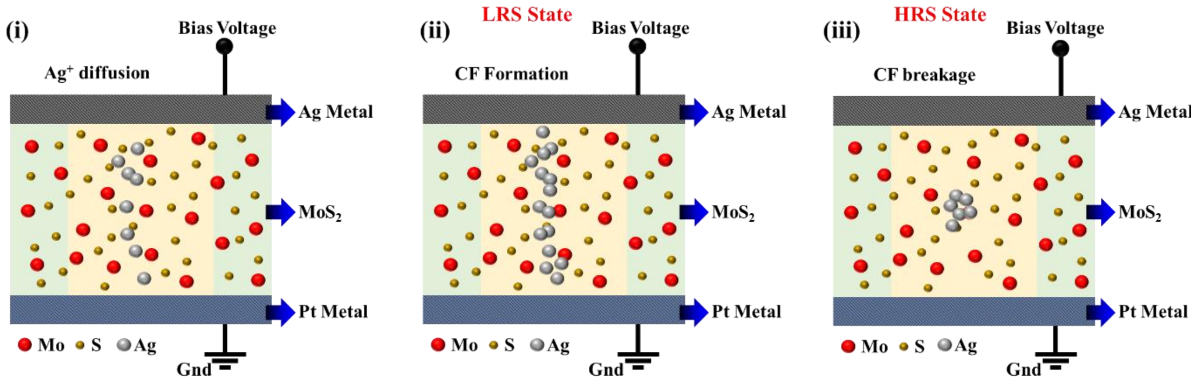


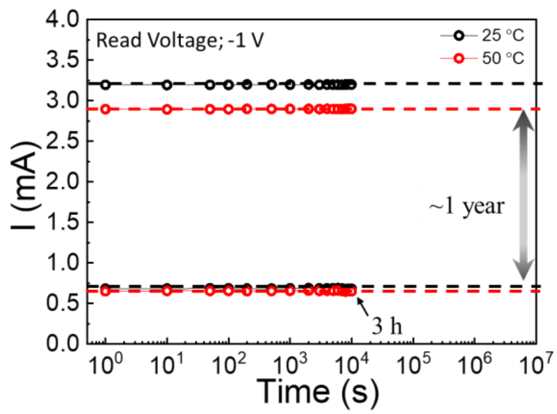

**Supplementary Figure 1**. Schematics of **a** RF magnetron sputtering system for Mo deposition and **b** CVD system for sulfurization. **c** Temperature profile with gas injection conditions for CVD sulfurization as a function of time.

**Supplementary Table 1.** Atomic fraction of $Mo^{4+}$ 3*d* and $Mo^{6+}$ 3*d* and ratio of $Mo^{4+}$ 3*d* to $S^{2-}$ *2p* in the $MoS_2$ film.

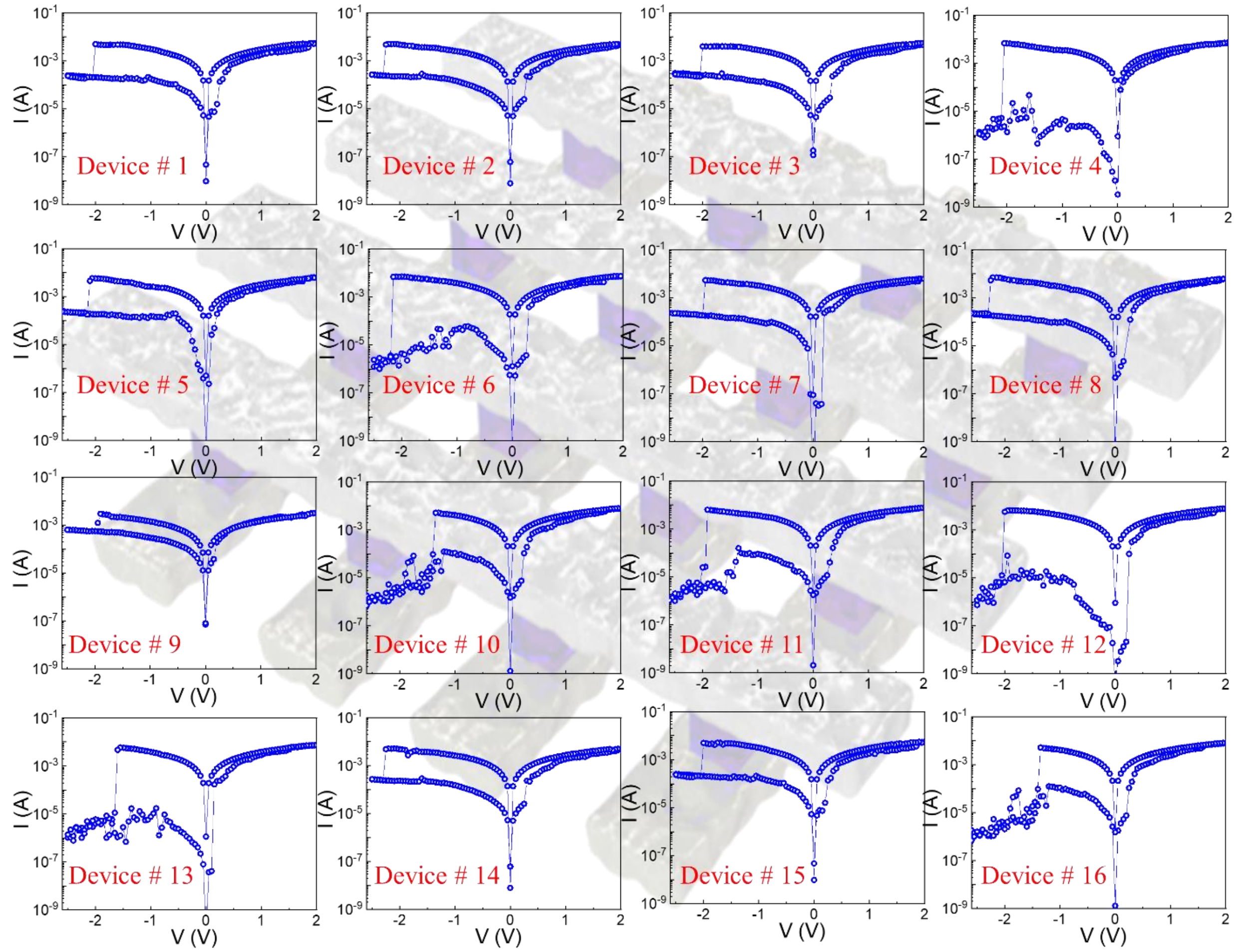
| | **$Mo^{4+}$ 3*d*** | **$Mo^{6+}$ 3*d*** | **Total** | **$Mo^{4+}$ 3*d* : $S^{2-}$ 2*p*** |
|---|---|---|---|---|
| $MoS_2$ film | 83.12 at.% | 16.88 at.% | 100 at.% | 2.19 |



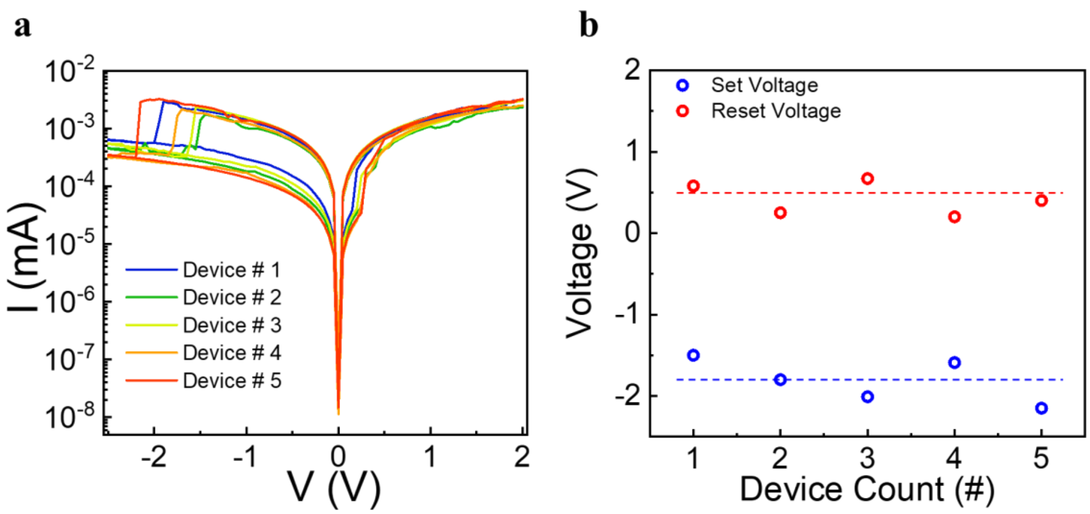

**Supplementary Figure 2**. The mechanism of proposed $MoS_2$ based memristor device, (i) Ag+ diffusion (ii) CF formation, and (iii) CF breakage.



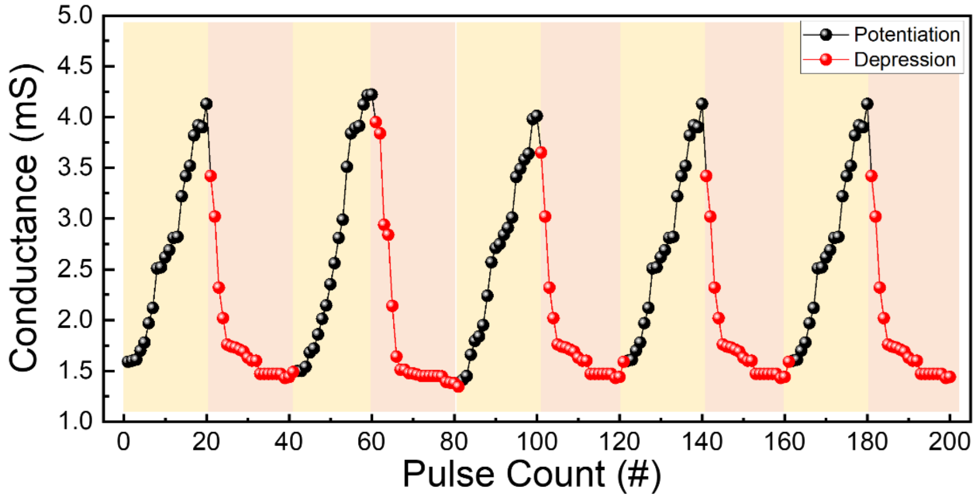

**Supplementary Figure 3**. Retention measurements of the $MoS_2$ memristor up to $10^4$ s at a read voltage of -1 V under temperatures of 25 °C and 50 °C.



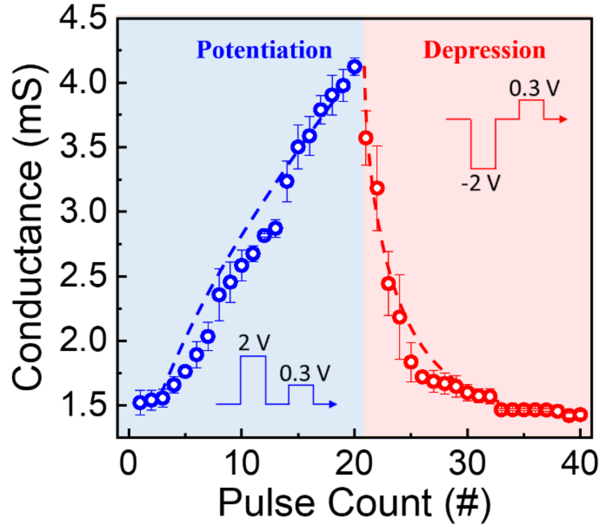

**Supplementary Figure 4.** I-V sweep measurements of the proposed (4 × 4) crossbar memristor array based on $MoS_2$ active material was fabricated on a single substrate.



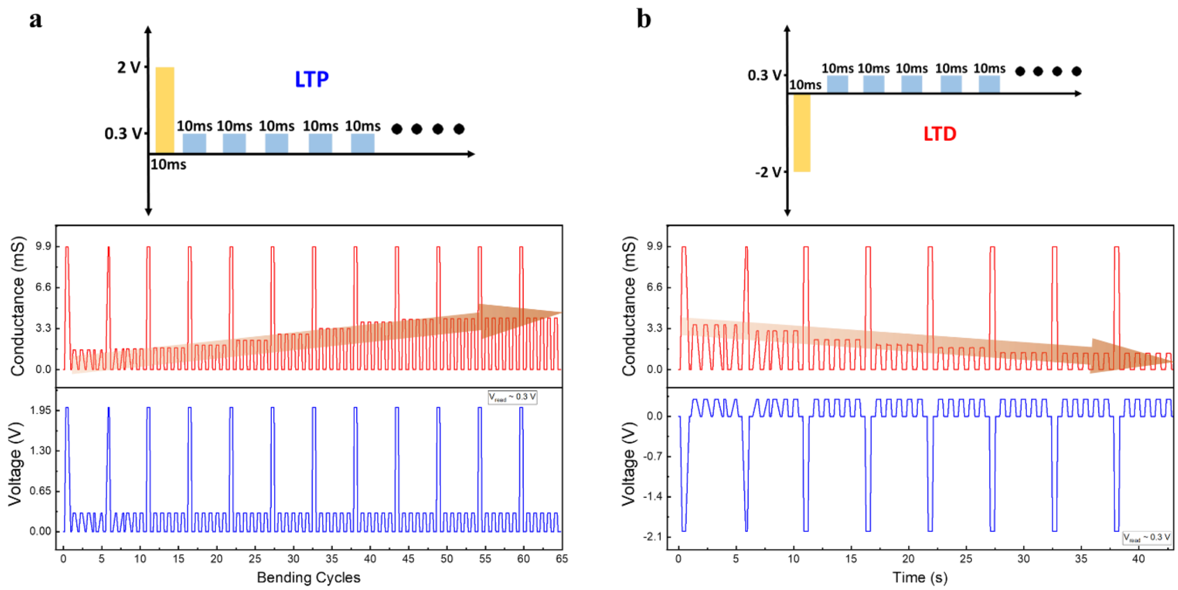

**Supplementary Figure 5**. The memory operation of additional five fabricated $MoS_2$ based memristor devices in terms of (a) I-V sweep and (b) set/reset voltage.



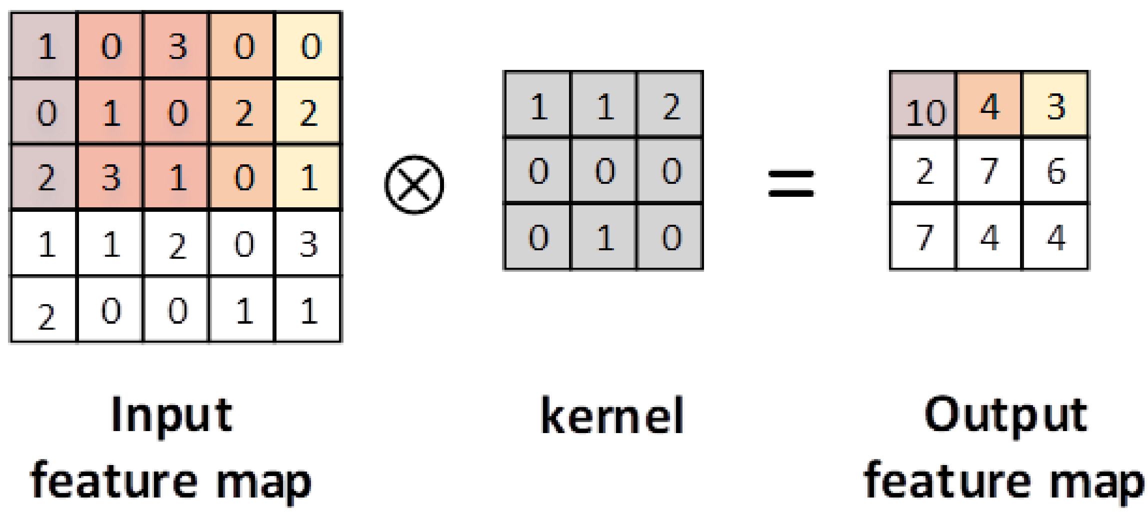

**Supplementary Figure 6**. Weight update curve of electric potentiation and depression measurements with symmetric read voltage of 0.3 V with set/reset voltage of 2 V/-2 V with a width of 10 ms up to 200 pulse counts.




**Supplementary Figure 7**. Electric potentiation and depression measurements of additional five fabricated $MoS_2$ based memristor devices by applying a single consecutive pulse at a read voltage of 0.3 V with a set voltage of 2 V (potentiation) and a reset voltage of −2 V (depression), with a width of 10 ms.




**Supplementary Figure 8**. The DC mode representation of multilevel synaptic dynamics in terms of a) long-term potentiation (LTP) and b) long-term depression (LTD).




**Supplementary Figure 9**. A descriptive representation of convolution operations for training process model.

**Supplementary Table 2.** A comparison table of the proposed $MoS_2$ synaptic memristor with previously reported $MoS_2$ memristor devices in terms of device and neuromorphic application parameters.

| $MoS_2$ based memristor structure | Endurance cycles | Retention time (s) | Deposition method | Bottom electrode/ substrate | Scale | Neuromorphic measurements | Computational method | Recognition accuracy | Year | Ref. |
|---|---|---|---|---|---|---|---|---|---|---|
| **Ag/$MoS_2$/Ag (Stacking structure)** | 1000 | N/A | Exfoliation | Ag | Flake (single device) | N/A | N/A | N/A | 2016 | 1 |
| **Cu/$MoS_2$/Au (Stacking structure)** | 20 | 5 h | MoCVD | Au/ $SiO_2$/Si | Large-area (16 devices) | STDP | N/A | N/A | 2019 | 2 |
| **Graphene/$MoS_2O_x$ Graphene (Stacking structure)** | $10^7$ | $10^5$ | Exfoliation | Graphene/ $SiO_2$/Si | Flake (Single device) | N/A | N/A | N/A | 2018 | 3 |
| **Ag/$MoS_2$/Ag (Stacking structure)** | 100 | ~$10^4$ | Ink ($MoS_2$ flakes) | Ag/ Polyimide | Crossbar | Multilevel storage | N/A | N/A | 2019 | 4 |
| **rGO/$MoS_2$@ZIF-8/rGO (Stacking structure)** | N/A | ~$10^4$ | Spin coating | rGO/PET | Single device | N/A | N/A | N/A | 2014 | 5 |
| **Al/$MoS_2$-$MoO_x$/Al (Stacking structure)** | $10^2$ | $10^4$ | Colloidal synthesis | Al/ $SiO_2$/Si | Large-area (50 devices) | N/A | N/A | N/A | 2016 | 6 |
| **Au/$MoS_2$/Au (lateral-memtransistor with dual-gate structure)** | 250 | ~$10^5$ | CVD | $SiO_2$/Si | Large-area Memtransistor (34 devices) | LTP/LTD (Dual-gate Pulses) | Artificial neural network (ANN) | 94% | 2020 | 7 |
| **Au/$MoS_2$/Au (lateral structure)** | 100 | N/A | CVD | $SiO_2$/Si | Flake (single device) | LTP/LTD | N/A | N/A | 2020 | 8 |
| **Au/$MoS_2$/$Nb_2O_5$/Au (lateral structure)** | 200 | $10^3$ | Sapphire (RF Sputtering + CVD) | $Al_2O_3$/Si | Single device | LTP/LTD (Gate-pulses) | Deep learning neural network | 94.2% | 2021 | 9 |
| **Ag/$MoS_2$(two-step process)/Pt (Stacking structure)** | 500 | $10^4$ | Direct growth (Sputtering + CVD) | Pt/ $SiO_2$/Si | Crossbar (4×4) (16 devices) | LTP/LTD (multilevel potentiation/ depression) | Deep neural network (DNN) | 98.55% | 2021 | This work |

**Supplementary Table 3.** The selected 8 conductance of potentiation & depression process of the proposed artificial neural network.

| Memristor Level | Conductance(mS) |
|---|---|
| **1** | 1.31 |
| **2** | 1.6 |
| **3** | 1.97 |
| **4** | 2.36 |
| **5** | 2.84 |
| **6** | 3.32 |
| **7** | 3.82 |
| **8** | 4.17 |

## Supplementary Section 1

## Nonlinearity (NL) Analysis

$$G_{LTP} = \mathrm{B}\left(1 - e^{\left(-\frac{P}{A}\right)}\right) + G_{min}$$

$$G_{LTD} = -\mathrm{B}\left(1 - e^{\left(-\frac{P-P_{max}}{A}\right)}\right) + G_{max}$$

$$\mathrm{B} = \frac{G_{max} - G_{min}}{1 - e^{-\frac{P_{max}}{A}}}$$

In this equation, GLTP and GLTD are conductance for potentiation and depression, respectively. P refers to number of pulses. By fitting the proposed memristor's potentiation and depression conductance to the equation, a normalized A value, which is inversely proportional to nonlinearity (NL) can be gained. The fitting process is progressed in MATLAB (provided as open-source). With normalized A value, NL values can be identified by the table provided in the reference.[9]

**Supplementary REFERENCES**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