Supplementary information for anomalous conductance quantization of a one-dimensional channel in monolayer WSe_2

Justin Boddison-Chouinard,[1,2] Alex Bogan,[2] Pedro Barrios,[3] Jean Lapointe,[3] Kenji Watanabe,[4] Takashi Taniguchi,[5] Jarosław Pawłowski,[6] Daniel Miravet,[1] Maciej Bieniek,[7,6] Pawel Hawrylak,[1] Adina Luican-Mayer,[1,*] and Louis Gaudreau[2,†]

[1] *Department of Physics, University of Ottawa, Ottawa, Ontario, K1N 9A7*

[2] *Emerging Technologies Division, National Research Council of Canada, Ottawa, Ontario, K1A 0R6*

[3] *Advanced Electronics and Photonics, National Research Council of Canada, Ottawa, Ontario, K1A 0R6*

[4] *Research Center for Functional Materials, National Institute for Materials Science, 1-1 Namiki, Tsukuba 305-0044, Japan*

[5] *International Center for Materials Nanoarchitectonics, National Institute for Materials Science, 1-1 Namiki, Tsukuba 305-0044, Japan*

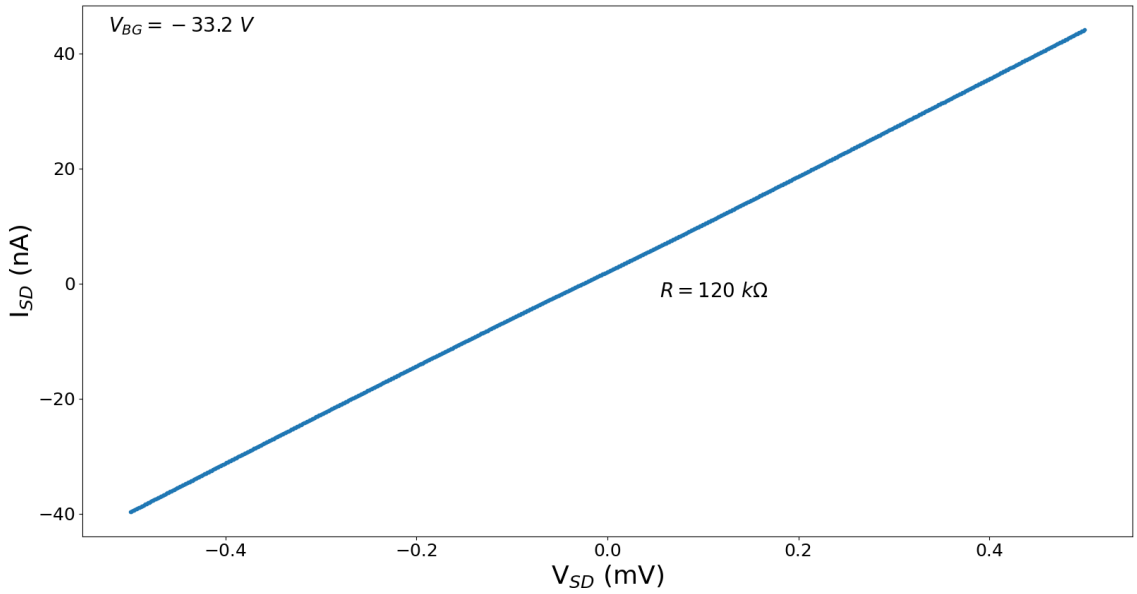
[6] *Institute of Theoretical Physics, Wrocław University of Science and Technology, Wrocław, Poland*

[7] *Institute of Theoretical Physics, Wurzburg University, Wurzburg, Germany*

Supplementary Methods

2-point measurement and contact resistance

We performed 2-point IV measurements in addition to the 4-point measurements presented in the main text to obtain the contact resistance. The 2-point measurement yielded a resistance of 120 kΩ (Supplementary Figure 1) which is a sum of the contact resistance (2 contacts), the RF line (connected to a single contact), and the channel resistance. From the 4-point measurement taken at a back-gate voltage of $V_{BG} = -33\ V$, the channel resistance is 480 Ω (Figure 2a in the main text). The RF line connected to one contact has a resistance of 100 kΩ. Therefore, the average contact resistance per contact is 9760 Ω.

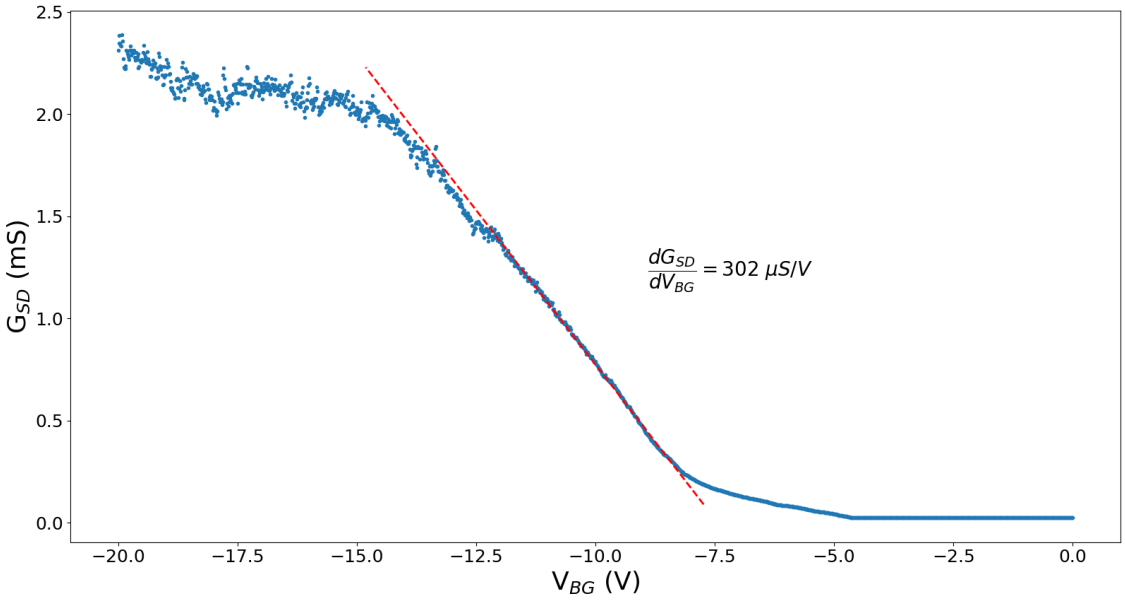


SUPPLEMENTARY FIGURE 1. **Current-voltage I-V characterisation of the device with open split gates**. 2-point measurement of the source-drain current as a function of the bias voltage when $V_{SG} = 0$, indicating a total resistance of 120 kΩ. T = 4 K.

* luican-mayer@uottawa.ca
† louis.gaudreau@nrc-cnrc.gc.ca

$$R_C = \frac{1}{2}(R_{2-\text{point}} - R_{4-\text{point}} - R_{\text{RF}}) = 9760\ \Omega \tag{1}$$

Mobility and carrier density calculation



SUPPLEMENTARY FIGURE 2. **Device activation curve taken with open split gates.** 4-point measurement of the source-drain conductance as a function of back-gate voltage taken at 4K and $V_{SG} = 0$.

In a 4-point measurement scheme, we monitor the resistance as a function of back-gate voltage with the split gate voltage set to zero. The conductance (inverse of resistance) increases linearly as of $V_{BG} = -8$ V. From this linear segment, we extract a slope of -302 μS/V and a x-intercept of $V_{th} = -7.44$ V, which corresponds to the threshold voltage. Using these values, we can estimate the field-effect mobility of our device and obtain the carrier concentrations for different values of V_{BG}. For calculating the mobility, we use:

$$\mu = \frac{dG_{\text{SD}}}{dV_{\text{BG}}} \frac{L}{w} \frac{1}{C_{\text{G}}} \tag{2}$$

where the ratio L/w is taken to be 0.3 (calculated from the geometry of the sample), and $\frac{dG_{\text{SD}}}{dV_{\text{BG}}} = -302$ μS/V (Supplementary Figure 2). The gate capacitance per unit area, C_{G}, is obtained by considering that the dielectric between the WSe_2 and the back-gate comprises of 285 nm of SiO_2 ($\epsilon_{SiO_2} = 3.9$) and 26 nm of hBN ($\epsilon_{\text{hBN}} = 2.5-4$)[1–3] (thicknesses confirmed by AFM). Therefore,

$$C_{\text{G}} = \epsilon_0 \left(\frac{\epsilon_{SiO_2}\epsilon_{\text{hBN}}}{\epsilon_{\text{hBN}} t_{SiO_2} + \epsilon_{SiO_2} t_{\text{hBN}}} \right) = (1.06 - 1.11) \times 10^{-4}\ \text{Fm}^{-2}. \tag{3}$$

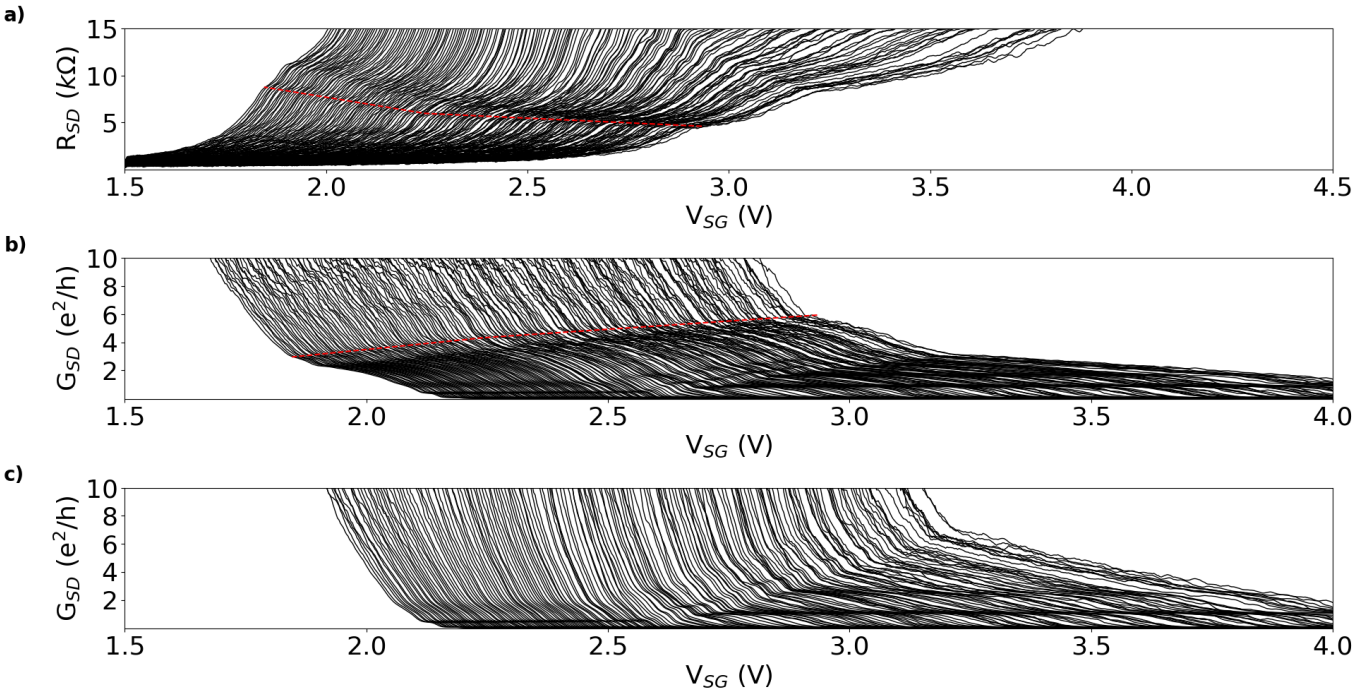
With these values, we obtain a mobility of approximately $\mu_{\text{FE}} \approx 8000 - 8500$ cm^{2}V^{-1}s^{-1} which is better than other high mobility values reported in WSe_2[4–7]. Additional values were extracted from similar curves taken at room temperature and at 1 K where we obtained $\mu_{\text{FE}}(\text{T} = 300\ \text{K}) \approx 300$ cm^{2}V^{-1}s^{-1} and $\mu_{\text{FE}}(\text{T} = 1\ \text{K}) \approx 16800 - 17600$ cm^{2}V^{-1}s^{-1}. This trend from low mobility to high mobility as temperature decreases further suggests that a clean and high mobility device has been fabricated.

The carrier concentration at any given back-gate voltage can be estimated by

$$n(\mathrm{V_{BG}}) = C_{\mathrm{G}} \frac{\mathrm{V_{BG}} - \mathrm{V_{Th}}}{e} \tag{4}$$

For example, at $\mathrm{V_{BG}} = -33$ V (Figure 2 a-b in main text), the hole concentration is approximately $n = 1.82 \times 10^{12}$ cm^{-2}.

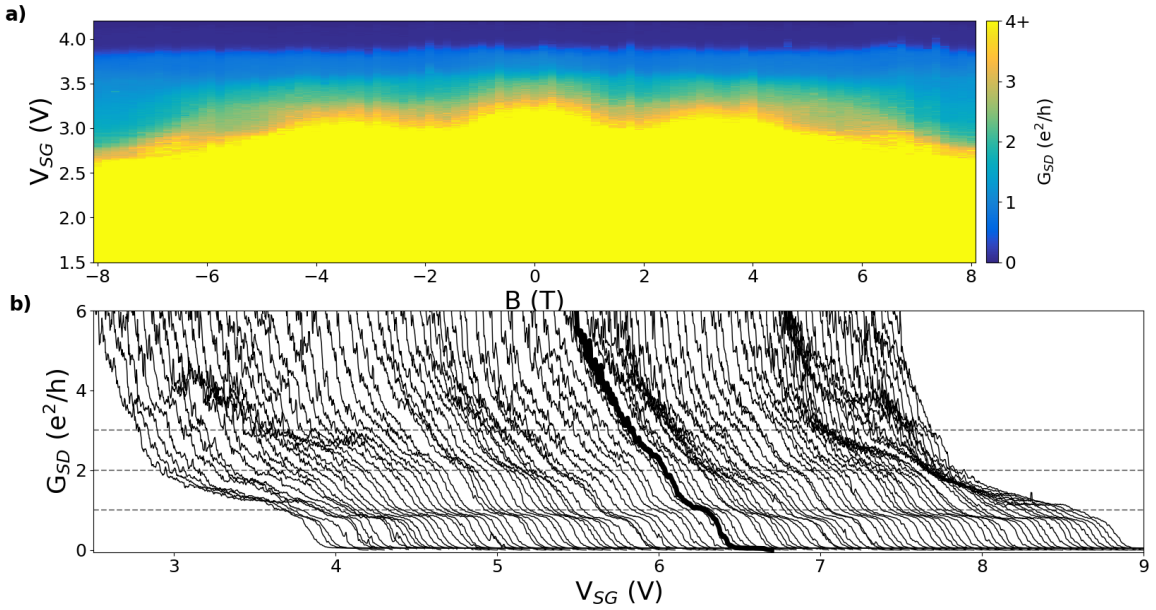
Series resistance calculation



SUPPLEMENTARY FIGURE 3. **Extraction of the series resistance.** (a) Resistance as a function of split gate voltage $\mathrm{V_{SG}}$ where each trace is taken at a different back-gate voltage $\mathrm{V_{BG}}$ ranging from -25 V (left) to -35 V (right). (b) Corresponding conductance curves plotted in units of e^2/h. The red lines in plots (a-b) correspond to the depletion of the split gates and consequently the series resistance. (c) The same traces as in (b) after subtracting the series resistance.

In Supplementary Figure 3(a), we plot the raw data (resistance vs. split gate voltage) for various values of the back-gate voltage. The leftmost curve corresponds to a back-gate voltage of -25 V and the rightmost curve corresponds to a back-gate voltage of -35 V. The spacing between each curve is 50 mV. In Supplementary Figure 3(b), the conductance ($\frac{1}{R_{\mathrm{SD}}}$) is plotted as a function of the split gate voltage for the same curves as in Supplementary Figure 3(a). In both Supplementary Figure 3(a-b), a red dotted line is plotted indicating the value of the series resistance that was subtracted to obtain Supplementary Figure 3(c) (Figure 2 c-d in the main manuscript). This series resistance represents the resistance at the point where the areas beneath the split gates are depleted and was obtained in a similar fashion to Marinov *et al.*[8]. As we can see, the series resistance decreases as a function of back-gate voltage because the WSe_2 sheets on either side of the split gates have more carriers and therefore less resistance. After removing the series resistance (Supplementary Figure 3(b)), we obtain the same plot as found in the main text (Figure 2d).

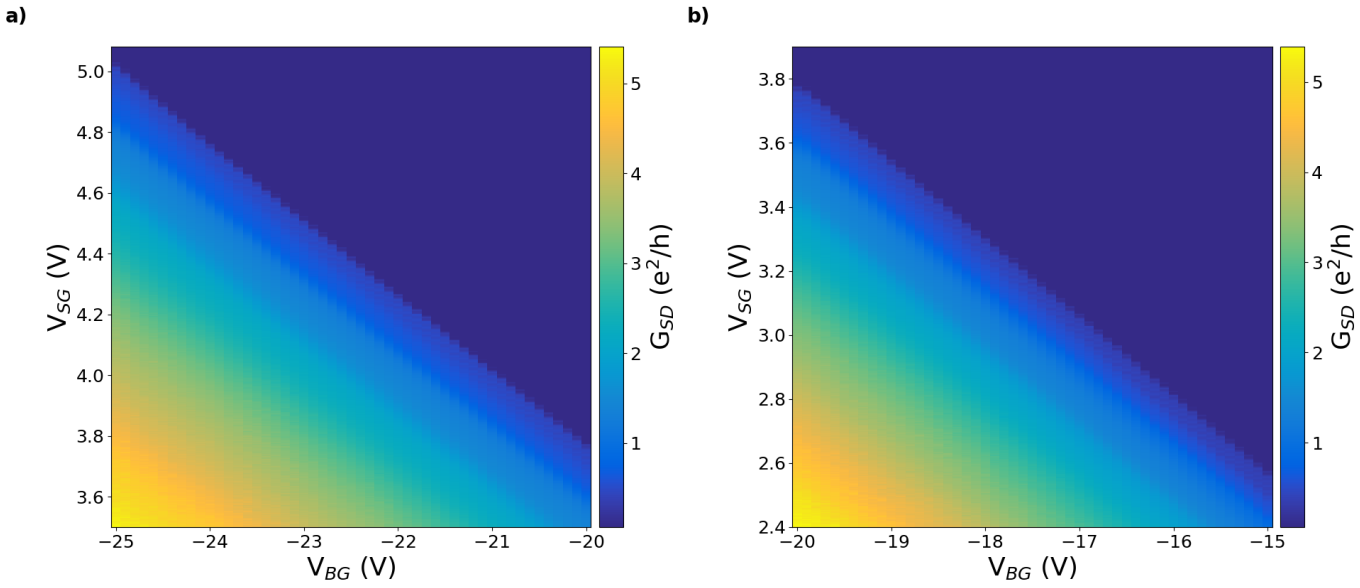
Reproducibility at 10 mK



SUPPLEMENTARY FIGURE 4. **Out-of-plane magnetic field $B_\perp$ dependence of the 1D channel at T = 10 mK.** (a) Dependence of the quantized conductance plateaus on a perpendicular magnetic field ranging from -8 T to 8 T. (b) Line cuts from (a) plotted in a "waterfall" style. A horizontal offset is introduced between adjacent line traces for clarity. A lead resistance of $R_L = 5083\ \Omega$ was subtracted. $V_{BG} = -33.2$ V.

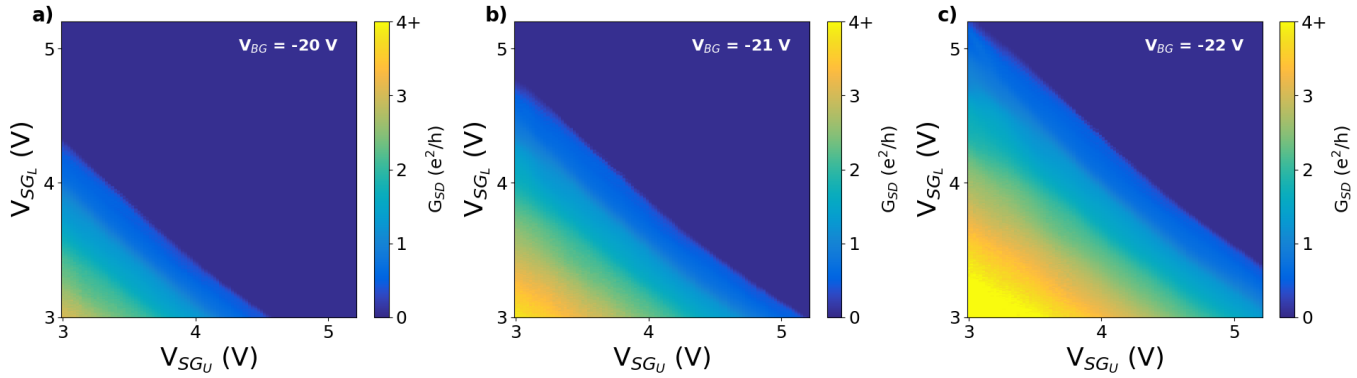
The same set of measurements found in Figure 3 in the main manuscript was also performed at the base temperature of the dilution refrigerator (10 mK) (Supplementary Figure 4). A first plateau appears at e^2/h for all values of the magnetic field. Another plateau appears around 2 e^2/h at $B = 0$ T and quickly converges to 2 e^2/h as we turn on the magnetic field. This value away from 2 e^2/h at $B = 0$ T is attributed to magnetoresistance effects in the leads. At approximately ± 5 T, the 2 e^2/h plateau evolves towards the e^2/h plateau as seen at 4 K.

Repeatability in a different measurement setup



SUPPLEMENTARY FIGURE 5. **Transport across the 1D channel as a function of the hole concentration.** Color map of conductance as a function of split gate voltage V_{SG} and back-gate voltage V_{BG}.

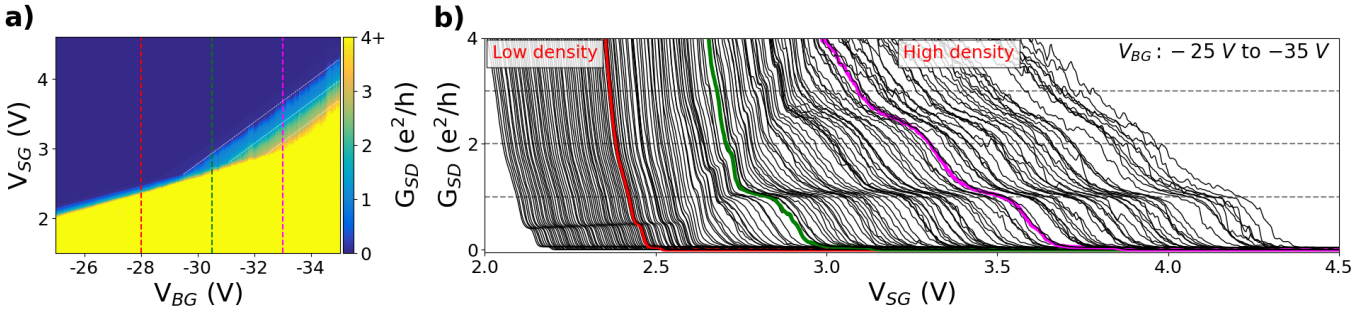
The device considered in the main manuscript was also studied in a 1K cryostat at 4 K. Similar results are observed where there are 3 robust plateaus each spaced by e^2/h for various carrier densities as seen in Supplementary Figure 5.



SUPPLEMENTARY FIGURE 6. **Conductance as a function of individual split gates V_{SG_L} and V_{SG_U}.** Measurements taken at (a) $V_{BG} = -20$ V, (b) $V_{BG} = -21$ V, and (c) $V_{BG} = -22$ V

To ensure that the conductance plateaus are related to the gate-defined channel and not some resonances under the split gates, we measured the conductance as a function of each individual split gate (Supplementary Figure 6). V_{SG_L}/V_{SG_U} refer to the lower/upper split gates in the inset of Figure 1b in the main text. These plots were taken at 3 different carrier concentrations (back-gate voltages) and we observed robust plateaus that are equally influenced by both gates (a slope of approximately 45°) indicating that the origin of the plateaus is located in between the two gates, hence the channel.

Transport in the low carrier density regime



SUPPLEMENTARY FIGURE 7. **Transport in a low hole concentration regime.** (a) Color map of conductance as a function of split gate voltage V_{SG} and back-gate voltage V_{BG} as found in Figure 2c of the main manuscript. A lead resistance is subtracted. (b) Line cuts from (a) plotted in a "waterfall" style indicating a first step at e^2/h and a second step around 2 e^2/h in the high density regime. An additional robust plateau is found at 0.5 e^2/h in the low density regime. The left most trace is taken at $V_{BG} = -25$ V and the right most trace is taken at $V_{BG} = -35$ V. The red, green and magenta lines are highlighted by similarly colored dashed lines in (a) and correspond to back-gate voltages of −28 V, −30.5 V, and −33 V respectively. These three curves feature the regimes where we observe the 0.5 e^2/h plateau (red), the 1 e^2/h plateau (green), and the 1 e^2/h and 2 e^2/h plateaus (magenta)

Transport through the 1D channel was studied at various back-gate voltages (-25 V to -35 V) which led to the observation of two distinct regimes as demonstrated in Supplementary Figure 7a. At higher hole concentrations ($V_{BG} < -30$ V) we observed conductance plateaus at 1 e^2/h and 2 e^2/h as discussed in the main manuscript. Furthermore, Supplementary Figure 7b reveals that there is a robust plateau located at 0.5 e^2/h found at lower carrier densities corresponding to a back-gate raised above -30 V. This plateau is unexpected and demonstrates that further research needs to be conducted on monolayer TMDs to fully understand their electronic properties.

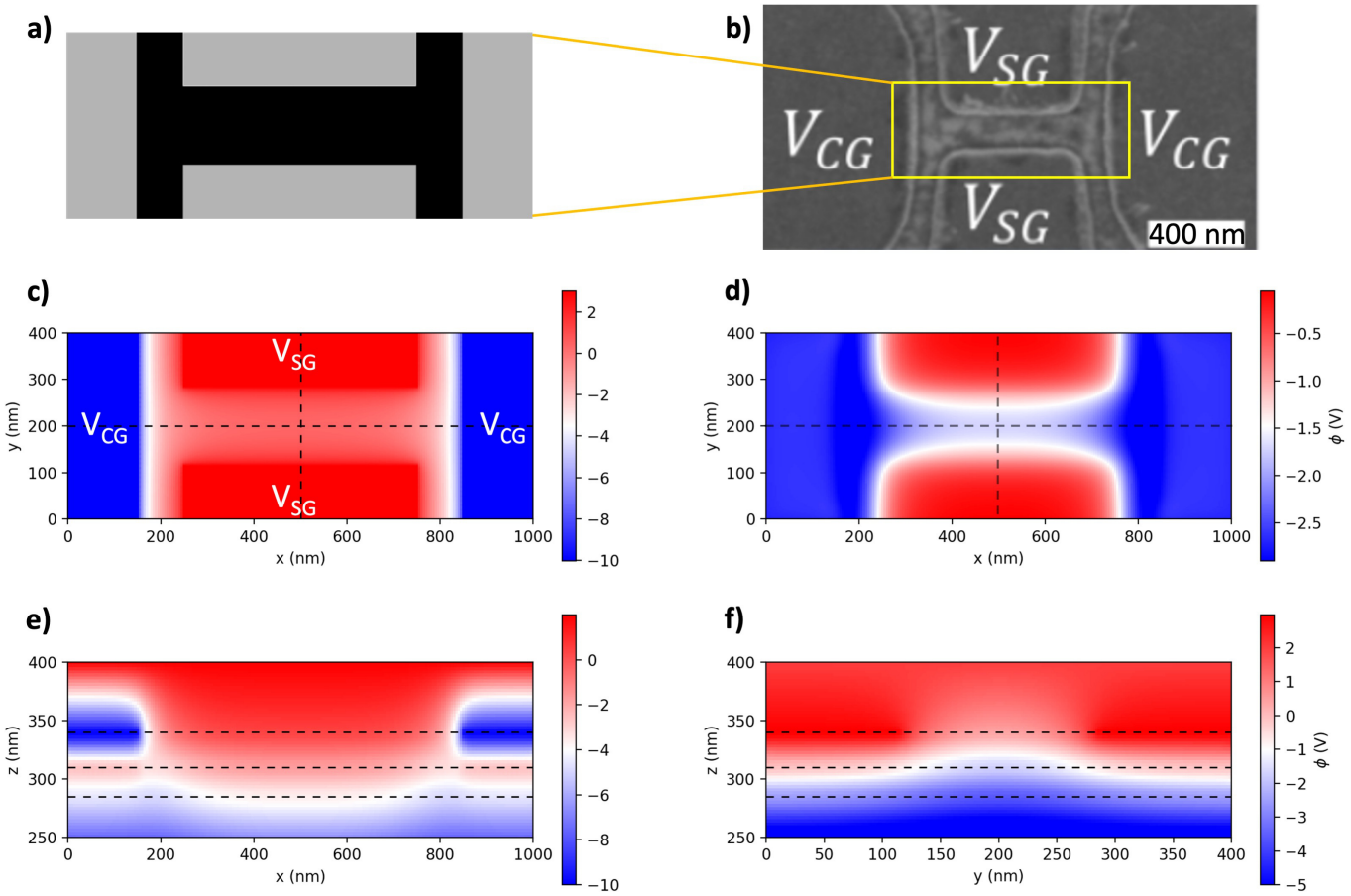
Self-consistent Poisson-Schrödinger calculations

To get the realistic channel potential landscape we performed Poisson-Schödinger calculations [9] with exact finite element modeling of the device electrostatics combined in a self-consistent manner with the Schrödinger tight-binding equation for the WSe_2 monolayer. The Poisson-Schödinger method was previously used to model devices based on gated monolayers [10, 11]. The Poisson equation includes the charge of holes confined in the channel with the space distribution obtained from the Schrödinger equation, and a hole gas accumulated under the contact gates. On the other hand, when solving the Schrödinger equation we take the confinement potential at the monolayer level extracted from the Poisson solution. Therefore both equations have to be solved self-consistently. For more details see e.g. [9].

The 3D electrostatic potential $\phi(\mathbf{r})$ was calculated by solving the Poisson equation in a computational box that covers central area of the device next to the gap between the split gates – see Supplementary Figures 8a-b. The device model includes the space-dependent permittivity of the various materials stacked in the heterostructure structure. The following dielectric constants were adopted [3]: $\varepsilon_{WSe_2} = 7.5$, $\varepsilon_{hBN} = 3.3$, and $\varepsilon_{SiO_2} = 3.9$. A realistic top gate layout, presented in Supplementary Figure 8a, and a p-doped substrate that serves as a back gate were assumed. All the voltages, geometric dimensions, and material parameters were strictly related to the experiment. The top gates (at $z = 340$ nm level), the WSe_2 monolayer ($z = 310$ nm) stacked between the two hBN layers, and top edge of the SiO_2 layer ($z = 285$ nm) are marked in Supplementary Figures 8e-f by black dashed lines (levels). During the calculations we applied the following voltages to the top gates: $V_{SG} = 3$ V, $V_{CG} = -10$ V, while on the back gate we applied $V_{BG} = -33$ V. The voltage conditions enforced on the gates are clearly visible in the potential map at the gates level, presented in Supplementary Figure 8c. The potential landscape at the WSe_2 monolayer level, with a clearly visible channel formed between the split gates, is presented in Supplementary Figure 8d. To have a complete picture of the potential, lateral cross-cuts along the x-axis and y-axis are shown in Supplementary Figure 8e and Supplementary Figure 8f.

Tight-binding parameters

In the tight-binding atomistic calculations we chose the following structural parameters: $d_{\|} = 1.9188$ Å (W-Se_2 dimer center distance), $d_{\perp} = 1.6792$ Å (Se atom distance from $z = 0$ plane). The tight-binding Slater-Koster parameters are given by (all in eV): $E_d = -0.4330$, $E_{p0} = -3.8219$, $E_{p\pm1} = -2.3760$, $V_{dp\sigma} = -1.58193$, $V_{dp\pi} = 1.17505$, $V_{dd\sigma} = -0.90501$, $V_{dd\pi} = 1.0823$, $V_{dd\delta} = -0.1056$, $V_{pp\sigma} = 0.52091$, $V_{pp\pi} = -0.16775$, together with characterising intrinsic spin-orbit couplings: $\lambda_W = 0.275$, $\lambda_{Se_2} = 0.08$. We note that these parameters are chosen to reproduce ab initio electronic band structure of two spin-full valence bands.



SUPPLEMENTARY FIGURE 8. **The realistic channel potential landscape.** (a) Gate layout adopted in the Poisson-Schrödinger model based on real arrangement of the top gates in the device presented in panel (b). Top view of the potential profile at the (c) top gates level, and (d) WSe_2 level. The channel is formed in the area between the split gates. The lateral view of the potential along the (e) x-axis and (f) the y-axis is also presented. Note that the p-doped substrate with the applied $V_{BG} = -33$ V is located at $z = 0$ and omitted in the plots for brevity.

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