

Ionotronic WS₂ Memtransistors for 6-bit Storage and Neuromorphic Adaptation at High Temperature

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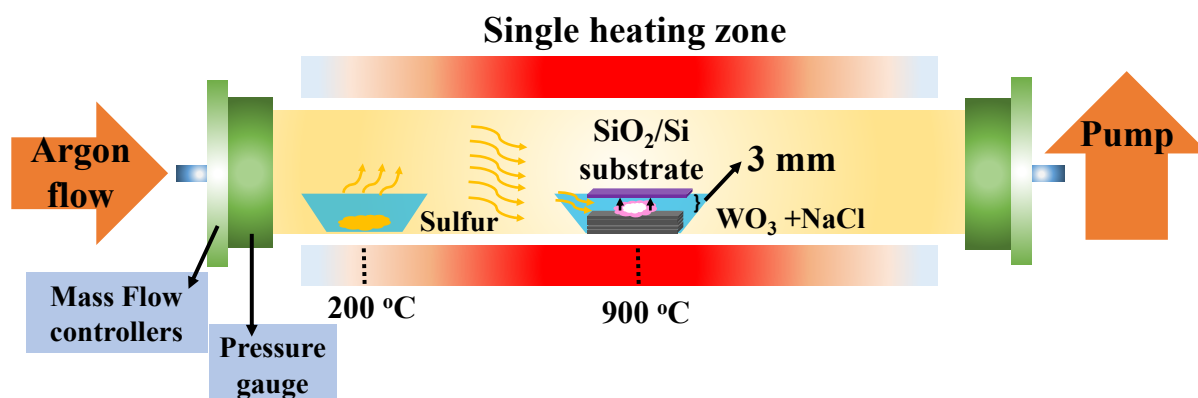
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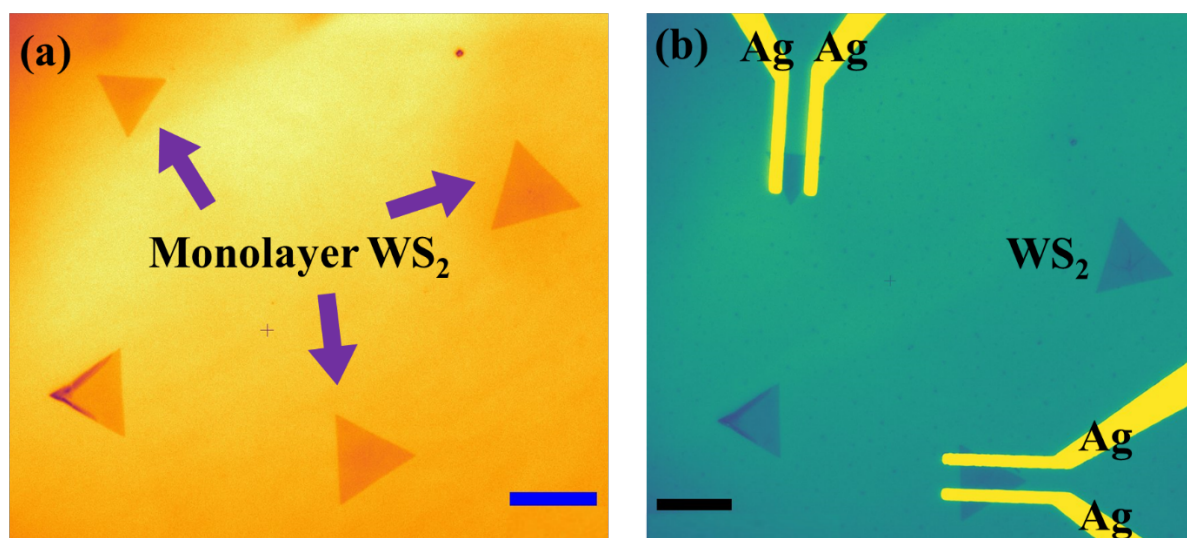
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Supplementary Note 1 : Salt-assisted CVD synthesis of monolayer WS₂



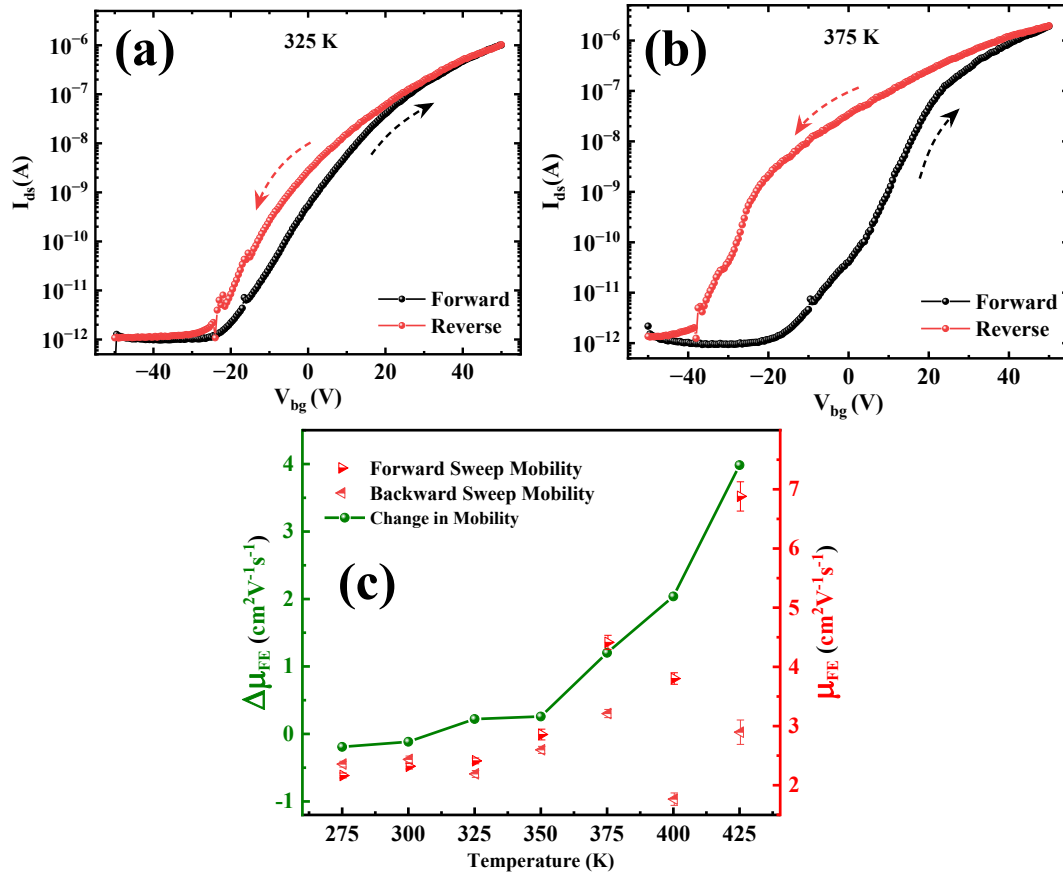
Supplementary Figure 1: The schematic representation of self-assembled CVD setup with a single heating zone working tube, illustrating the main components and their arrangement: The arrow in left side of the figure indicates the direction of the carrier gas (in our case, Ar) towards the chamber through a mass flow controller. An pressure gauge is attached to the tube for measuring the real-time vacuum pressure inside the system during growth. The single zone programmable heat controller regulates the temperature at the central part only. The arrow in ride side indicates the outlet directions for the flow of residuals, which also helps to maintain the pressure.

Supplementary Note 2 : Optical micrographs of monolayer samples and devices



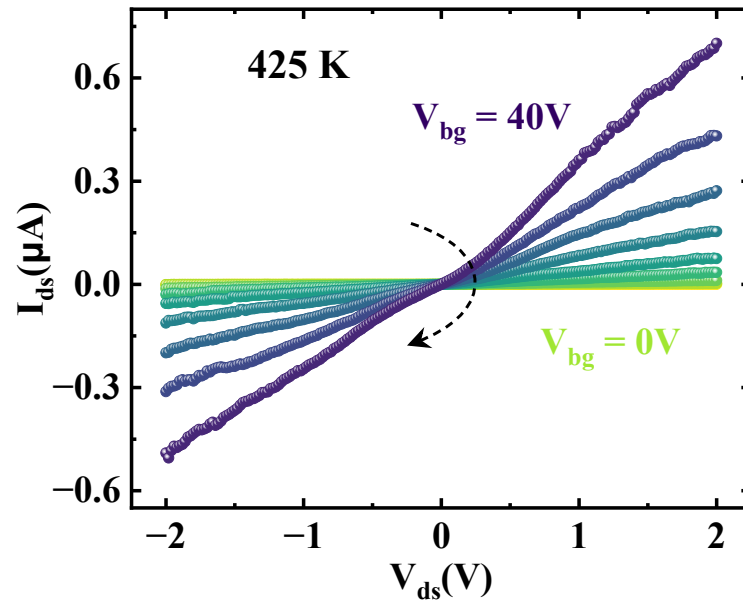
Supplementary Figure 2: Optical image (a) of triangular domain CVD growth of monolayer WS₂ (b) after device fabrication process where Ag is used as drain-source electrodes (Scale bar is 20 μm).

Supplementary Note 3 : Temperature dependent Reverse Hysteresis



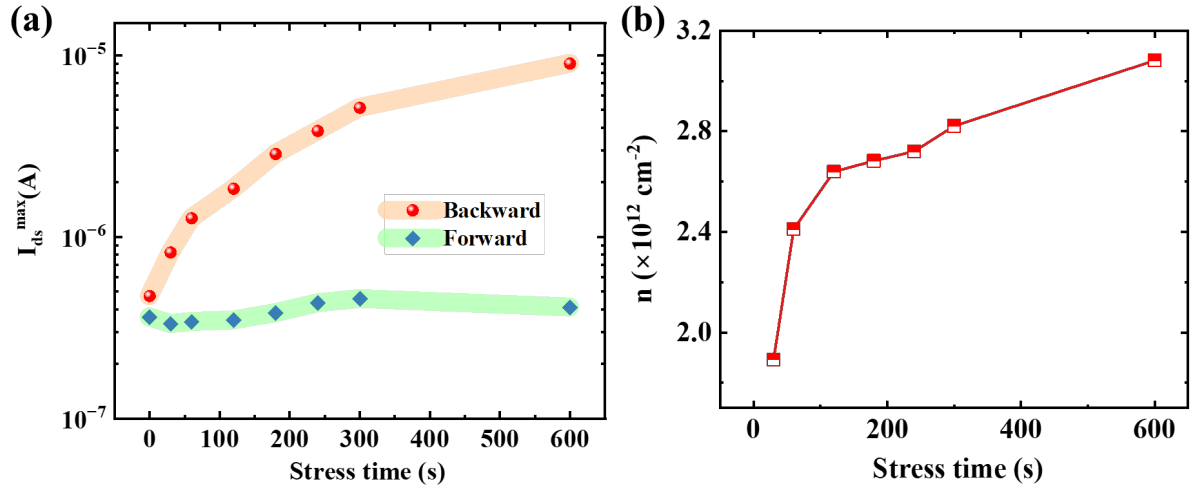
Supplementary Figure 3: Temperature dependent Hysteresis evolution: The dual sweep transfer characteristics at temperature (a) 325 K and (b) 375 K for gate voltage sweep range of ± 50 V. The black and red arrows represent forward and backward sweep direction illustrating the anti-clockwise hysteresis behaviour (c) The extracted forward and backward mobilities with respect to temperature. The error bars represent the standard error of the mean.

Supplementary Note 4 : High temperature output characteristics



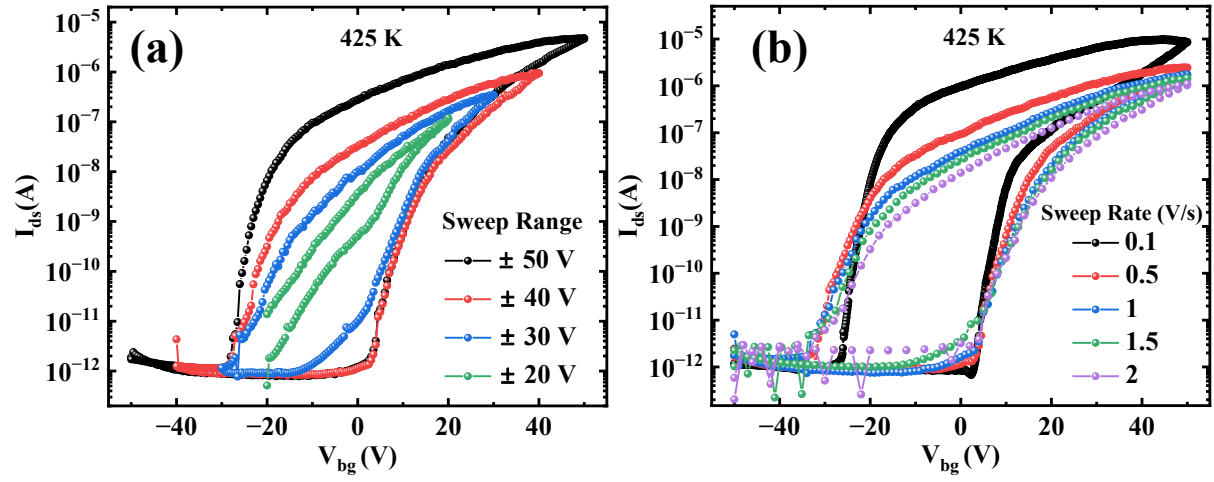
Supplementary Figure 4: The output characteristics ($I_{ds} \sim V_{ds}$) taken at a high temperature, 425 K for various gate voltages ranging from 40V to 0V.

Supplementary Note 5 : Stress induced current variations during dual sweep



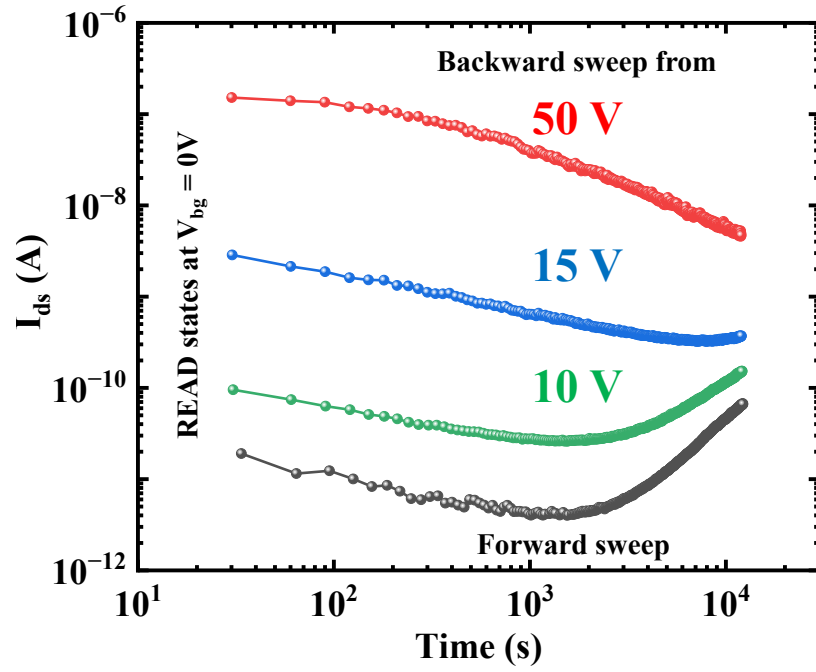
Supplementary Figure 5: (a) Represents the variation of maximum drain current stressed at $\pm 50 \text{ V}$ during dual sweep extracted from Fig. 2 (e) and (f). Blue and red points indicates the maximum current during forward and backward sweep. An increase in the backward sweep current with respect to prolonged stress time under positive gate bias stress at 50 V , whereas the variations of forward currents remain flatter. (b) Represents the variation of electrostatic doping densities with stress time at temperature 425 K .

Supplementary Note 6 : Sweep rate and sweep range dependent hysteresis plot



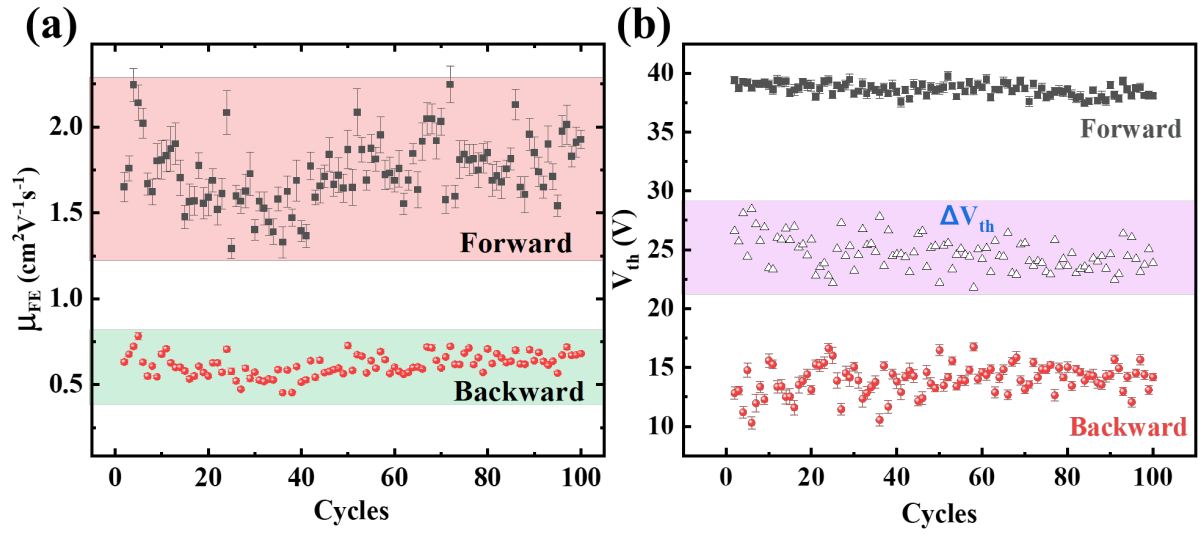
Supplementary Figure 6: Sweeping Variations: Dual sweep transfer characteristics of various gate voltage sweep conditions i.e. (a) different ranges from ± 20 V to ± 50 V at constant sweep rate of 0.5 V/s (b) different sweep rate from 0.1 V/s to 2 V/s at a fixed range between ± 50 V.

Supplementary Note 7 : Retention of sweep range induced PROGRAM states



Supplementary Figure 7 : Retention measurements of Fig. 4 (f) at $V_{bg} = 0 V$. The black curve represents the retention curve taken during forward sweep and other three colours represents the retention curves measured during backward sweep from various amplitudes 10 V (Green), 15 V (Blue), 50 V (Red).

Supplementary Note 8: Endurance in Mobility and Threshold Voltage shifts



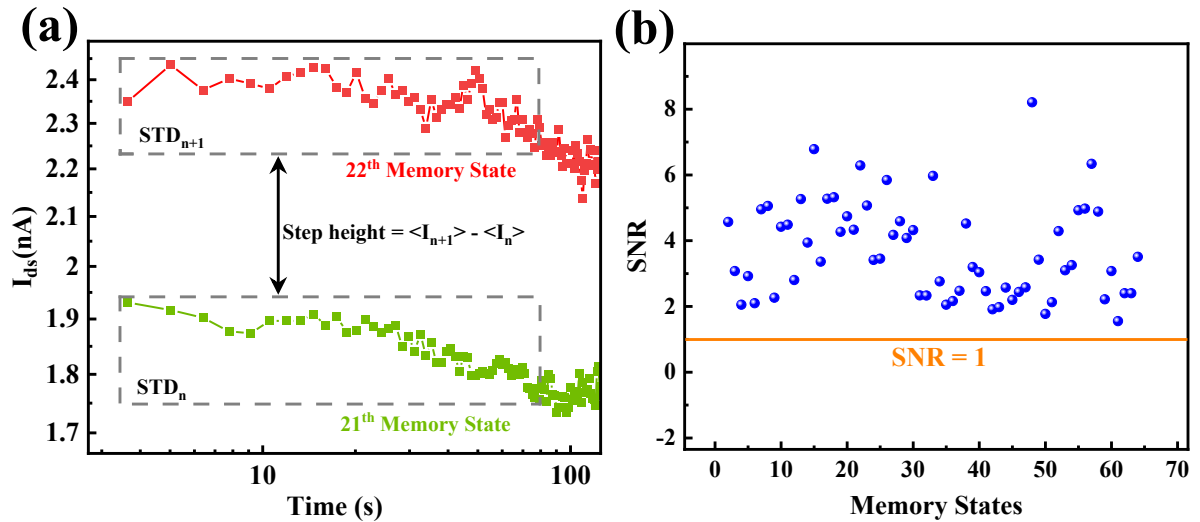
Supplementary Figure 8: (a) Mobility during the forward sweep (the error bars represent the standard error of the mean) and backward sweep of 100 repeated cycles forming a range indicated by the red and green band, respectively, (b) Threshold voltage (V_{th}) of the transfer characteristic during forward and backward sweep is indicated by black square and red circle respectively. The white triangles in the pink band represent the difference between both V_{th} , also referred to as the memory window.

Supplementary Note 9 : Signal to Noise Ratio (SNR) Calculation

By utilizing a particular technique, the signal-to-noise ratio can be determined. This technique involves the computation of the mean currents and standard deviations of two consecutive storage levels during retention measurements. Fig. S8 (a) provides an illustration where the storage currents of states 21th and 22th are 1.8 nA and 2.3 nA, respectively, with STDs of 39 pA and 41 pA, respectively. In order for these two states to be distinguishable, the disparity between the two current signals, 28th and 29th, should be greater than the sum of their STDs. As a result, the signal-to-noise ratio is defined as follows:

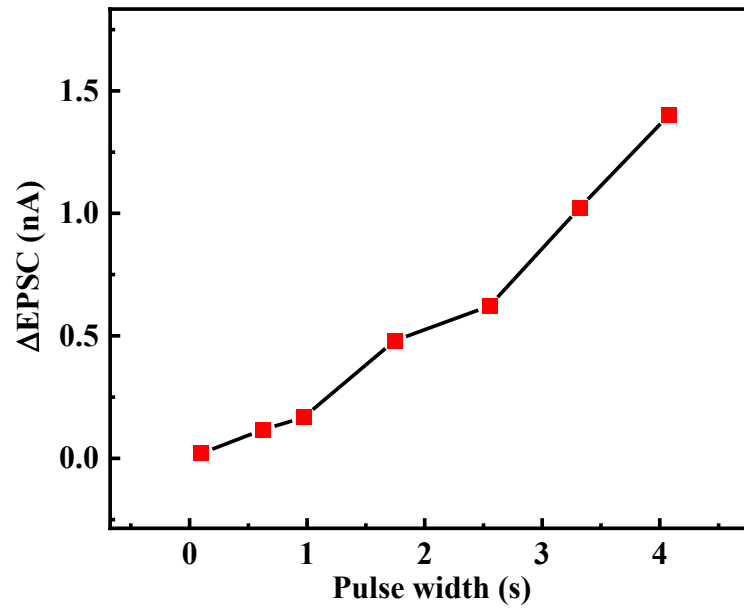
$$\text{SNR} = \frac{I_{n+1} - I_n}{\text{STD}_{n+1} + \text{STD}_n} \quad (1)$$

When the values of currents and standard deviations for states 28th and 29th are inserted into the aforementioned equation, where n ranges from 1 to 65, the resultant ratio is calculated to be 5.07, indicating that these two states are distinguishable from each other as these ratio is greater than 1. A similar approach is employed to assess the remaining states' reliability, and the outcomes are illustrated in Fig. S8 (b). All the computed ratios surpass the critical limit of $\text{SNR} = 1$, confirming the credibility of all the storage states.



Supplementary Figure 9: (a) Storage currents states of 28th and 29th STD stands, and (b) Signal-to-noise ratio for all the storage states.

Supplementary Note 10: Linear response of synaptic plasticity



Supplementary Figure 10: The linear response of change in PSC with respect to pulse width.