

Supplementary information for
Active Dual-Gated Graphene Transistors for Low-Noise, Drift-Stable, and Tunable
Chemical Sensing

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S1. Fabrication of the local dual-gated graphene device

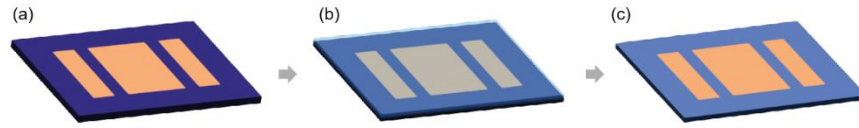


Figure S1. Fabrication process flow for the dual-gated substrate. (a) A tri-metal gate stack (5nm Ti / 20nm Au / 10nm Pt) is deposited via electron-beam evaporation to form the source drain contacts as well as the back gate metal. (b) 35 nm of HfO₂ is deposited by atomic layer deposition to form the gate dielectric. (c) Source/drain openings are etched using reactive ion etching to create the final structure showing the completed local back gate architecture.

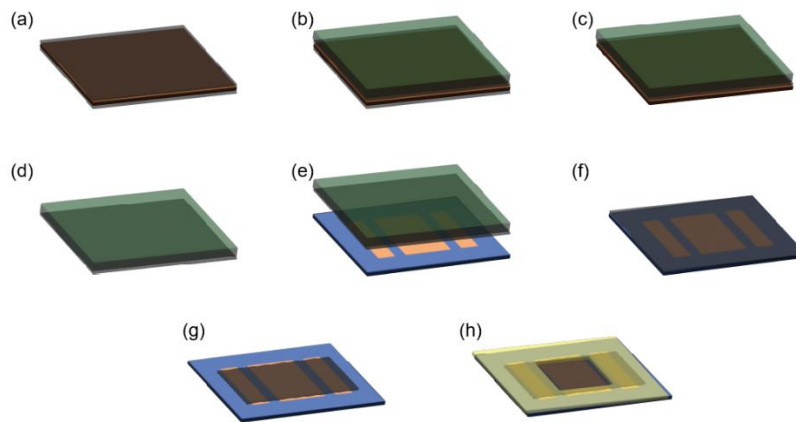


Figure S2. Key steps in the graphene transfer and device patterning process. (a) CVD Graphene on copper (b) PMMA-spin coating (c) Backside graphene etch (d) Copper etching (e) transfer to the target substrate (f) PMMA removal (g) Photolithographic patterning and plasma etching to define the graphene channel (h) SU-8 encapsulation to passivate the device and expose the sensing window for electrolyte gating

S2. PCB and Software information

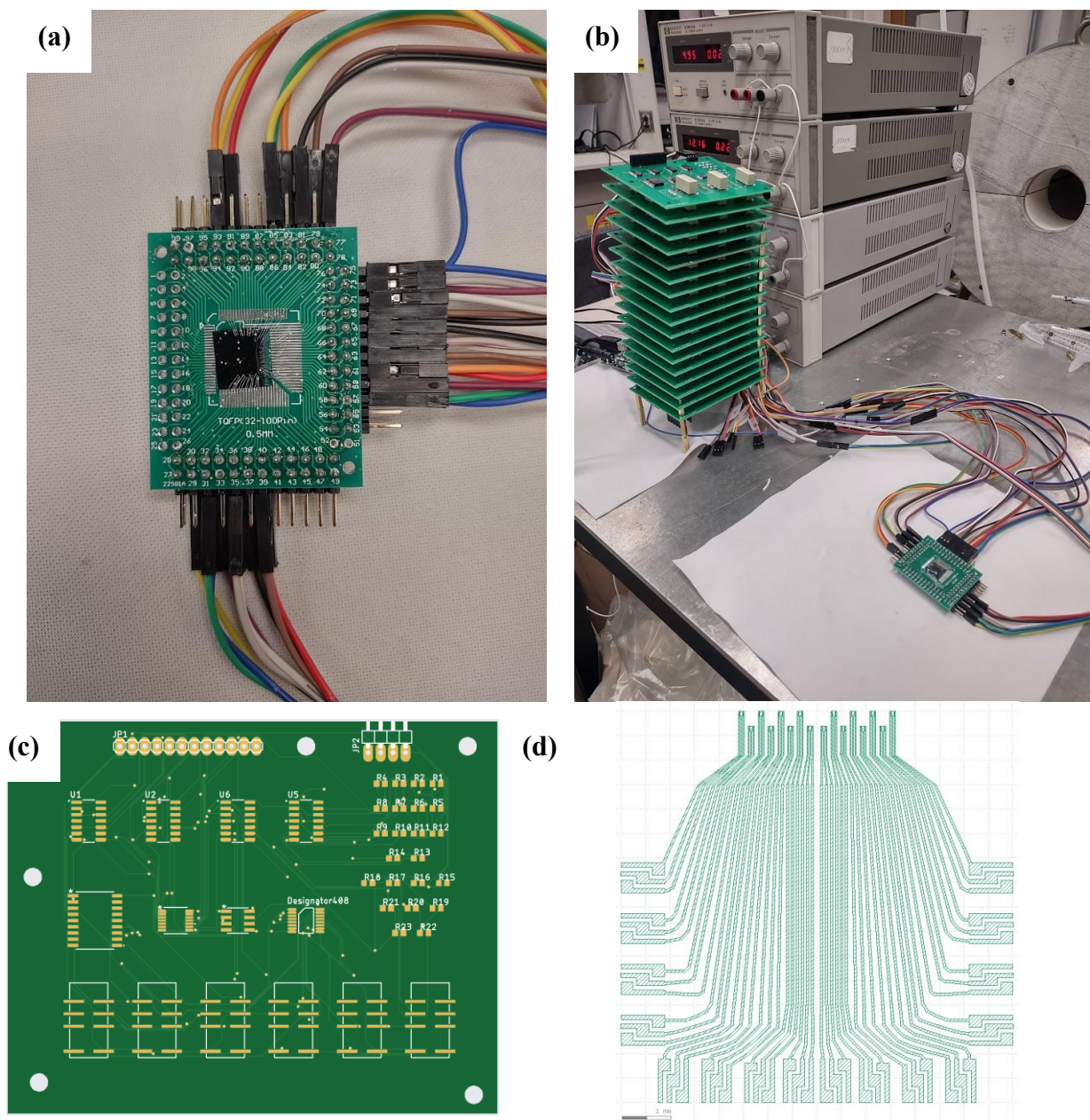


Figure S3. Multichannel measurement setup for graphene sensor arrays. (a) Close-up image of a wire-bonded graphene device under test on the PCB platform. (b) Photograph of the stacked PCB system capable of simultaneously measuring up to 16 devices. (c) Schematic of the custom PCB design, illustrating the layout for individual device connections, signal routing, and integration with the measurement system. (d) Lithographic mask design of the 16-sensor array chip showing metal contacts to the sensors and contact pads.

S3. Top Gate Sweep (TGS) data for different electrolyte media

Electrochemical impedance spectroscopy (EIS) was performed to characterize the double-layer capacitance and solution resistance of various electrolytes at the sensing interface. A three-electrode configuration was used, with a platinum counter electrode, Ag/AgCl reference electrode, and a gold working electrode. Measurements were carried out in the frequency range of 1 Hz to 1 MHz using a 50 mV AC perturbation at open circuit potential. The impedance spectra were fitted with a Randles equivalent circuit.

Theoretically, the back gate capacitance is calculated to be:

$$C_{bg} = \frac{\epsilon_0 \epsilon_r A}{d} \approx 38 \text{ pF}$$

, where $\epsilon_r = 25$ for hafnia, $d \cong 35 \text{ nm}$, $A = 6000 \text{ } \mu\text{m}^2$

And the corresponding geometric top gate capacitance from the C_{dl} measurements with PBS are:

$$C_{tg} = C_{dl} \times A \approx 1388 \text{ pF}$$

, where the top gate is exposed around $A \cong 3000 \text{ } \mu\text{m}^2$

Table S1. Media capacitance measurement using electrochemical impedance spectroscopy

	$R_{sol} (\text{k}\Omega)$	$C_{dl} @ 1\text{Hz}$ (F/cm ²)
DIW	16.77	0.54p
10mM KCl	0.23	36.36u
PBS	0.22	46.28u
ACET	105.90	0.35p
ACET 10mM PHAS	1.22	16.25u
IL	4.83	8.51u

S4. Top Gate Sweep (TGS) data for all the devices tested

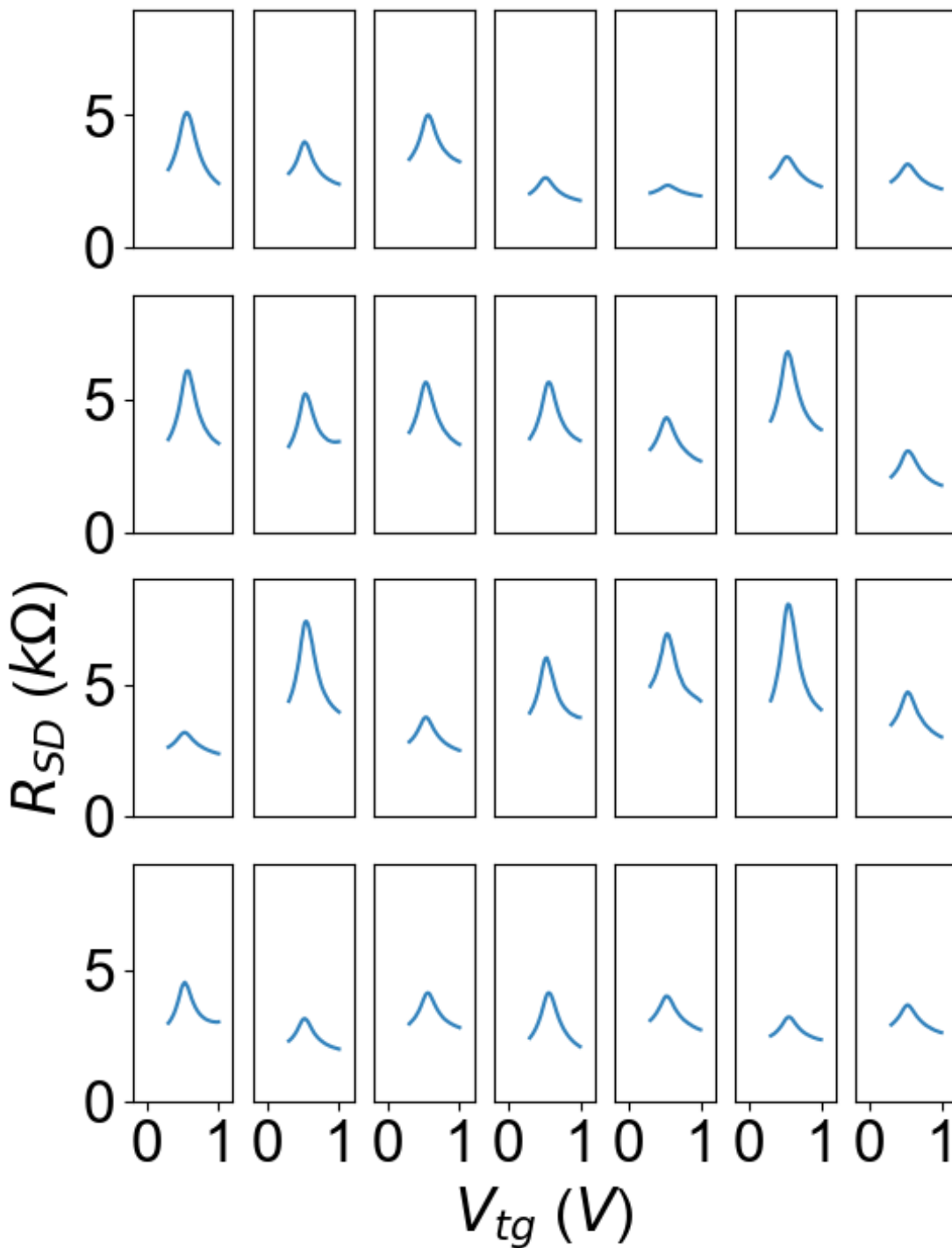


Figure S4. Top Gate Sweep (TGS) data for all the devices tested in PBS electrolyte. Raw data is available in the accompanying dataset for reference.

S5. Back Gate Sweep (BGS) data for all the devices tested

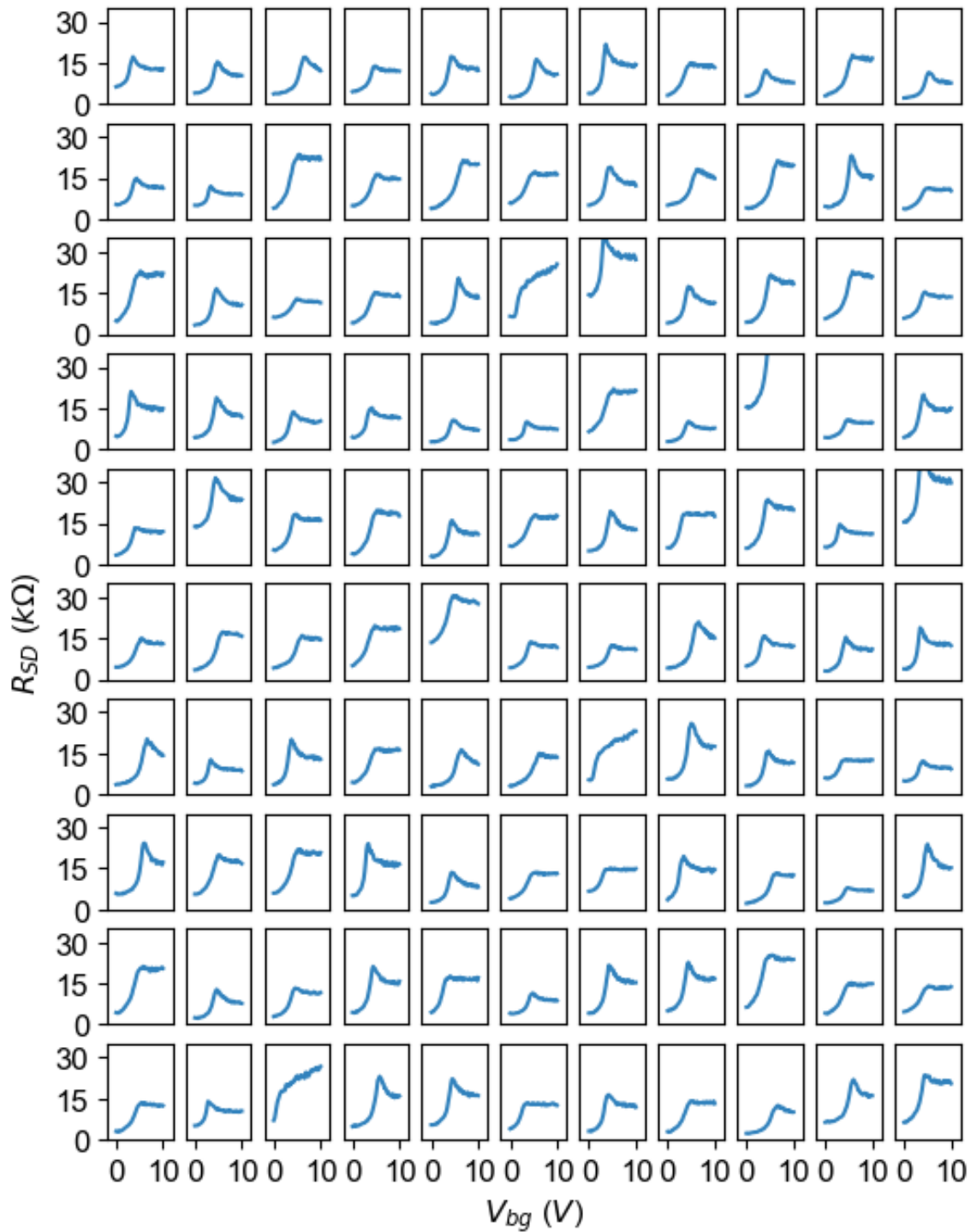


Figure S5. Back Gate Sweep (BGS) data for all the devices tested. Raw data is available in the accompanying dataset for reference.

S6. Comparison of Back Gate Sweep (BGS) characteristics in ambient air versus electrolyte

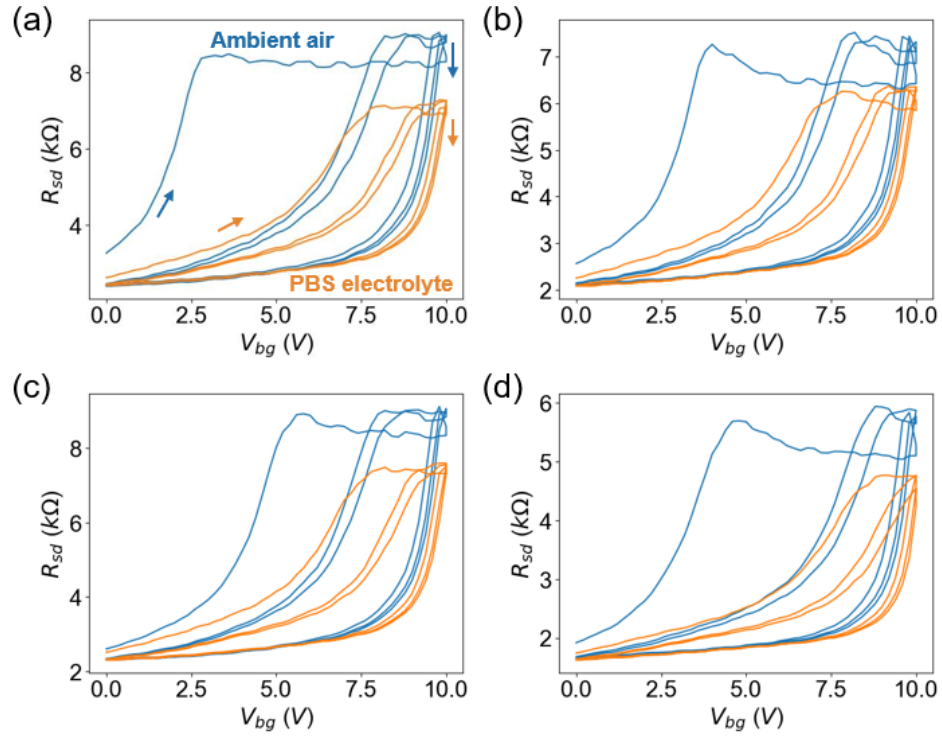


Figure S6. Back-gate transfer characteristics in dry vs. liquid environments. R_{sd} vs. V_{bg} curves for four representative devices measured in ambient air and subsequently in $1\times$ PBS electrolyte with the top gate floating. The addition of the electrolyte induces significant p-doping, evidenced by the positive shift of the Dirac point. Multiple consecutive sweeps (direction by arrows) reveal hysteresis and charge trapping effects.

S7. Addition Mode (AM) data for different electrolyte media

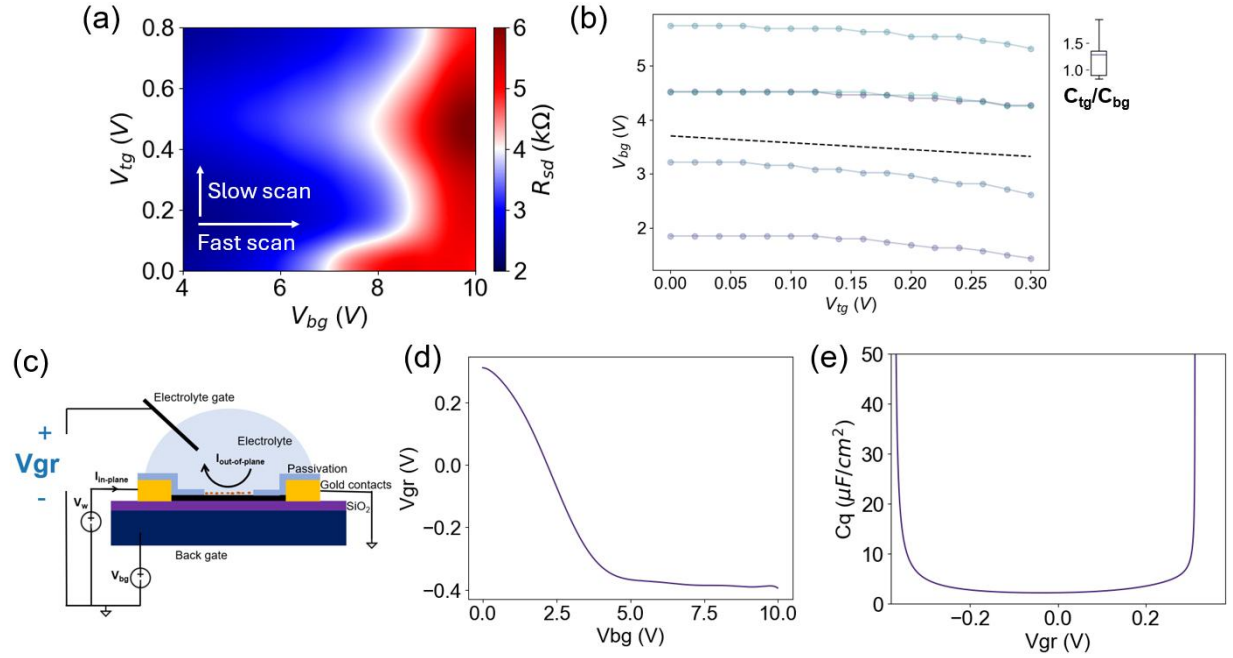


Figure S7. Dual-gated GFET: hysteresis and band-filling analysis. (a) Evolution of the Dirac peak in Addition Mode under repeated dual-gate sweeps. Early sweeps show a sharp charge-neutrality peak that broadens and shifts with subsequent measurements because of hysteresis, charge trapping, and ionic drift. (b) Amplified back gate response DMS mode (V_{BG}) to the top gate sweep (V_{TG}) in DIW, with an observed slope $\sim 1.2\times$. (c) Schematic and definition of V_{gr} . During a back-gate sweep with a Pt top gate in electrolyte, V_{gr} is the graphene potential measured versus a reference electrode in the electrolyte. (d) Measured V_{gr} as a function of V_{bg} , reflecting the band-filling (Fermi-level) shift of graphene. (e) Quantum capacitance Cq of graphene computed at different V_{gr} values using the slope from panel (c) via $Cq = -Cox \times (dV_{bg}/dV_{gr} + 1)$, showing a range of Cq from about 2 microfarads per square centimeter to greater than 50 microfarads per square centimeter.

S8. Differential Feedback Mode data

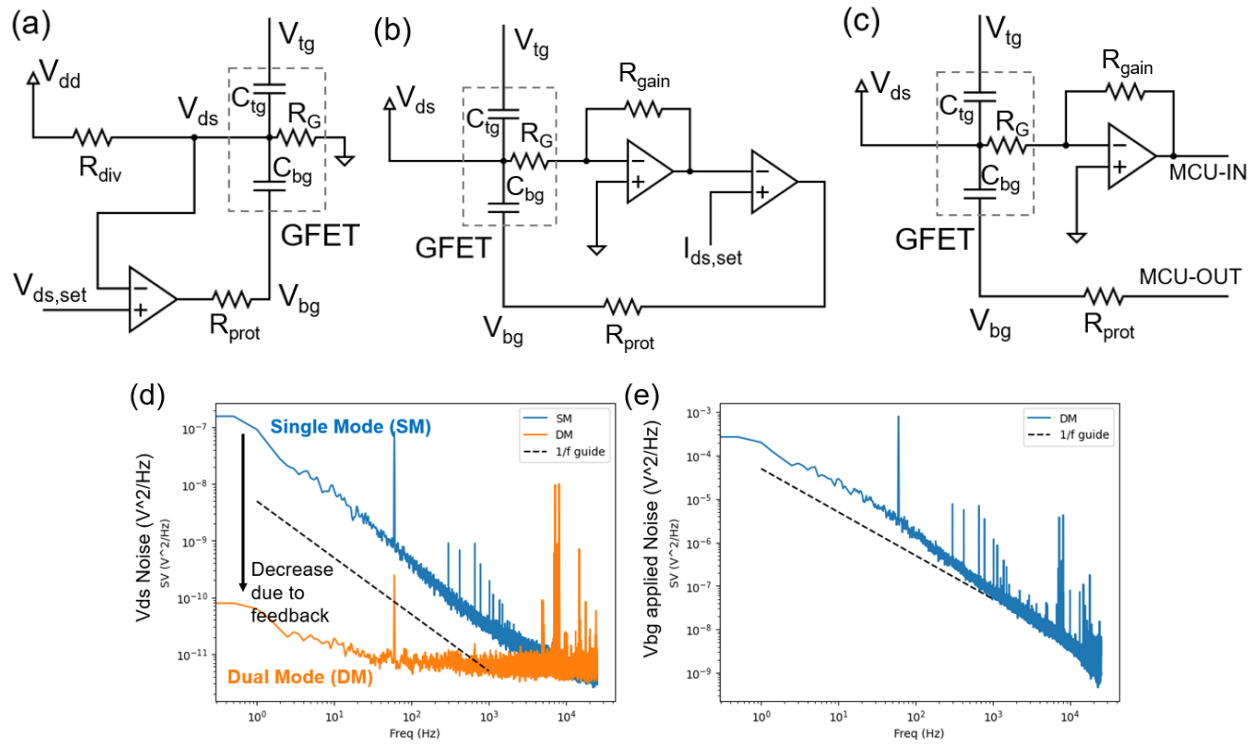


Figure S8. To evaluate the stability of different biasing strategies for dual-gated graphene field-effect transistors (GFETs), we simulated three representative circuit architectures (a-c) using an off-the-shelf operational amplifier model (TL074). The GFET was modeled as a gate-voltage-dependent channel resistance, denoted as R_G , varying from one kilohm at V_{bg} equal to zero volts to five kilohms at V_{bg} equal to five volts, with parasitic top-gate and back-gate capacitances, denoted as C_{tg} and C_{bg} , respectively. R_{gain} and R_{prot} denote the trans-impedance gain and back-gate protection resistor respectively. (a) In this configuration, V_{dd} is applied through a passive resistor network to the GFET channel, with V_{ds} monitored at the divider midpoint. This approach is intrinsically stable due to its purely resistive bias path. However, due to high V_{ds} , gating is asymmetric across the channel introducing a differential gating effect, where both V_{bg} and V_{ds} influence the GFET's electrostatic state. This can shift the apparent transfer curve and complicate interpretation of sensing signals. (b) In this scheme, an operational amplifier maintains a constant I_{ds} setpoint, denoted as $I_{ds,set}$, by adjusting V_{bg} through feedback. While theoretically attractive for low V_{ds} and automated bias control, the closed-loop dynamics involve multiple capacitances (C_{tg} and C_{bg}) interacting with the op-amp's finite bandwidth. For realistic op-amp models such as TL074, the loop can approach instability in certain R_G -capacitance combinations. Compensation networks could improve stability but would add complexity to design and reduce bandwidth. Furthermore, with varying molecule/electrolyte, the response would change. For these reasons, this architecture was not adopted in the present work. (c) In this architecture, V_{ds} is fixed at a low value (for example, ten millivolts), while I_{ds} is measured via a shunt resistor and digitized at MCU-IN. Because V_{ds} remains nearly constant regardless of R_G , the differential gating effect is greatly

suppressed, and the electrostatic control is dominated by V_{bg} . Due to digital control this method is stable over the full R_G range, with minimal phase lag introduced by C_{tg} and C_{bg} . It is therefore both effective in isolating back-gate control and straightforward to implement. (d) Reduction of current $1/f$ noise in the Differential Mode Fixed (DMF) system, specifically (a)-circuit. Spectral density of source-drain current noise measured under different gating modes, highlighting the suppression of low-frequency $1/f$ noise in the dual-mode configuration. (e) The corresponding noise transformed into equivalent back-gate voltage noise, demonstrating reduced gate voltage fluctuations in DMF. This reduction in both current and equivalent gate noise underscores the effectiveness of dual-mode feedback in stabilizing the device response and improving sensing resolution.

S9. Limit of Detection (LOD) analysis

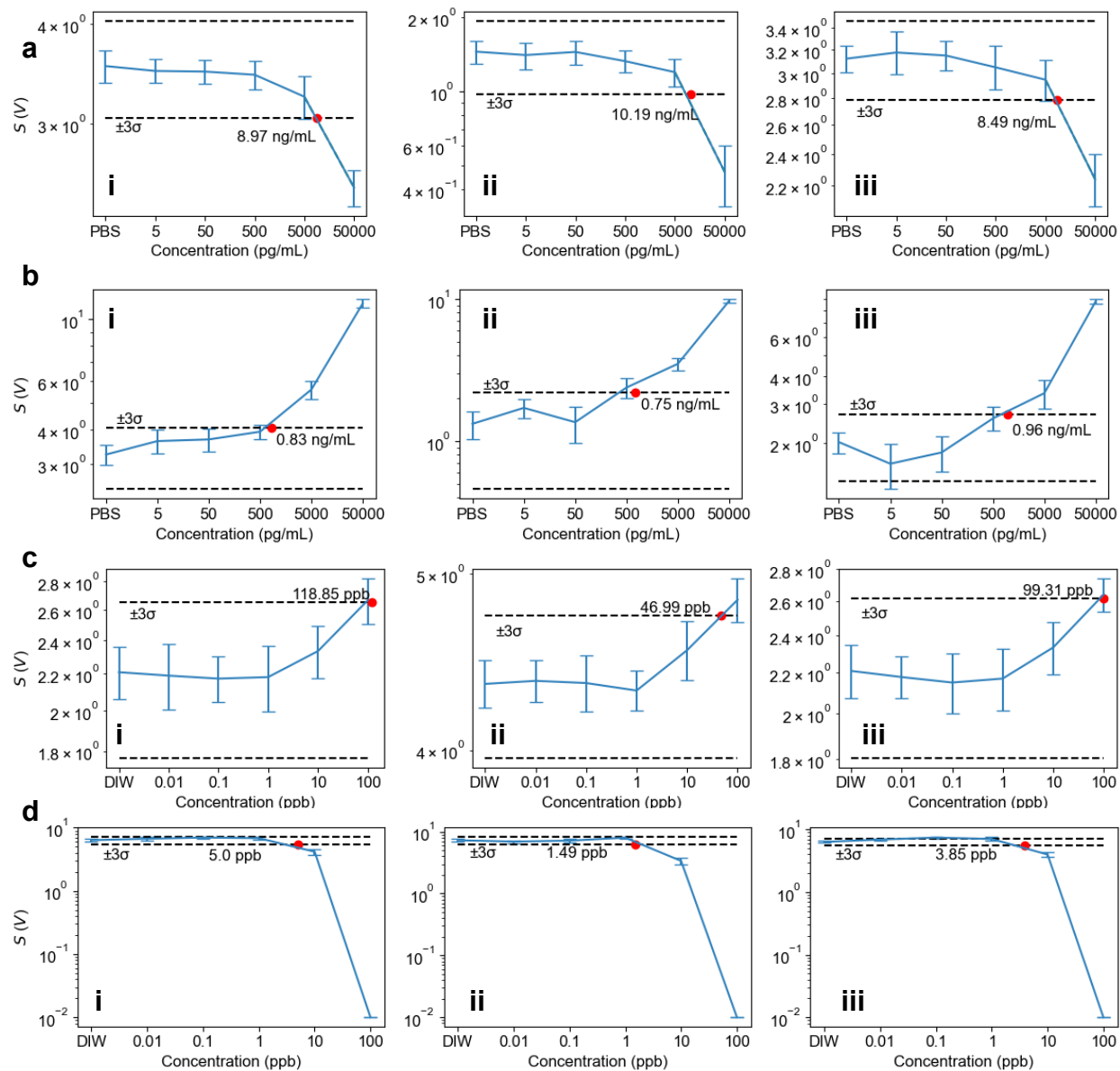


Figure S9. Limit of detection estimation for IL-6 (a) TGF (b) DMF and PFOA (c) TGF (d) DMF for three distinct devices (i to iii).

S10. Volatile organic compound measurement setup

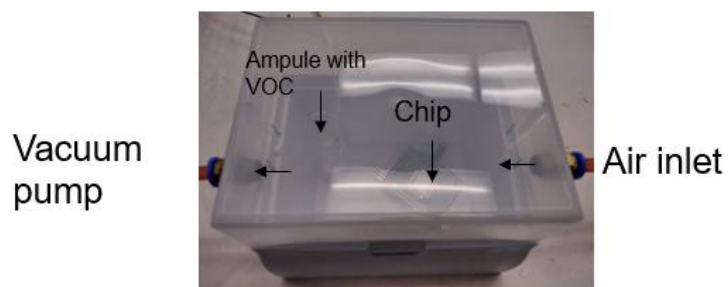


Figure S10. Optical image of the volatile organic compound (VOC) measurement setup. The system consists of an enclosed container purged with clean dry air (CDA) to establish a controlled baseline atmosphere. A known quantity of VOC is introduced by bubbling CDA through an enclosed container containing the liquid VOC, allowing controlled evaporation into the main chamber.