nature electronics

SUPPLEMENTARY INFORMATION

https://doi.org/10.1038/s41928-018-0038-8

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Flexible CMOS integrated circuits based on carbon nanotubes with sub-10 ns stage delays

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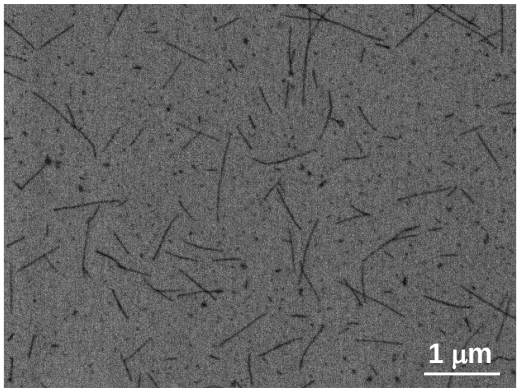
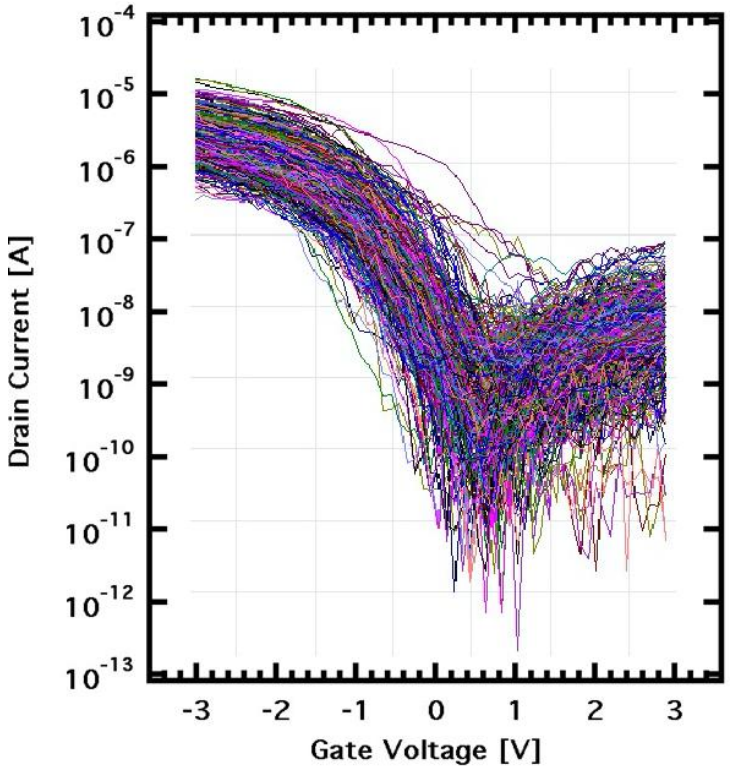
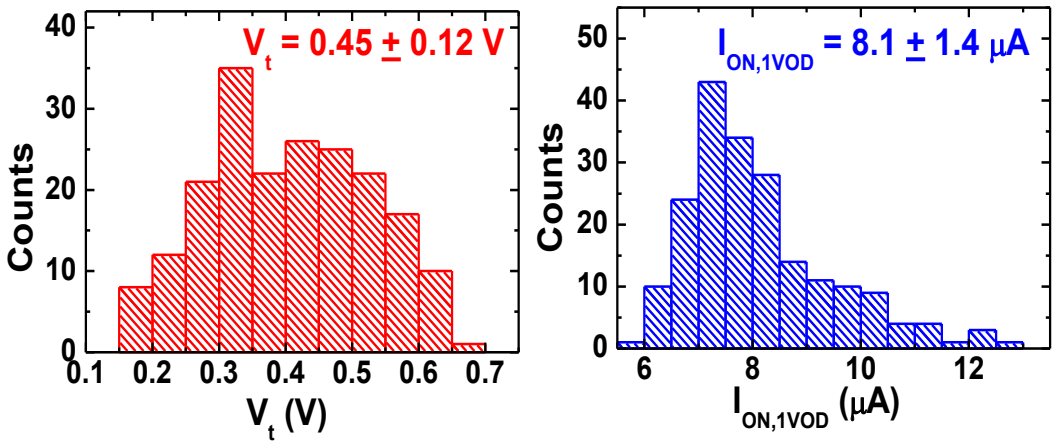


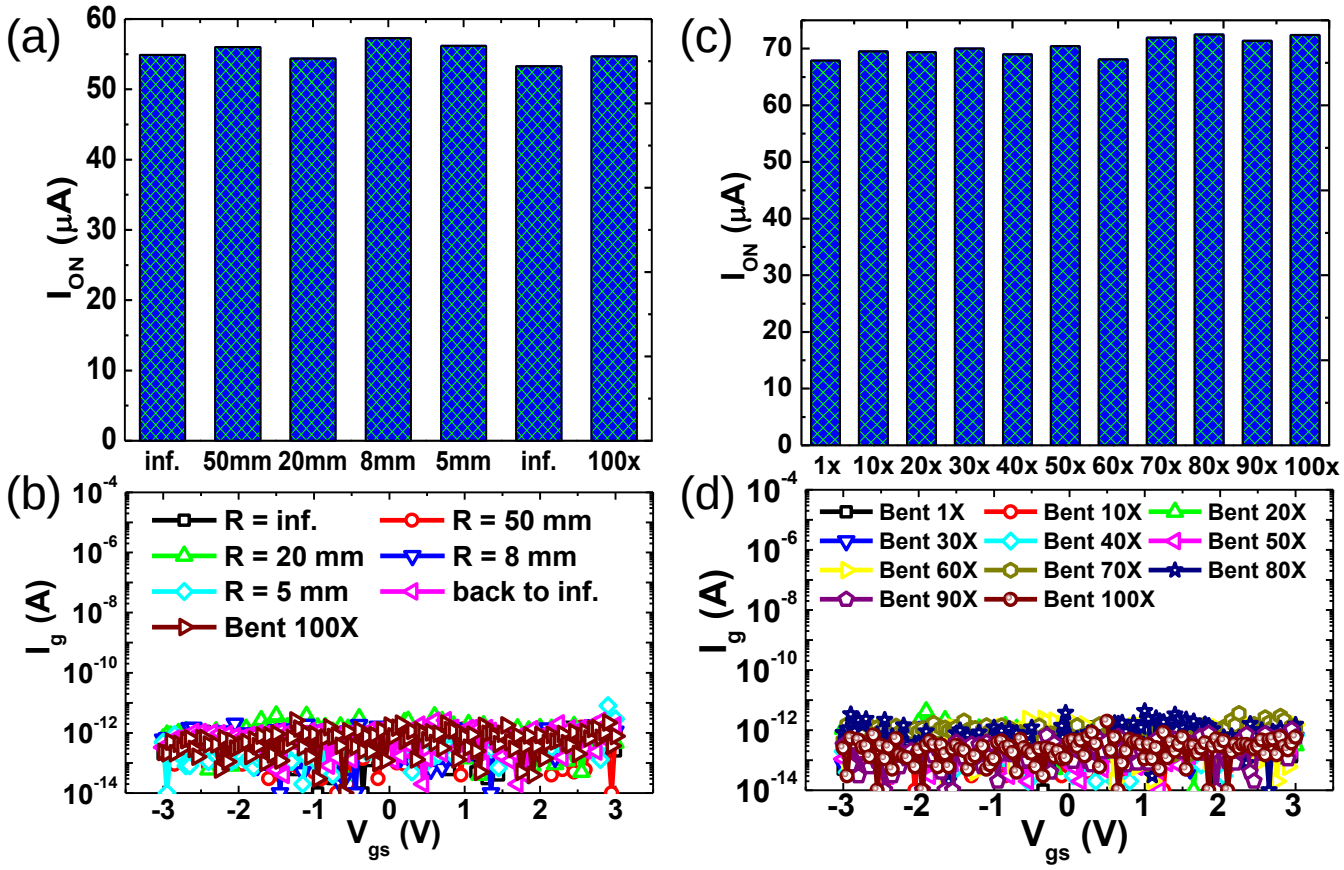
Supplementary Figure 1. **Estimation of carbon nanotube length**. SEM image of "sparse" carbon nanotubes dispersed on a SiO_2/Si substrate to estimate the tube length. Most CNTs have length between 0.5-1.5 μm, and the average tube length is about 1 μm.



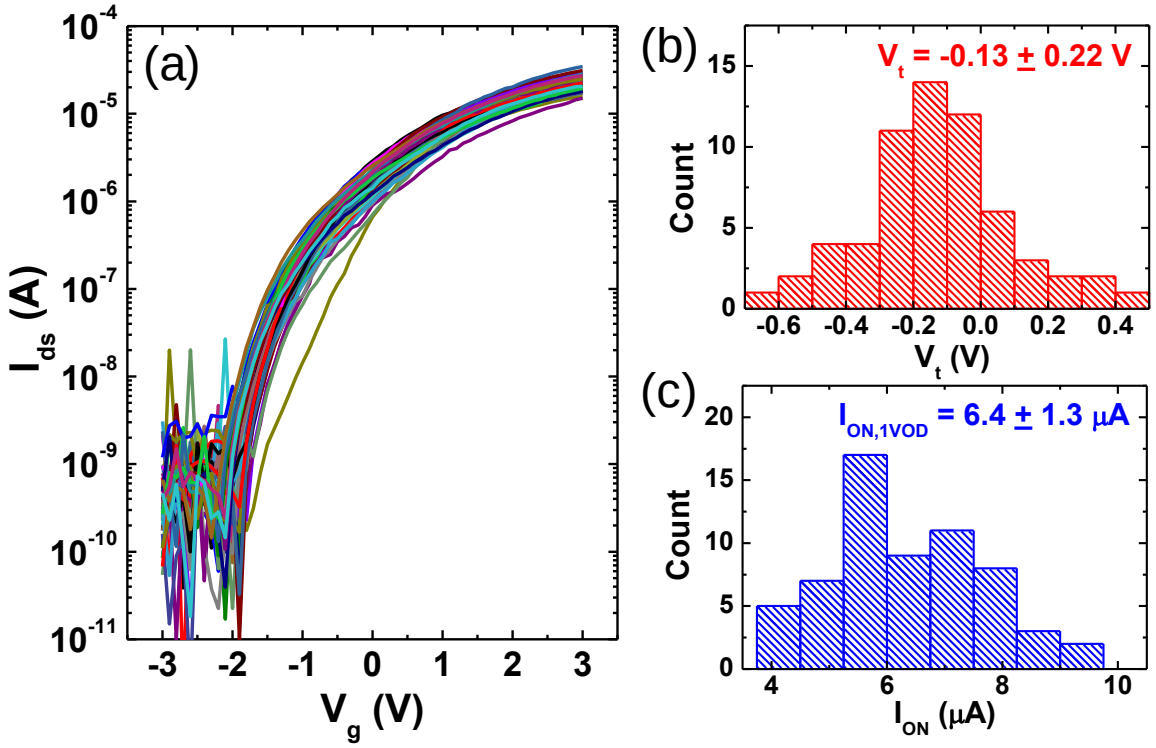
Supplementary Figure 2. Electrical testing of semiconducting CNT purity. I_{ds}−V_{gs} transfer curves at V_{ds} = −0.5 V from 1,000 representative CNT transistors with a nominal channel length of L_{ch} ~150 nm. No metallic (non-modulating or weakly modulating) device was observed. To further quantify the semiconducting CNT purity beyond the detection limit of absorption spectrum, we have done electrical testing on samples consisted of in total about 21,000 CNT field-effect transistors (nominal L_{ch} ~150 nm) using a semi-automated probe station. Those devices were fabricated using the same CNT solution (diluted) for TFT fabrication in this study. Out of 18,595 conductive devices (implying one or several CNTs across the channel), no metallic device was observed. This result implies a semiconducting tube purity over 99.99%.



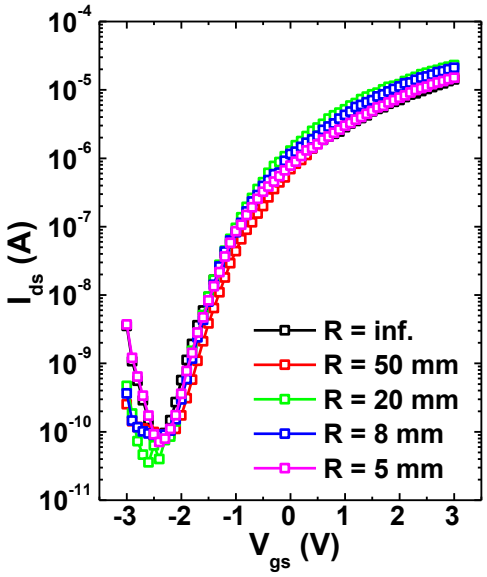
Supplementary Figure 3. Statistics analysis of CNT TFTs. Histogram of 250 CNT TFTs (W_{ch} = 10 μm, L_{ch} = 2 μm) threshold voltage V_t (left panel) and ON current (right panel) at a constant gate overdrive ($|V_{gs} - V_t|$ = 1 V) for **Fig. 2a** in the main text. The observed variability is mainly because of the process limitations on flexible substrates, especially the spatial variation in tube density (which can be roughly seen from the SEM image in **Fig. 1c** in the main text) and also possibly process contaminations (e.g., trapped charged particles or molecules on flexible substrate surface could induce V_t shift). Devices made on rigid SiO_2/Si substrates using a similar process have shown much smaller variability. Therefore, it is possible that the variability demonstrated in this work can be largely reduced by improving process conditions, such as substrate cleanliness and flatness, uniformity in tube deposition (or using other techniques better than simple drop-casting method) and also gate dielectric deposition, *etc*. For commercial technologies, it is generally important to control the I_{ON} variation within 5~10% and V_t variation within ~0.5 V. However it should be noted that the acceptable variation levels highly depend on the specific applications as they may have varying circuit designs and operation tolerances. For example, in TFT-based display technology, peripheral circuits are usually used to compensate TFT variations in V_t and I_{ON} so that it may tolerate larger variations of 15-20% or even higher.



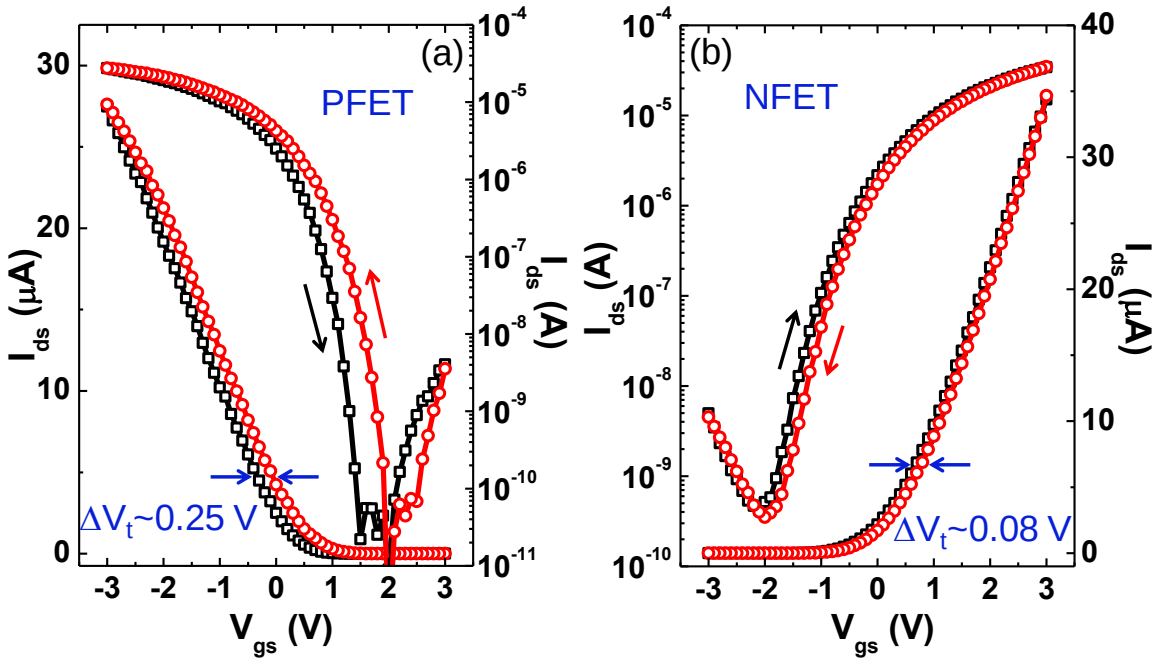
Supplementary Figure 4. Durability test of CNT TFTs. (a) Device ON current and (b) gate leakage during bending tests with different bending radii on an individual CNT TFT. (c) Device ON current and (d) gate leakage during repeated bending tests up to 100 times on another CNT TFT. In both experiments, there was no apparent degradation on the device performance and no damage on the gate oxide was found.



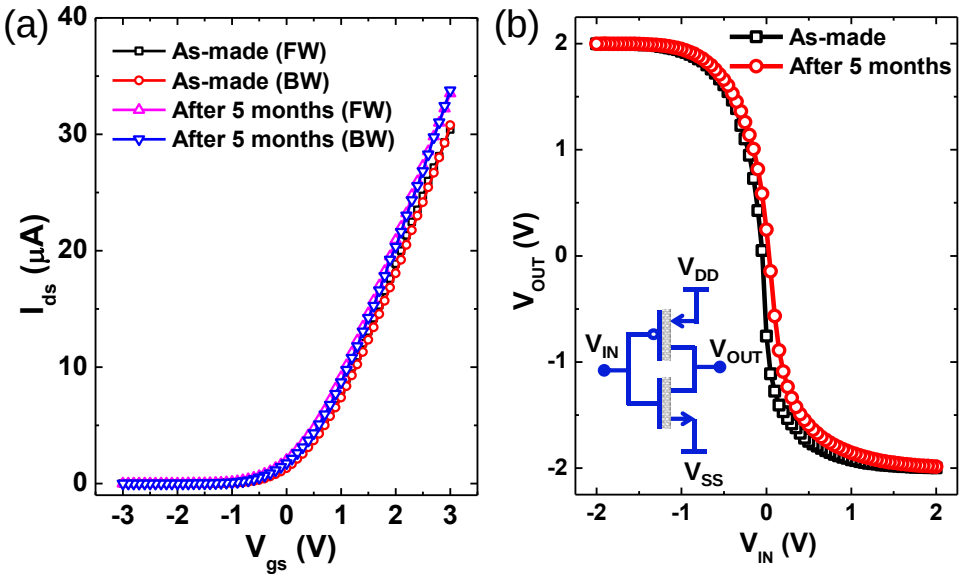
Supplementary Figure 5. Statistics analysis of CNT NFETs. (a) I_{ds}–V_{gs} transfer curves at V_{ds} = 0.5 V for 64 CNT NFETs. The carrier mobility in NFETs was estimated as: $\mu = 40 \pm 7$ cm^2/Vs. (b) Histogram of threshold voltage V_t. (c) Histogram of ON current (right panel) at a constant gate overdrive ($|V_{gs} - V_t| = 1$ V).



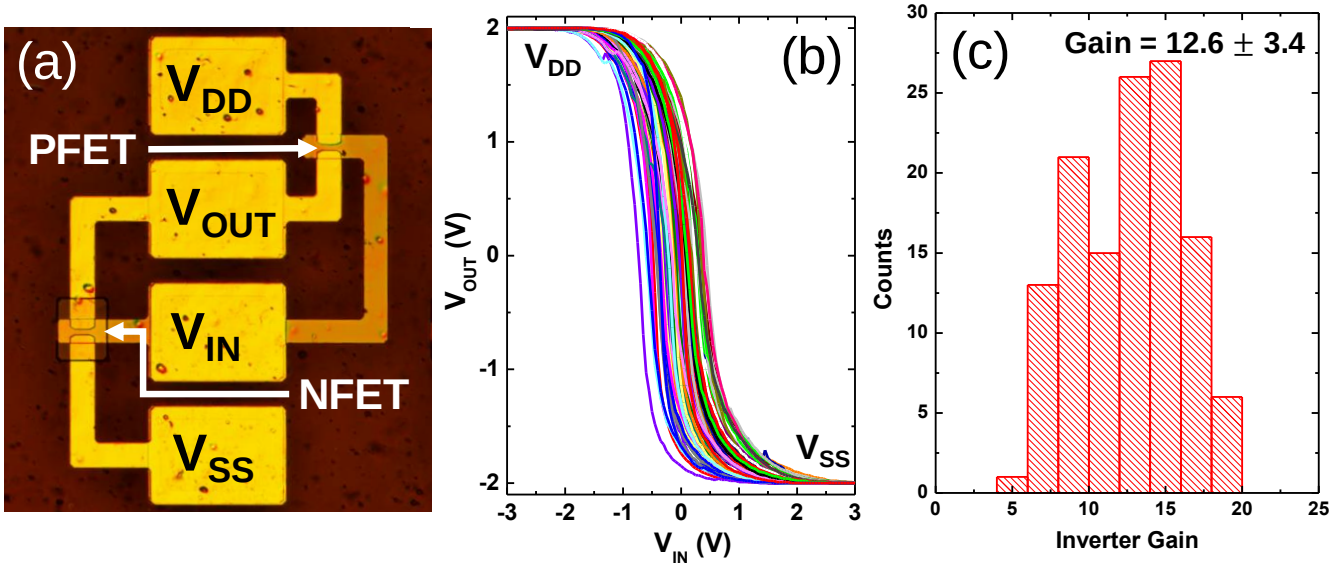
Supplementary Figure 6. Bending tests of CNT NFETs. I_{ds}–V_{gs} transfer curves at V_{ds} = 0.5 V of a typical CNT NFET bent under different radii *R*, showing no degradation on the device performance with *R* down to 5 mm. Although the NFET involves more complex capping oxide layers (mainly Al_2O_3), those oxide layers were very similar (in terms of thickness and deposition condition) to the gate oxide (HfO_2/Al_2O_3 by ALD) used in both PFET and NFET, and they were both shown to be robust during bending tests.



Supplementary Figure 7. Hysteresis in CNT TFTs. (a) Dual-sweep I_{ds}−V_{gs} transfer curves at V_{ds} = −0.5 V of a typical CNT PFET in both linear scale (left axis) and logarithmic scale (right axis). (b) Dual-sweep I_{ds}−V_{gs} transfer curves at V_{ds} = 0.5 V of a typical CNT NFET in both linear scale (right axis) and logarithmic scale (left axis). CNT PFET exhibited a relatively small hysteresis ($\Delta V_t \sim 250$ mV), and it was significantly reduced in the NFET ($\Delta V_t \sim 80$ mV) that was well passivated by the *n*-type doping layer. The small hysteresis is likely attributed to charge trapping by molecules (e.g., water) near carbon nanotubes absorbed from the atmosphere, which has been extensively studied in the literature. The hysteresis can be readily reduced by appropriate passivation using polymers (e.g., Ha, et al., *ACS Appl. Mater. Interfaces* **6**, 8441, 2014) or oxides (as in the case of NFET). Those molecules are typically slow "charge traps" so no hysteresis is expected in high-frequency operations (e.g., Park, et al., *ACS Nano* **10**, 4599, 2016).



Supplementary Figure 8. Stability of CNT NFETs and CMOS inverters. (a) I_{ds}−V_{gs} transfer curves at V_{ds} = 0.5 V of an as-made CNT NFET and re-measured after 5 months. The "FW" and "BW" indicate forward (from −3 V to 3 V) and backward (from 3 V to −3 V) gate sweeping, respectively. The NFET showed no apparent degradation in device performance and hysteresis over time. (b) Output characteristics of an as-made CNT CMOS inverter and re-measured after 5 months. The bottom inset shows the schematic diagram of CMOS inverter. Both NFET and inverter showed excellent stability over time.



Supplementary Figure 9. Statistics analysis of CNT CMOS inverters. (a) Microscope image of a CNT CMOS inverter. (b) Output characteristics of 125 CNT CMOS inverters (V_{DD} = 2 V, V_{SS} = −2 V). (c) Histogram of the extracted inverter gain, showing an average gain of 12.6.