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SUPPLEMENTARY INFORMATION

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Resistive random-access memory based on ratioed memristors

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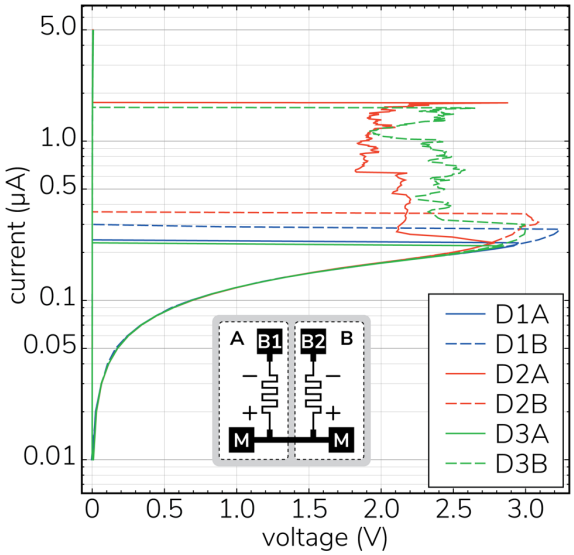
Supplementary Notes and Figures

Supplementary Note 1: Experiment E1

The objective of Experiment E1 is to highlight the extent of the device-to-device and cycle-to-cycle variations of memristors, and illustrate the capability of our ratio-based encoding to reduce the effect caused by such variations. Three pairs of pristine (unformed) memristors (D1, D2 and D3) were used, each pair consisting of two anti-serially connected bipolar memristors (D#A and D#B), corresponding to the left and right memristors in an H3 cell. Each pair is a small 1-by-2 crossbar with two bottom electrodes (B1 and B2) and one top or middle electrode (M), as schematically shown in the inset in Supplementary Figure 1. Details on the device structure can be found in [1]. All measurements were performed on an Agilent 4156C analyser. The experiment is as follows:

1. We individually electroformed each memristor by applying a quasi-static current sweep of 5 µA at electrode M, grounding the bottom electrode of the device being formed, and leaving the other bottom electrode floating.
2. Once formed, we individually reset each memristor with a negative voltage sweep of −1.6 V applied to electrode M while grounding the bottom electrode of the device that we were resetting and floating the bottom electrode of the other device.
3. Then, we set and reset each memristor for four cycles with a voltage sweep of 1.6 V for set and −1.5 V for reset, applied at electrode M and grounding/floating the corresponding bottom electrode. For the set operation, we used an external current compliance of 1 mA.
4. Finally, we cycled four more times the memristors, but now as a pair (D1, D2 and D3), by applying a voltage sweep of 2 V and −2 V at electrode B1, grounding electrode B2, and measuring the voltage at electrode M.

To minimize the effect of device degradation and/or aging, the four voltage-voltage sweeps in step 4 were conducted immediately after the four current-voltage sweeps in step 3 for each pair. Supplementary Figure 1 shows the applied current and measured voltage at electrode M for each device during its electroforming step. All devices exhibited an initial high resistance of 8 MΩ @ 1 V and began to form with a voltage of around 3 V, consistent with what was reported in [1] for the same devices.



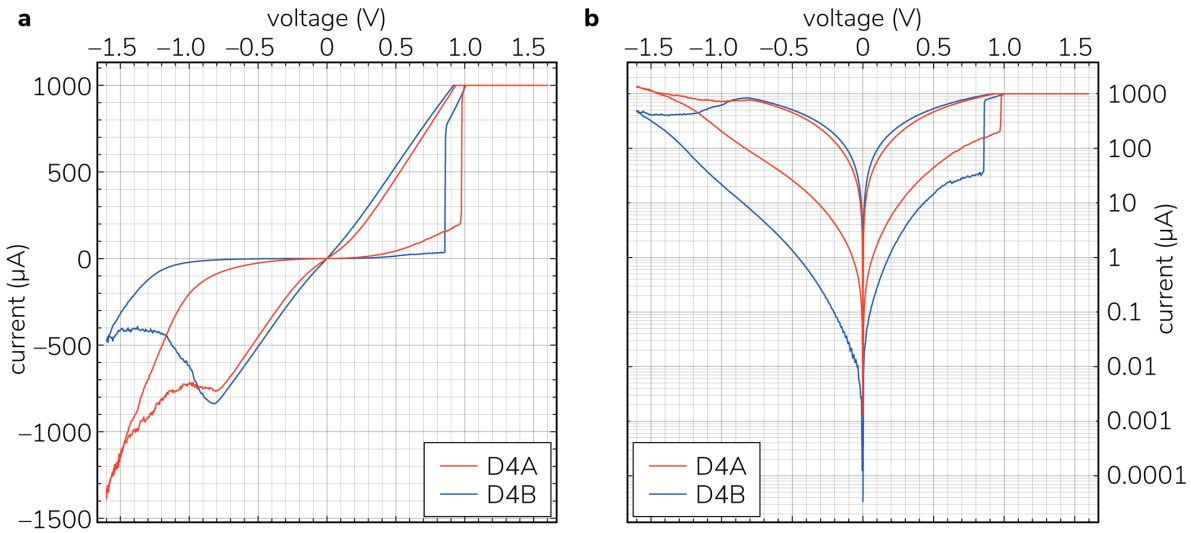
Supplementary Figure 1. Initial electroforming step. Electroforming step and device structure for pairs of devices D1, D2 and D3.

Supplementary Note 2: Experiment E2

No single set of write voltages (for set and reset) will be optimal for all memristors in a memory system. Programming voltages that are too low may result in partial switching. Programming voltages that are too high may end up with either excessively thick filaments [2] during sets, or the over-RESET problem [3] during resets. A consequence of using a fixed set of programming voltages is that some memristors, over their lifetime, may accumulate errors in their state to the point of corrupting the encoded data. The objective of Experiment E2 is to demonstrate the robustness of our ratio-based solution with respect to changes in the HRS/LRS ratio and absolute LRS and HRS resistances throughout the lifetime of a memristor. We used a different pair of devices (D4A and D4B) with the same configuration, same electroforming, and same initial reset, as described in Experiment E1. Then:

1. We independently set and reset D4A and D4B in batches of 20 cycles, with 10 µs voltage pulses applied at their electrode M, while grounding the bottom electrode. No current compliance was enforced. We used a pulse of 1.3 V for set, and −1.7 V for reset. After each set/reset pulse, a read pulse of 100 mV was applied and the current was measured and integrated for 1 ms.
2. We cycled again D4A and D4B, but now as a pair. We applied 10 µs voltage pulses of 2 V and −2 V at electrode B1, while grounding electrode B2. After each pulse, a read pulse of 100 mV was applied, and the voltage at electrode M was measured and integrated for 1 ms.
3. After each 20-cycle batch, we visually assessed if the device's window had started to close, and if so, we manually voltage-swept the device to bring its original window back (a *refresh* operation).

Devices D4A and D4B were deliberately chosen as they exhibited a large discrepancy in their I-V characteristics, as shown in Supplementary Figures 2a and 2b for linear and logarithmic scales, respectively. We found that device D4A had a particularly weak HRS (1.7 µA @ 100 mV), which contrasted to the stronger HRS of device D4B (0.28 µA @ 100 mV). The LRS for devices D4A and D4B were 57 µA @ 100 mV and 94 µA @ 100 mV, respectively.



Supplementary Figure 2. Characteristic I-V plot for devices D4A and D4B. a, I-V plot in linear scale. **b**, I-V plot in logarithmic scale.

Supplementary Note 3: Mechanism behind the improved state uniformity

The mechanism behind the improved uniformity does not come from measuring the state of the device as a voltage versus as a current, neither from the fact that the two memristors are anti-serially connected. The improvement is due to measuring the "ratio" of the states of the two memristors. The anti-serial connection merely provides a convenient way to program the devices as a complementary resistive switch (CRS), while also providing a convenient way of measuring the state of the device as a voltage divider (i.e., it directly outputs the ratio of the memristor's resistance). Note that the same voltage divider effect can be obtained if the devices were serially connected.

The uniformity can be explained by comparing the probability of encoding an error. In a resistance-based approach (that uses the absolute resistance of a single memristor to encode a binary bit), an encoding error occurs if either (1) the intended device's LRS is below the reference current, **OR** (2) the device's HRS is above such reference current. In contrast, in our ratio-based encoding (that uses the ratio of resistances of two memristors to encode a binary bit), an encoding error occurs only when two conditions are **simultaneously** met: the intended LRS of one memristor becomes higher than some value **AND**, the intended HRS of the other memristor becomes lower than the same value, which is much less likely to happen.

To illustrate this, let us assume that under all D2D and C2C variations, the LRS and HRS of a memristor are normally distributed with mean μ_{LRS} and standard deviation σ_{LRS} for the LRS, and μ_{HRS} and σ_{HRS} for the HRS. While this may be an oversimplification, it helps illustrate our point. Assuming a current sensing approach, all units are in units of current, and thus $\mu_{LRS} > \mu_{HRS}$, as shown in the inset in Figure R1. Let us further assume that X_{LRS} and X_{HRS} are two normally distributed random variables described by $[\mu_{LRS}, \sigma_{LRS}]$ and $[\mu_{HRS}, \sigma_{HRS}]$, respectively.

Traditional resistance-based current sensing approach: Given a global, fixed reference G_{ref}, X_{LRS} will be correctly considered a logic '1' if $X_{LRS} > G_{\text{ref}}$, and X_{LRS} will be correctly considered a logic '0' if $X_{HRS} < G_{\text{ref}}$. Let A be the event of incorrectly interpreting X_{LRS} as logic '0', and B the event of incorrectly interpreting X_{HRS} as logic '1'. In a traditional resistance-based current sensing approach, the probability of A occurring can be then expressed as:

$$P(A) = P(X_{LRS} < G_{\text{ref}}) = \int_{-\infty}^{G_{\text{ref}}} \frac{e^{-\frac{(x-\mu_{LRS})^2}{2\sigma_{LRS}^2}}}{\sqrt{2\pi\sigma_{LRS}^2}}\,dx = \frac{\frac{1}{\sqrt{1/\sigma_{LRS}^2}} - \sigma_{LRS}\text{erf}\left(\frac{\mu_{LRS} - G_{\text{ref}}}{\sqrt{2}\sigma_{LRS}}\right)}{2\sigma_{LRS}},$$

and the probability of B occurring can be expressed as:

$$P(B) = P(X_{HRS} > G_{\text{ref}}) = \int_{G_{\text{ref}}}^{\infty} \frac{e^{-\frac{(x-\mu_{HRS})^2}{2\sigma_{HRS}^2}}}{\sqrt{2\pi\sigma_{HRS}^2}}\,dx = \frac{\frac{1}{\sqrt{1/\sigma_{HRS}^2}} + \sigma_{HRS}\text{erf}\left(\frac{\mu_{HRS} - G_{\text{ref}}}{\sqrt{2}\sigma_{HRS}}\right)}{2\sigma_{HRS}}.$$

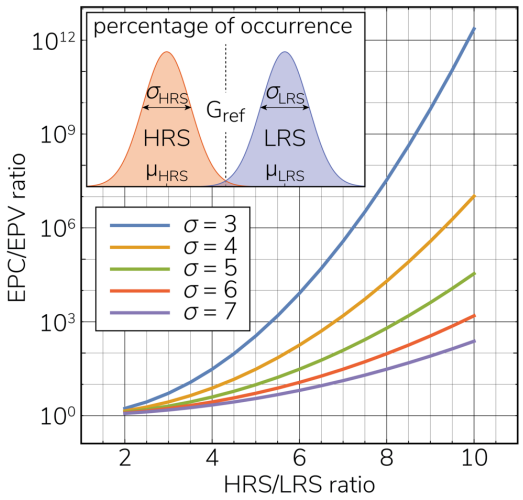
Assuming an equal probability for a cell to store logic '0' or logic '1', the probability of storing an erroneous logic value using a resistance-based current sensing approach (EPC) can be calculated as:

$$\text{EPC} = 0.5 * P(A) + 0.5 * P(B).$$

Proposed ratio-based voltage sensing approach: Let us assume that the variations of both memristors in an H3 cell follow the same $[\mu_{LRS}, \sigma_{LRS}]$ and $[\mu_{HRS}, \sigma_{HRS}]$ parameters. In such case, the probability of storing an erroneous logic '1' in an H3 cell will be equivalent to the probability of storing a logic '0'. Regardless of the logic stored in an H3 cell, the state of one memristor will be given by X_{LRS} while the other will be given by X_{HRS}. Thus, an H3 cell will store an erroneous value if $X_{LRS} < X_{HRS}$, whose probability is equal to that of $X_{LRS} - X_{HRS} < 0$. Since both X_{LRS} and X_{HRS} are normally distributed, their difference is also normally distributed. Therefore, the probability of an H3 cell to store an erroneous logic value under our ratio-based voltage sensing approach (EPV) can be expressed as:

$$\text{EPV} = P(X_{LRS} - X_{HRS} < 0) = 0.5\left(\text{erf}\left(\frac{\mu_{HRS} - \mu_{LRS}}{\sqrt{2}\sqrt{\sigma_{HRS}^2 + \sigma_{LRS}^2}}\right) + 1\right).$$

To eliminate the G_{ref} variable from the EPC expression, let us further assume that both LSR and HRS have the same standard deviation ($\sigma_{LRS} = \sigma_{HRS} = \sigma$), thus the optimal global reference G_{ref} of the resistance-based approach is simply $(\mu_{LRS} + \mu_{HRS})/2$. Supplementary Figure 3 shows a numerical example of the relative performance of our ratio-based approach compared to a resistance-based approach (EPC/EPV ratio). We plot the expected EPC/EPV ratio as a function of the LRS/HRS ratio (μ_{LRS}/μ_{HRS} ratio) under various σ values in the range of 3 to 7, for a base HRS of $\mu_{HRS} = 5$. Both μ_{HRS} and σ are given in arbitrary units. As shown in Figure R1, a linear change to both LRS/HRS ratio and σ result in a super-exponential reduction in the error probability of our ratio-based approach (EPV) versus the resistance-based approach (EPC).



Supplementary Figure 3: Under normally distributed LRS and HRS (measured in terms of current for a given read voltage), our ratio-based encoding result in a significantly smaller error probability compared to a resistance-based encoding.

Supplementary Note 4: Experiment E3

The objective of Experiment E3 is to demonstrate the write operation in an H3 cell, and to evaluate the effectiveness of using the middle terminal of an H3 cell to (1) reduce the effective write voltage needed to complete a write transition for cells we intend to write into, and (2) increase the effective write voltage, while preventing or blocking a write transition for half-selected cells we want to protect from an unintentional write. Cases (1) and (2) outlined above are further compared with a similar study using a regular CRS-inspired write operation (Case (3)), which do not have access to the middle terminal. We used another pair of devices (D5A and D5B) with the same material and initialization as described in Experiments E1 and E2, but with an opposite anti-serial polarity. In all three cases, we set device D5 into a LRS|HRS configuration and applied a ramp of 10 µs pulses (V_{PULSE}) from 1 V to 2.2 V (with a step size of 6 mV) at electrode B1 (grounding electrode B2) with interleaved read pulses of 100 mV (integrated for 1 ms). For the **CRS-inspired write case** (i.e. Case (3)), we floated electrode M. For the **two-step mFET-assisted write case** (i.e. Case (1)), we applied a voltage pulse of magnitude V_{ASSIST} at electrode M. During the first step, $V_{ASSIST} = V_{PULSE}$ (to enforce the LRS|LRS configuration). During the second step, $V_{ASSIST} = 0$ V (to enforce the final HRS|LRS configuration). This second step is triggered when the voltage at the middle electrode is close to 50 mV (55 mV in this experiment). For the **mFET-assisted block case** (i.e. Case (2)), we applied a voltage pulse $V_{BLOCK} = V_{PULSE}/2$ at electrode M. To enable a fair comparison, we interleaved the write operations (mFET assist→CRS write→mFET block), and before each write, we initialized the state of D5A and D5B to 3 µA @ 100 mV and 15 µA @ 100 mV, respectively, using an adaptation of the algorithm described in [7]. Such a reduced state range (3-15 µA @ 100 mV) and a smaller LRS/HRS ratio of 5 were adopted to prevent abrupt changes in the device's state (a known source of variations). For the mFET-assisted **write** and **block** cases, we used a fix resistor of 5 kΩ to represent the 'ON' resistance of the mFET. Figure 6 in the main text summarizes this experiment with 15 consecutive write cycles for each case (45 cycles in total). Compared to the CRS write, an mFET-assisted write crosses the 20% upper margin at a lower voltage (1.5 V vs. 1.75 V) and complete the LRS|HRS→HRS|LRS transition at a lower voltage (e.g. at 2 V all curves are well within the 20% lower margin, whereas only 1 out of 15 cycles of a regular CRS write are below the 40%). On average, an mFET-assisted write crosses the 20% lower margin 0.3 V earlier than the CRS write, while the mFET-assisted block delays crossing the upper 20% about 0.1 V, as shown in Figure 6h. Note that half-selected devices experience half of the voltage (under a 'V/2' biasing scheme) reported in Figure 6 (e.g. 1-1.1 V) which is not disturbing in any case.

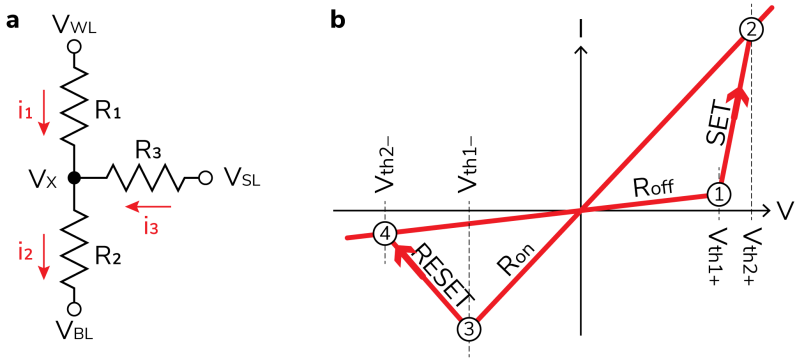
Supplementary Note 5: Valid Write Region

To estimate the valid write region, we model an H3 cell as a four-terminal voltage divider, illustrated in Supplementary Figure 4a, and described by:

$$V_x = \frac{R_1R_2V_{SL} + R_1R_3V_{BL} + R_2R_3V_{WL}}{R_1R_2 + R_1R_3 + R_2R_3}$$

where V_x is the voltage at the middle electrode, V_{WL}, V_{BL} and V_{SL} are the voltages applied to the word, bit, and sense lines, respectively. R_1 and R_2 are the resistances of the left and right memristors, and R_3 is the resistance of the mFET. The resistances of R_1, R_2 and R_3 are in general voltage dependant, but for simplicity they are modelled as linear resistors. The resistance for R_1 and R_2 can be switched between a high resistance state (HRS) with a value of R_{off}, and a low resistance state (LRS) with a value of R_{on}. The resistance for R_3 is modelled as an open circuit, when the mFET is disabled, and with a resistance of αR_{on} when the mFET is enabled, where α is a design parameter. Note that during an mFET-assisted write, V_x can be arbitrarily shifted is a function of R_3 and V_{SL}, to either assist a write operation (for the targeted cell), or to hinder it (for half-selected and unselected cells).

Supplementary Figure 4b shows the change in resistances for resistors R_1 and R_2 as a function of the applied voltage across its terminal, the state resistances R_{on} and R_{off}, set threshold voltages V_{th1+} and V_{th2+}, and reset threshold voltages V_{th1-} and V_{th2-}. In general, for voltage sweeps, the set transition (between points ① and ②) tends to be sharper than the reset transition (between points ③ and ④) since the former is a positive-feedback process [4] whereas the latter is more gradual and controlled [5, 6].



Supplementary Figure 4. Simplified H3 cell and memristor models. a, Simplified resistive model of an H3 cell. The mFET is modelled as a resistor R_3. **b**, Simplified I-V model for a voltage-controlled bipolar memristor.

As in a CRS cell, an H3 cell's I-V characteristics is symmetric, and thus is sufficient to describe the valid write region for a single write transition, e.g., from logic '0' to logic '1'. Here we consider writing a logic '1' (HRS|LRS configuration) into an H3 cell that currently stores a logic '0' (LRS|HRS configuration) using a CRS-inspired write operation. To do so, a voltage V_{W1} is applied as a voltage difference $V_{WL} - V_{BL}$. Then, we define the *valid write region* as the parameter region in which for a given combination of write voltage V_{W1}, state resistances R_{on} and R_{off}, set threshold voltages V_{th1+} and V_{th2+}, and reset threshold voltages V_{th1-} and V_{th2-}, the following three conditions are simultaneously met:

- **C1:** While applying the write voltage V_{W1}, the left memristor (R_1), that is in HRS, must be able to be fully transition to a LRS without disturbing the right memristor (R_2), that is LRS, i.e., the LRS|LRS configuration must be reachable.
- **C2:** Once in the LRS|LRS configuration, the same voltage V_{W1} should be high enough to complete the transition to the desired LRS|HRS configuration.
- **C3:** All the half-selected and unselected devices must not be disturbed.

Condition **C1** itself is met if all the following statements are true:

C1.1: The voltage across R_1 (in LRS) is less than its first reset threshold $|V_{th1-}|$ while R_2 is in HRS. That is:

$$\textbf{C1.1} = |V_x - V_{WL}| < |V_{th1-}|$$

for $R_1 = R_{on}$, $R_2 = R_{off}$, $V_{WL} = V_{W1}/2$ and $V_{BL} = -V_{W1}/2$.

C1.2: The voltage across R_2 (in HRS) is greater or equal than its first set threshold $|V_{th1+}|$ while R_1 is in LRS. That is:

$$\textbf{C1.2} = |V_x - V_{BL}| \geq |V_{th1+}|$$

for $R_1 = R_{on}$, $R_2 = R_{off}$, $V_{WL} = V_{W1}/2$ and $V_{BL} = -V_{W1}/2$.

C1.3: The voltage across R_2 (in LRS) is greater or equal than its second set threshold $|V_{th2+}|$ while R_1 is in LRS. That is:

$$\textbf{C1.3} = |V_x - V_{BL}| \geq |V_{th2+}|$$

for $R_1 = R_{on}$, $R_2 = R_{on}$, $V_{WL} = V_{W1}/2$ and $V_{BL} = -V_{W1}/2$.

C1.4: The voltage across R_1 (in LRS) is less than its first reset threshold $|V_{th1-}|$ while R_2 is in LRS. That is:

$$\textbf{C1.4} = |V_x - V_{WL}| < |V_{th1-}|$$

for $R_1 = R_{on}$, $R_2 = R_{on}$, $V_{WL} = V_{W1}/2$ and $V_{BL} = -V_{W1}/2$.

Once condition **C1** is met (i.e. a stable LRS|LRS was reached), condition **C2** will be met if all the following statements are true:

C2.1: The voltage across R_1 (in LRS) is greater than its first reset threshold (its absolute value) $|V_{th1-}|$ while R_2 is in LRS. That is:

$$\textbf{C2.1} = |V_x - V_{WL}| \geq |V_{th1-}|$$

for $R_1 = R_{on}$, $R_2 = R_{on}$, $V_{WL} = V_{W1}/2$ and $V_{BL} = -V_{W1}/2$.

C2.2: The voltage across R_1 (in HRS) is greater than its first reset threshold (its absolute value) $|V_{th2-}|$ while R_2 is in LRS. That is:

$$\textbf{C2.1} = |V_x - V_{WL}| \geq |V_{th2-}|$$

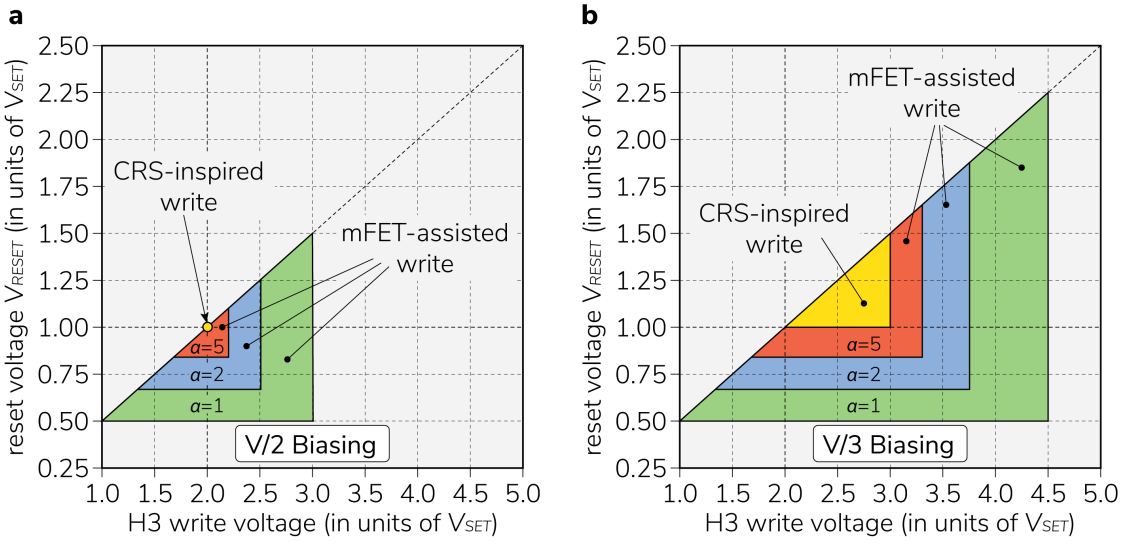
for $R_1 = R_{off}$, $R_2 = R_{on}$, $V_{WL} = V_{W1}/2$ and $V_{BL} = -V_{W1}/2$.

Condition **C3** is met if the maximum applied voltage is less than the first set threshold V_{th1+} of (1) all same-row half-selected devices, (2) all same-column half-selected devices, and (3) all unselected devices. That is:

$$\textbf{C3} = |V_x - V_{BL}| < |V_{th1+}|$$

for $R_1 = R_{on}$, $R_2 = R_{off}$.

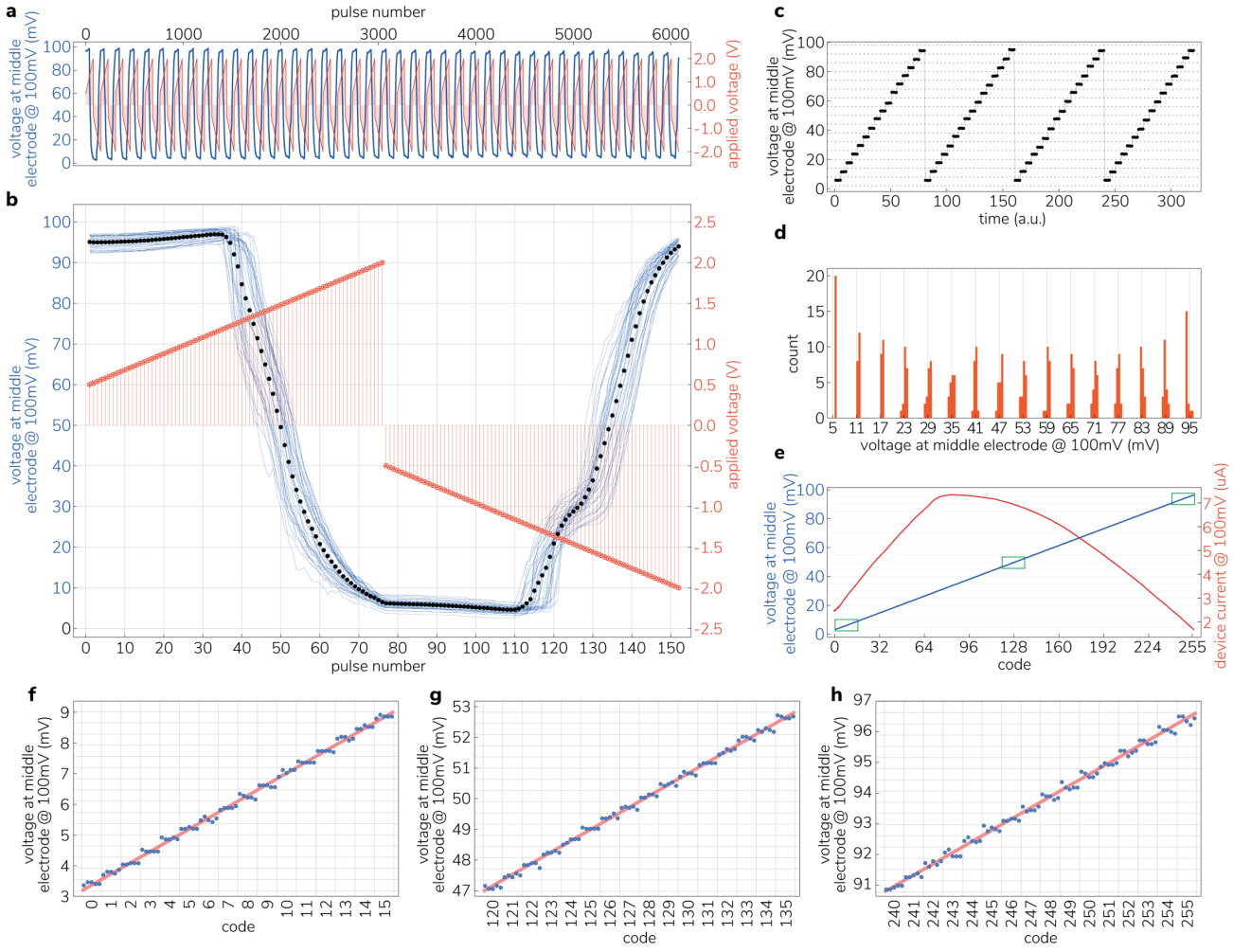
For condition **C3**, voltages V_{WL} and V_{BL} depend on the biasing scheme used. In general, $V_{WL} - V_{BL} = V_{W1}/b \pm \varepsilon$, where $b = 2$ for a V/2 biasing scheme, and $b = 3$ for a V/3 biasing scheme. For the V/2 biasing scheme, ε is a parameter (fixed for a given configuration) that equalizes the disturbance effect for the same-row and same-column devices. For the V/3 biasing scheme, ε is set to equalize the disturbance of the same-row, same-column, and unselected devices. $\varepsilon = 0$ for a CRS-inspired write. $\varepsilon \neq 0$ for an mFET-assisted write, since V_{BLOCK} can only be applied to the same-row devices, but not to the same-column devices.



Supplementary Figure 5: Valid write region comparison between the CRS-inspired write (in yellow) and our mFET-assisted write (in coral, blue and green) as a function of the write voltage for H3 cells, the reset voltage for memristors, and mFET ON resistance. a, The valid write region assuming a V/2 biasing scheme, in which a write voltage V ($|V_{W0}|$ or $|V_{W1}|$) is applied to the selected word line, V/2 to the unselected word and bit lines, and the ground potential (0V) to the selected bit line. For the CRS-inspired write, the mFET is disabled. For the mFET-assisted write, the selected mFET is enabled and a voltage V_{ASSIST} = V is applied to the selected sense line. A voltage V_{BLOCK} = V/2 is applied to the unselected (but enabled) mFETs. Note that the valid write region for the CRS-inspired write is a single point where $|V_{W0}| = |V_{W1}| = |2V_{SET}| = |2V_{RESET}|$, which is not realistic due to variations in V_{SET} and V_{RESET}. **b**, The valid write region assuming a V/3 biasing scheme. In both **a** and **b**, the H3 write voltage ($|V_{W0}|$ or $|V_{W1}|$) and reset voltage V_{RESET} are normalized with respect to the set voltage for memristors V_{SET}. The ON resistance of the mFET is defined as α times the resistance of a memristor in an LRS.

Supplementary Note 6: Experiment E4

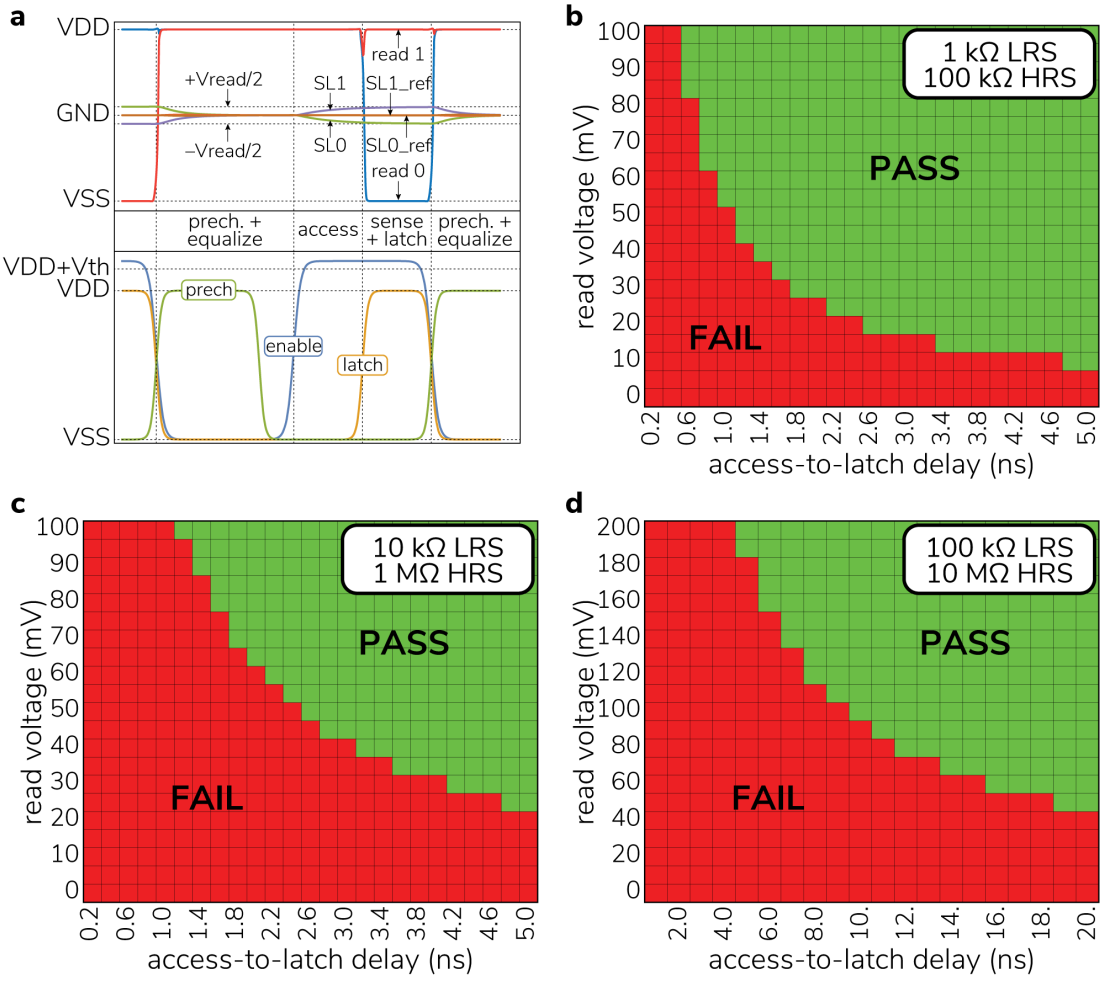
The objective of Experiment E4 is to evaluate the multilevel characteristics of an H3 cell. For this experiment, we used another pair of devices (D6A and D6B) with the same material, initialization, and polarity as described in Experiments E1 and E2. We then applied a ramp of pulses from 0.5 V to 2 V, followed by a ramp from –0.5 V to –2 V (both in steps of 20 mV) with interleaved read pulses of 100 mV (integrated for 1 ms) to monitor the state of the device. Supplementary Figures 6a and 6b show the gradual evolution of the state of the device for 40 cycles. Supplementary Figures 6c and 6d show that 16-levels are possible using a simple incremental step pulse programming (ISPP) algorithm [8]. Supplementary Figure 6e and its close-ups 6f, 6g and 6h, show that 256 levels in an H3 cell are achievable using a modified version of the iterative pulse programming algorithm described in [7]. As shown with red in Supplementary Figure 6e, the codes towards the middle of the range are about 3-4 times more conductive than the lower and upper range, since both devices in an H3 cell are more conductive.



Supplementary Figure 6. Multilevel characteristics of an H3 cell. a: State evolution of device D6 for 40 consecutive programming cycles. **b**: Superimposed cycles from **a** showing smooth and repeatable transitions. **c**: A 16-level H3 memory cell can be achieved using a simple incremental step pulse programming (ISPP) approach with a step of 5 mV. **d**: Histogram of 20 writes for each level using the ISPP approach. **e**: In blue, 256 levels can be obtained using a modified version of the iterative pulse programming algorithm described in [7] with a step size of 5 mV. In red, the total device current @ 100 mV (between electrodes B1 and B2). **f**, **g**, and **h**: Close-up of the lower, middle and upper range, respectively, of the ranges highlighted in **e** with green boxes. A red line is included as a visual guide.

Supplementary Note 7: Estimation of access-to-latch delay

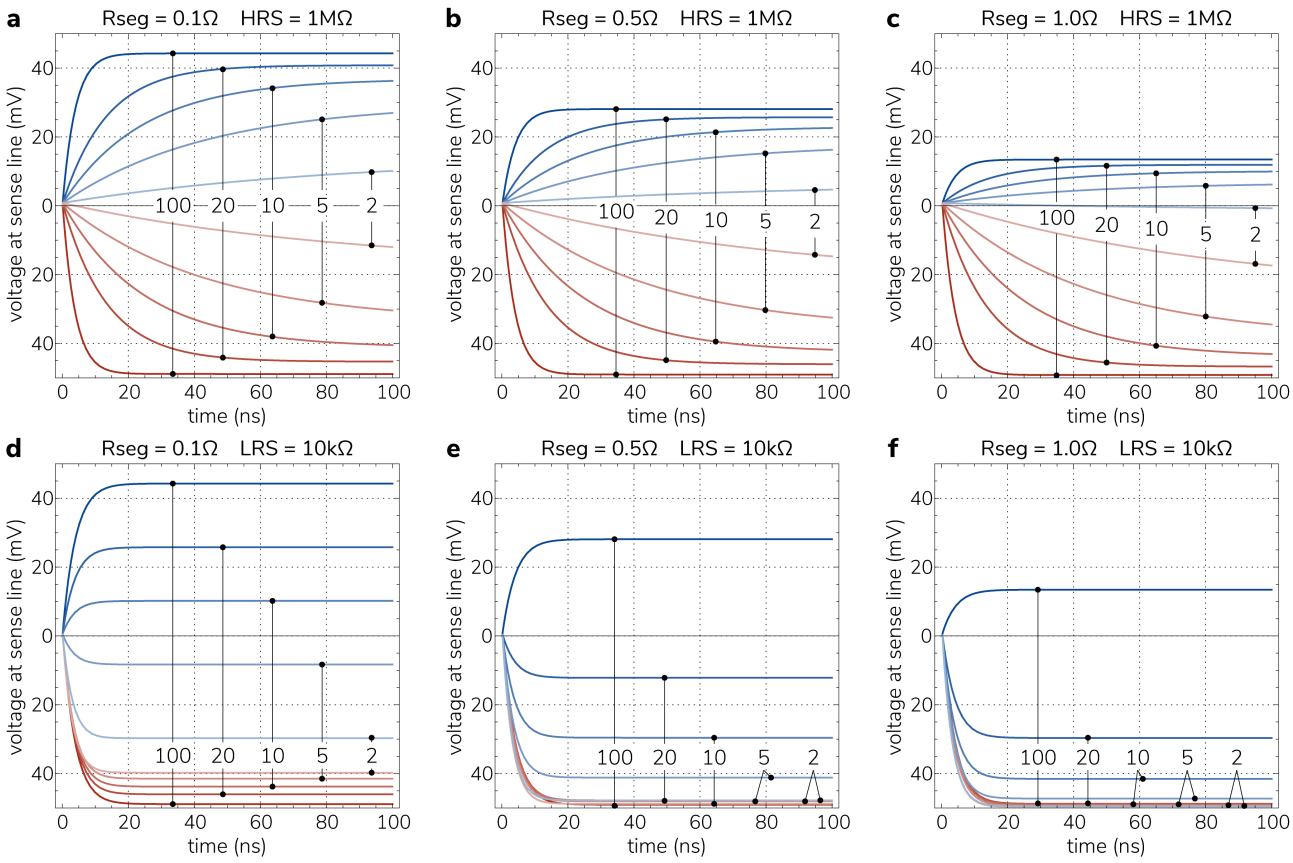
The read operation of an H3 cell in a memory array is limited by the speed of the CMOS read circuitry, but mainly by the time it takes the memristor in LRS state (either the left or right memristor) in an H3 cell to charge its sense line, thus the critical delay in a read operation will be given by the delay between the time the mFET is enabled and time the voltage is latched by a voltage comparator at the end of the sense line, i.e., the *access-to-latch delay*. The time diagram of a typical voltage-based read operation in a 1 Mb (1024x1024) array is shown in Supplementary Figure 7a. A read operation starts by precharging the sense lines to half of the maximum voltage, and by applying a small read voltage V_R using a V/2 biasing scheme through the word and bit lines. The mFET is then enabled which pulls the line either to $+V_R/2$ or $-V_R/2$, which is finally latched by the voltage comparator. Note that the left and right memristors never experience a voltage drop across them larger than V_R (not even temporary) which is not disturbing. Supplementary Figures 7b through 7d show the SPICE-simulated shmoo plots on a 130-nm technology node as a function of the read voltage and access-to-latch delay for various LRS and HRS values, but all with an HRS/LRS ratio of 100. We found that for a memristor with a LRS of 10 kΩ or less, we can obtain random-access read latencies of a few nanoseconds.



Supplementary Figure 7. Access-to-latch delay estimation on a 1 Mb (1024x1024) array of H3 cells on a 130-nm node. **a**, Timing diagram and control signals of a read operation. **b** through **d**, SPICE-simulated shmoo plot as a function of the read voltage and the time delay between the moment the mFET being activated (access) and the moment the developed signals being latched by the voltage comparator, under different LRS and HRS resistances.

Supplementary Note 8: Effect of HRS/LRS ratio and wire resistance on the SL voltage swing

Supplementary Figure 8 shows the SPICE-simulated voltage swing on the sense line (SL) in a 1024x1024 (1Mb) array on a 130-nm node when reading the farthest cell from the peripheral circuitry, as a function of the HRS/LRS resistance ratio and the FET and ReRAM wire resistances, for a read voltage V_{read} = 100 mV. We modelled the FET and ReRAM wire resistances as the resistance per memory cell R_{seg}, such that a row (or column) of X memory cells effectively presents a resistance of X*R_{seg}. In blue tones, we show the SL voltage when reading a logic '1', and in red tones for logic '0'. The values for R_{seg} are indicated on top of each plot. For Supplementary Figures 8a, 8b and 8c, the HRS was fixed to 1 MΩ, and the LRS was swept from 10 kΩ to 500 kΩ. For Supplementary Figures 8d, 8e and 8f, the LRS was fixed to 10kΩ and the HRS was swept from 20 kΩ to 1 MΩ. The numbers inside each plot indicate the HRS/LRS resistance ratio in each case. In general, the voltage swing (the voltage difference between a red and blue line for a given HRS/LRS ratio) is larger for larger HRS/LRS resistance ratios. In Supplementary Figures 8a, 8b and 8c, the total leakage current as seen by the selected word line (WL) and bit line (BL) is approximately constant (as it is mainly determined by the HRS, which is fixed at 1 MΩ), and thus the voltage swing is less sensitive to R_{seg}. In contrast, for Supplementary Figures 8d, 8e, and 8f, the total leakage current increases for lower HRS/LRS resistance ratios, and thus the voltage swing is more sensitive to R_{seg}. The reason is that for lower total series resistances (HRS+LRS) in an H3 cell, the leakage increases and thus the voltage drop across the ReRAM and FET lines also increases, decreasing the voltage swing at the SL (e.g. it is practically null if R_{seg} = 1 Ω and HRS/LRS < 10). Also note that, in all cases, the logic '0' configuration (LRS|HRS) is less sensitive to changes in R_{seg}. This is because the WL (connected to the left device that is in LRS) is only in charge of charging the SL of the line we are reading from, whereas the BL (which is where V_{read} is applied) sees 1024 leak paths (i.e. a total current of 1024*V_{read}/(HRS+LRS)). As a general rule, LRS should be close to the ON resistance of the mFET, and HRS should be as high as possible to reduce leakage.



Supplementary Figure 8. Effect of HRS/LRS ratio and wire resistance on voltage swing of the sense line. The values of R_{seg} and HRS or LRS are indicated on top of each subfigure. The numbers inside each plot indicate the HRS/LRS resistance ratio for each simulated case.

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