
Supplementary information

A cryogenic CMOS chip for generating control signals for multiple qubits

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Supplementary Material for A cryogenic CMOS chip for generating control signals for multiple qubits

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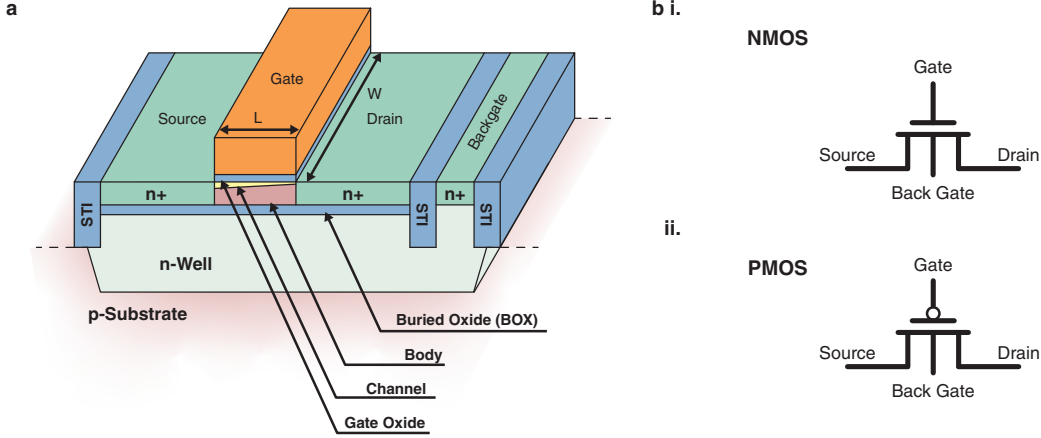


FIG. S1. **28nm FDSOI process.** **a** Cross-section of an NMOS device. A PMOS transistor is fabricated on similar layer stack but with p-doped drain, source and backgate region. Width, W and Length, L of the device is denoted in the diagram. STI stands for Shallow Trench Isolation, separating the various n or p- doped areas. The inversion channel (yellow) underneath the gate when transistor is on is also shown. **b** Circuit symbol for NMOS and PMOS devices with corresponding electrical terminals.

I. CRYOGENIC CMOS IMPLEMENTATION DETAILS

The circuit is designed on a 28 nm Fully Depleted Silicon-On-Insulator (FDSOI) process with 8 metal layers. The core transistors are fabricated on a Silicon-Insulator-Silicon layer stack in a p-type substrate, as shown in Fig. S1. Source and drain regions for a transistor are formed with n- or p-type doping in a 7 nm thick silicon body. A polysilicon gate structure is etched on top of a 1.3 nm HfO_2 dielectric layer between the source and drain. A 22 nm thick buried oxide layer isolates the body of the transistor from the underlying layers. An n-type layer beneath the buried oxide forms the backgate terminal for NMOS, whereas the p-type backgate for PMOS transistors is situated within an n-well. The SOI structure isolates the transistors from the substrate and reduces parasitic capacitance significantly, thus providing superior speed and power performance compared to a standard bulk CMOS process. The core transistors, used for logic, including the FSM, oscillator and memory, within the chip are rated for 1 V operation, however the process also provides a family of transistors with thicker gate oxide and larger feature sizes compatible with 1.8 V operation which are used for the CLFG cells to allow an extended operating range.

The surface charge potential of the silicon body between the drain and source region can be modulated by applying a voltage on the gate terminal. The NMOS transistor is off when the gate potential with respect to source or body (V_{GS}) is less than or equal to zero. When in the off state, the transistor exhibits a large resistance between its drain and source. Only a small leakage current flows between the two nodes, the source of which is attributed to the subthreshold current. On the other hand, the transistor is on when V_{GS} exceeds a threshold level, V_{th} and a channel of minority carriers – called the inversion channel – is formed in the body region underneath the gate connecting the drain and source. Current can flow from drain to source if $V_{DS} > 0$. The leakage and the value of V_{th} can be tuned using the backgate, which is formed by the n- or p-well that runs under the transistors. The value of this leakage at different temperatures and backgate voltages is shown in Fig. S2.

Stacking up combinations of both n and p type transistors for complementary switching enables building low power, high speed complex digital logic gates. As described above, the charge transport through MOS transistors when on is governed by drift current as opposed to diffusion current in Bipolar Junction Transistor (BJT), which renders conventional BJTs unusable at temperatures below carrier freezeout. The effective free carrier concentration in the body drops rapidly as temperature is lowered but the formation of an inversion channel in a MOS transistor is still possible at the cost of higher V_{th} as the temperature decreases. Furthermore, access to a backgate in this process provides a secondary control to circumvent the effect of V_{th} increase at low operating temperature and is particularly advantageous for cryogenic applications.

A. Charge-Lock Fast-Gate Cells

With respect to the Charge-Lock Fast-Gate (CLFG) circuitry described in the main article, the key performance parameters for a MOS transistor as a switch are the leakage current, on-resistance, and input-output voltage swing. Leakage directly determines the charge retention efficacy for the CLFG cells. For a given held voltage over time, the value of the $C_{PULSE,N}$ in the CLFG cells (see Fig. 2b) can be smaller – resulting in area and power savings – if the transistor leakage current is reduced. In addition, idle power cost is set by the total leakage current of the chip, which scales as more circuitry is integrated to interface with many qubits. Leakage decreases exponentially with lowering temperature.

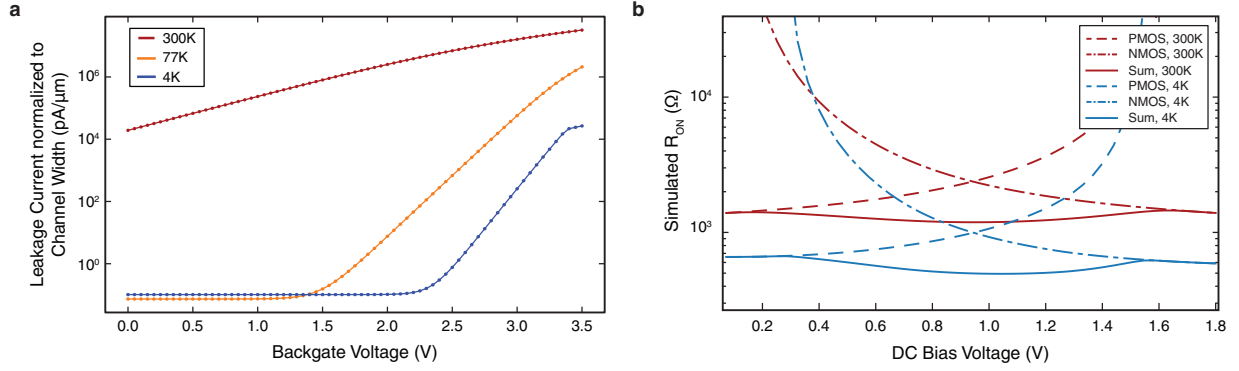


FIG. S2. **Performance of MOS transistor as a switch at cryogenic temperature.** **a** Measured leakage current at 3 different temperatures through an NMOS transistor when off. **b** Simulated on-state resistance, R_{ON} for an NMOS transistor, a PMOS transistor and a transmission-gate switch (formed by placing an NMOS and PMOS transistor in parallel) at 300 K (red) and 4 K (blue). The x-axis shows bias voltage V_{DC} , with the applied voltage on the drain and source node set to $V_{DC} + 10$ mV and $V_{DC} - 10$ mV respectively.

Furthermore, $\frac{k_B T}{C_{PULSE,N}}$ noise is inherently lower, where k_B and T stands for Boltzmann's constant and temperature respectively. Cryogenic operation of CLFG cells can leverage these advantages to retain the charge-locked potential at the gate of quantum devices with better accuracy for longer. Fig. S2a shows that an NMOS transistor in this process exhibits more than 4 orders of reduction in leakage current when measured at 4 K compared to its normal room temperature operation.

Referring to Fig. 2b in the main article, the on-resistance of the fast-gating switches (controlled by the $G_{FG,N}$ signal) and $\frac{C_{PULSE,N} \times C_{P,N}}{C_{PULSE,N} + C_{P,N}}$ forms an RC time constant limiting the rise/fall time of the control signal. A lower on-resistance is desirable to attain faster rise/fall time for the pulses generated on qubit gates. $C_{PULSE,N}$ is implemented as an on-chip Metal-Oxide-Metal (MOM) capacitor of value 5.6 pF. The switches are implemented using a pair of NMOS and PMOS transistors of length 0.15 μm and width 0.32 μm and 0.96 μm respectively in parallel, known as Transmission Gate (TG) switch. The on-resistance of the transistor can be modelled as,

$$R_{on} = \frac{L}{\mu C_{ox} W (V_{GS} - V_{th})} \quad (S1)$$

Where μ is the carrier mobility, C_{ox} is the gate capacitance per unit area and W , L are width

and length of the transistor respectively. Note, the above equation holds for small $V_{GS} - V_{th} \gg V_{DS}$, which is the case when the transistor is employed as a switch and V_{GS} is driven with a positive power supply. The well-established foundry provided room temperature models do not hold when the transistors are operated at deep cryogenic temperature and, notwithstanding a valid low temperature simulation model for the devices, high performance circuit design becomes prohibitively challenging. We have carefully measured and analysed the transistor characteristics at different temperatures and developed a cryo-CMOS model for our application. Detailed analysis of the low temperature behaviour of transistors is a complex endeavour and outside the scope of this paper. However, it is worth pointing out the two primary artefacts of low temperature operation that directly impacts the transistor's performance as a switch is the increase of V_{th} and μ with cooling. The former is attributed to exponential reduction of effective carrier density resulting in increased Fermi potential in silicon, and the latter is due to reduced phonon scattering as temperature is lowered. The amount of increase in μ and V_{th} depends on the specifics of the fabrication process parameters. As described by S1, increased μ and V_{th} determines the resultant R_{on} at low temperature. Fig. S2(b) shows the simulation results of small signal R_{on} as a function of drain-source for two temperatures. $R_{ON,TG}$ provides lower on-resistance across the entire power supply range between 0 V and 1.8 V as compared to a single NMOS or PMOS device. In addition we expect R_{ON} to be approximately halved when temperature is reduced from 300 K to 4 K, resulting in sharper rise and fall transitions on fast-gating pulses at 4 K.

B. Oscillator

The oscillator circuit generates master clock for the FSM. We have chosen the ring oscillator implementation where an odd number of inverter gates are connected in a feedback loop to produce a free running clock. Fig. S3 shows the circuit block diagram. The tradeoff between power and delay is of paramount importance at mK operation, which is governed by the on-resistance (see eq. S1 and intrinsic capacitance (WLC_{ox}) of the transistors, number of inverter stages and also the power supply voltage. We have extensively measured and characterized the performance of individual transistors and logic gates fabricated in this process at temperatures between 300 K and 4 K. Our choice of oscillator topology in conjunction with our proprietary simulation models and database of low temperature measurement re-

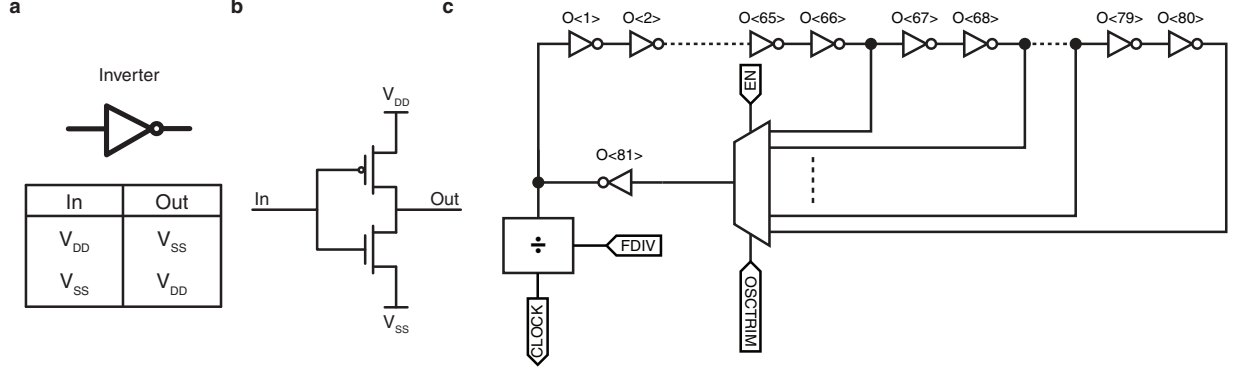


FIG. S3. **Oscillator circuit block diagram.** **a** Inverter logic gate and its truth table. V_{DD} and V_{SS} are the highest and lowest power supply for the chip respectively. **b** Schematic of the inverter with PMOS and NMOS transistor. **c** Ring oscillator circuit for on chip clock generation. 81 custom inverters are connected in series. The output of each stage is denoted by $O < i >$ with $i = 1$ to 81. The tap-off point for the feedback – and therefore the output oscillation frequency – is controlled by the three-bit OSCTRIM. The output clock frequency is further divided by an integer between 1 to 255, set by the eight-bit FDIV, before passing onto FSM. The block is deactivated when $EN = 0$. Inset shows implementation of an inverter gate with NMOS and PMOS transistors.

sults enable us to design the circuit with predictable performance at cryogenic temperature. We have carefully sized the core devices of the oscillator block and also selectively grouped their back-gates for the purpose of optimising the power-delay performance at its intended operating temperature for a range of V_{DD} .

As shown in Fig. S3, the outputs from the 66th to the 80th stage (in increment of 2) are multiplexed and the OSCTRIM setting is used to determine which of these 8 outputs are fed back to the input of the first stage to form the ring. Thus, OSCTRIM provides a simple 3 bit trimming for the output frequency. The block also includes a divider circuit, and the frequency of the ring oscillator can be further divided down by FDIV, a value between 1 to 255. OSCTRIM and FDIV are static registers which the user can configure through the Serial Peripheral Interface (SPI).

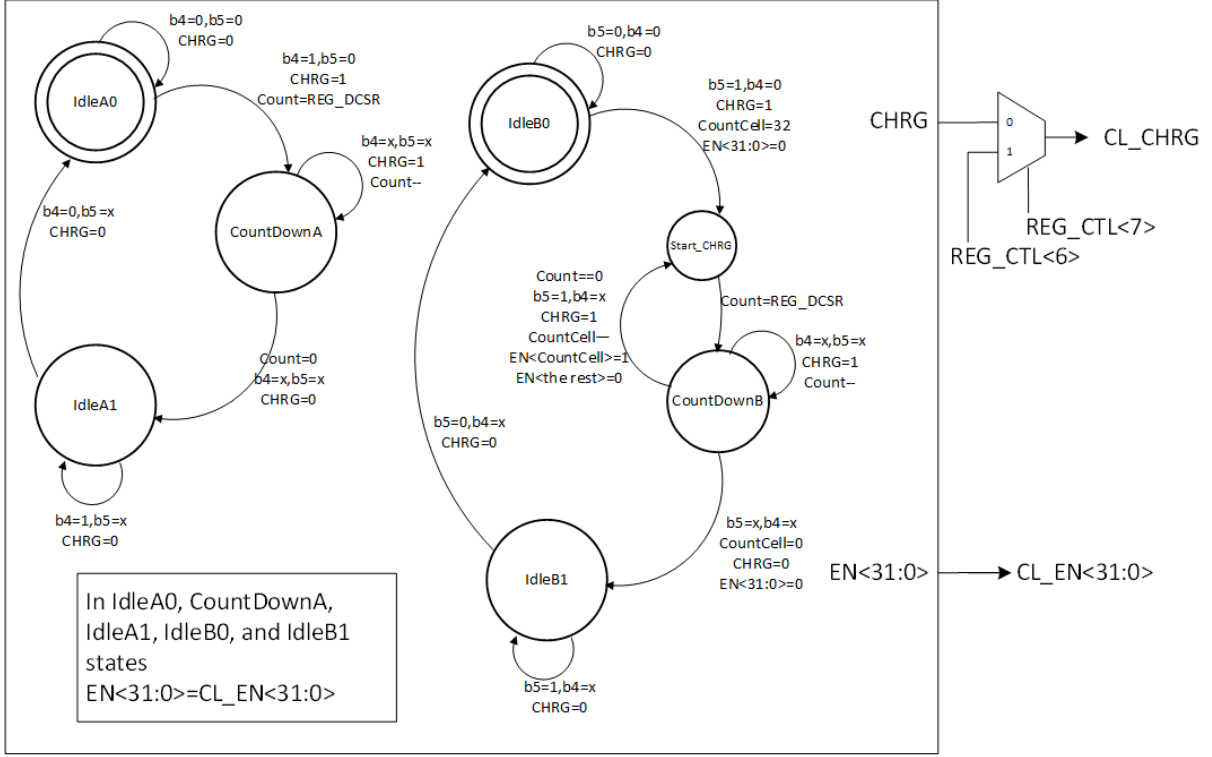


FIG. S4. DC Charge Locking FSM flow diagram

C. Finite State Machine

A Finite State Machine (FSM) is responsible for controlling periodic charge locking and sequencing the fast-gating action according to the preloaded bit pattern in the 128-bit memory. The operating mode of the FSM is controlled by a 32-bit register, REG_CTL which is configured through the SPI interface. In addition, another 32-bit register, CL_EN , dictates which CLFG cells are available to be controlled by the FSM. The diagram in Fig. S4 is a graphical description of the FSM responsible for DC charging of the CLFG cells. "b5" and "b4" refer to bits 5 and 4 of the REG_CTL register; these two bits determine which of the two flows (FSM A or FSM B) are in action. The state-transition diagram on the left (FSM A) describes concurrent DC charging – only the CLFG cells enabled according to their corresponding bits set to 1 in CL_EN register will be charged. The diagram on the right (FSM B) describes sequential DC charging on all 32 CLFG cells, regardless of the value of the CL_EN register.

The DC charging action of FSM A consists of three steps – set $CL_CHRG = 1$, wait for

number of a clock cycles set by the REG_{DCSR} register, then update $\text{CL}_{\text{CHRG}} = 0$. These steps are directly followed in FSM A. Note, within each of the CLFG cells the CL_{CHRG} signal is masked by the corresponding bit in the CL_{EN} register. Therefore even though the global CL_{CHRG} may be one, DC charging takes place only for the CLFG cells which are enabled in the CL_{EN} register.

The steps for sequential DC charging of all 32 cells in FSM B are:

1. Set $n = 32$
2. Set the n^{th} bit of $\text{CL}_{\text{EN}} = 1$, and $\text{CL}_{\text{CHRG}} = 1$.
3. Count REG_{DCSR} clock cycles.
4. Set the n^{th} bit of $\text{CL}_{\text{EN}} = 0$, decrement and decrement n .
5. Repeat (2)-(4) until $n = 0$.
6. Set $\text{CL}_{\text{CHRG}} = 0$.

The FSM then enters the idle state (*IdleB0*, *IdleB1*).
