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Supplementary information

Radiofrequency transistors based on aligned carbon nanotube arrays

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Supplementary Information

Aligned carbon nanotube arrays-based transistors operating in terahertz regime

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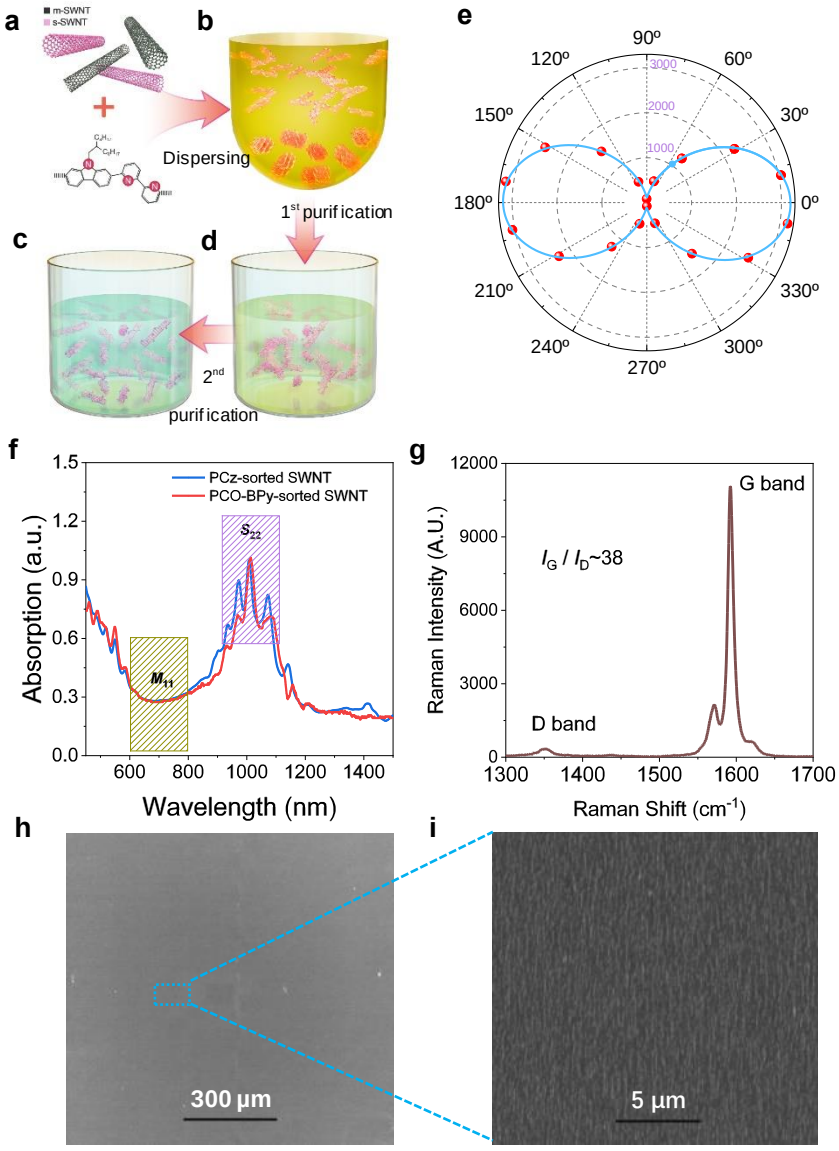
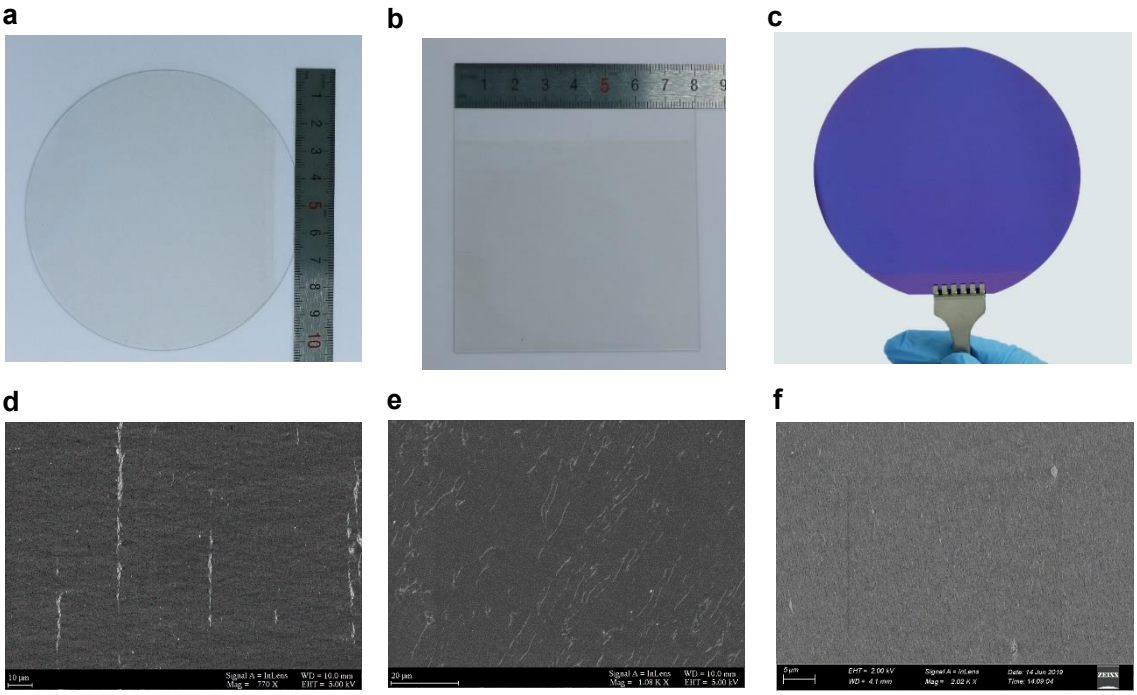
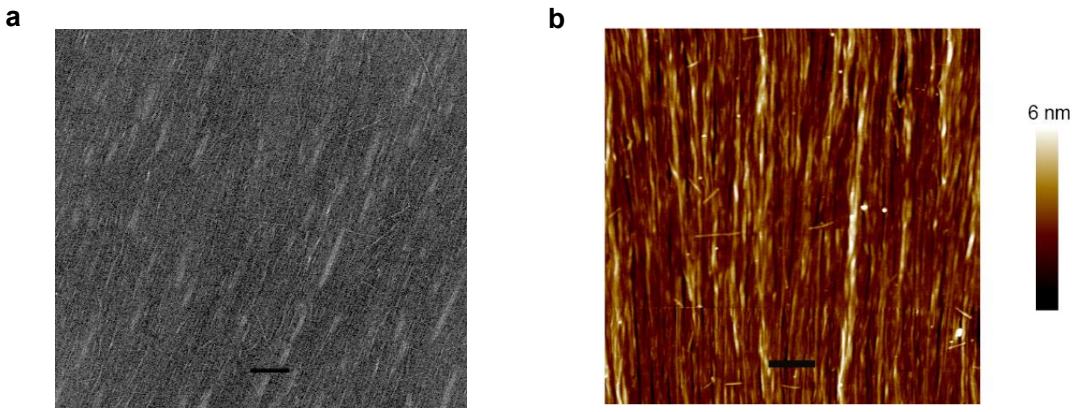


Supplementary Figure 1 | Double dispersion process and characterization of ultrahigh semiconducting purity CNTs. a-d, CNT dispersing and re-dispersing process using conjugated polymer PCO-BPy molecules and 2 separate organic solvents [toluene solvent as shown in (**b**,**c**) and 3-chlorotoluene as shown in (**d**)]. The mixture of CNTs and PCO-BPy molecules are first dispersed in toluene solvent. The residuals from the solvent are re-dispersed in target 3-chlorotoluene solvent to create ideal monodispersed CNTs with ultrahigh semiconducting purity followed by a filtration process and THF rinsing process. **e**, Polarized Raman spectrums of CNTs with different incident angle Θ and their Raman intensity *I* and fitting curve in polar coordinates. Raman intensity (*I*) of G-band peak (Red dots) versus polarization angle Θ in polar coordinates can be described by a cos2Θ function (fitted curve in blue line). The ratio of max Raman intensity (I_{max}) and minimum Raman intensity (I_{min}) is 40. **f**, Comparison of absorbance spectrums of PCz-sorted and PCO-BPy-sorted SWNTs after 2rd dispersion, indicating that PCO-BPy-sorted CNTs should have similar semiconducting purity as that of PCz-sorted CNTs[13]. **g**, Raman spectrum of as-deposited aligned

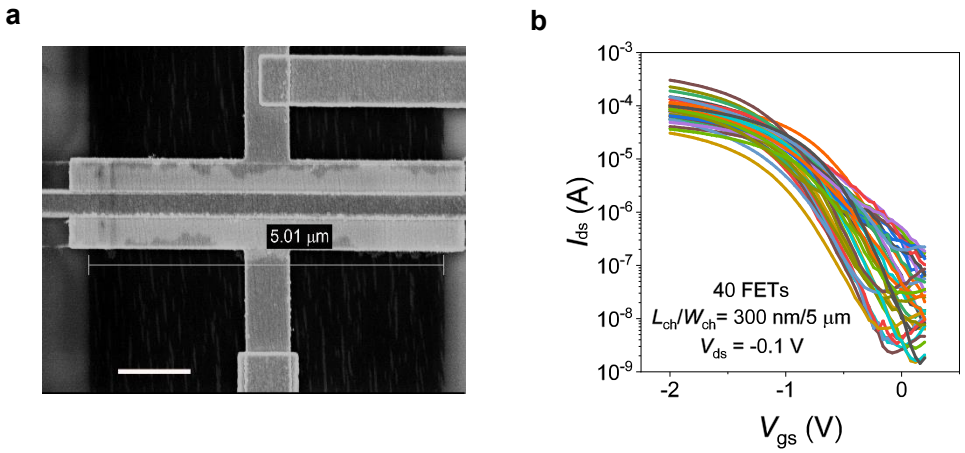
CNT arrays (along CNT oriented direction). G-band/D-band peak ratio as high as 38 reflects the good quality and little defect of our aligned CNT arrays. **h**,**i**, SEM images of as-deposited CNT arrays on a silicon substrate with different magnifications. The scale bars are 300 μm (**h**) and 5 μm (**i**), respectively.



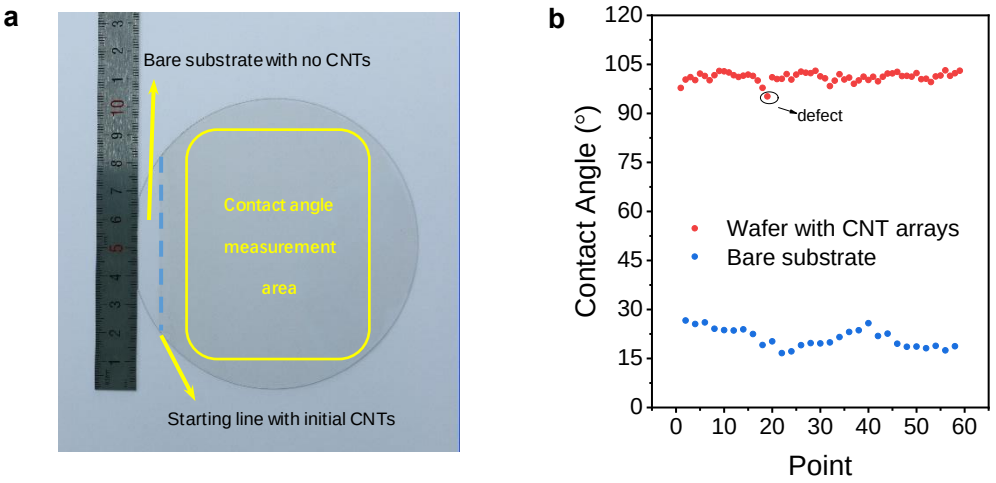
Supplementary Figure 2 | Characterization of CNT arrays prepared using BLIS procedure on different substrates. a-c, Optical images of quartz (**a**), glass (**b**) and silicon wafer (**c**), respectively, with full CNT array coverage. **d-f**, Corresponding SEM images of CNT arrays on quartz (**d**), glass (**e**) and silicon wafer (**f**), respectively. These SEM images reveal that BLIS procedure is applicable for a range of different kinds of substrates.



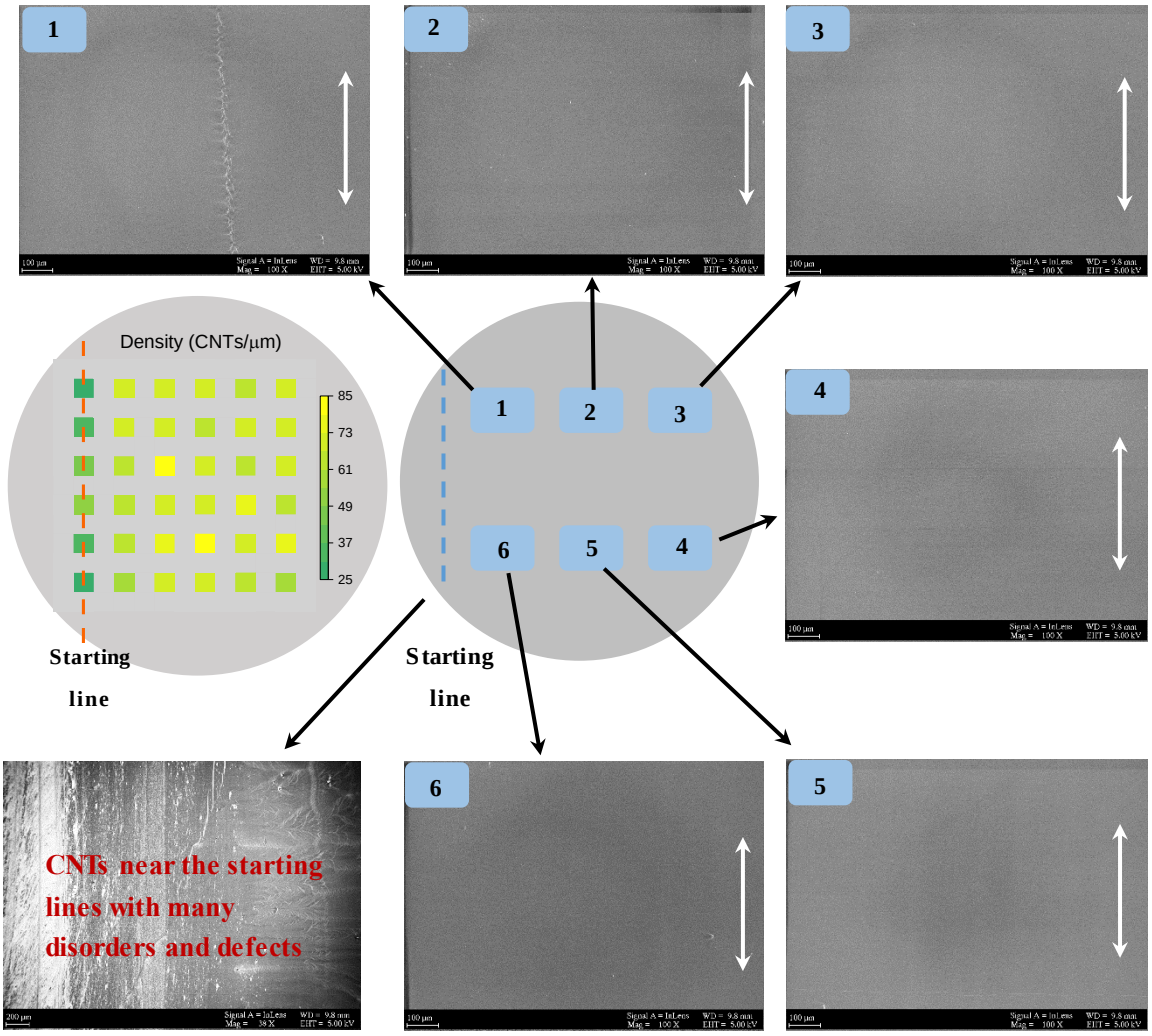
Supplementary Figure 3 | Characteristics of CNT arrays on quartz substrate. a, SEM image of as-deposited CNT arrays on quartz substrate prepared using BLIS procedure. The CNT density is approximately 70 CNTs/μm. Scale bar, 200 nm. **b**, AFM image of as-deposited CNT arrays on quartz substrate, indicating CNT density of approximately 70 CNTs/μm. Scale bar, 200 nm.



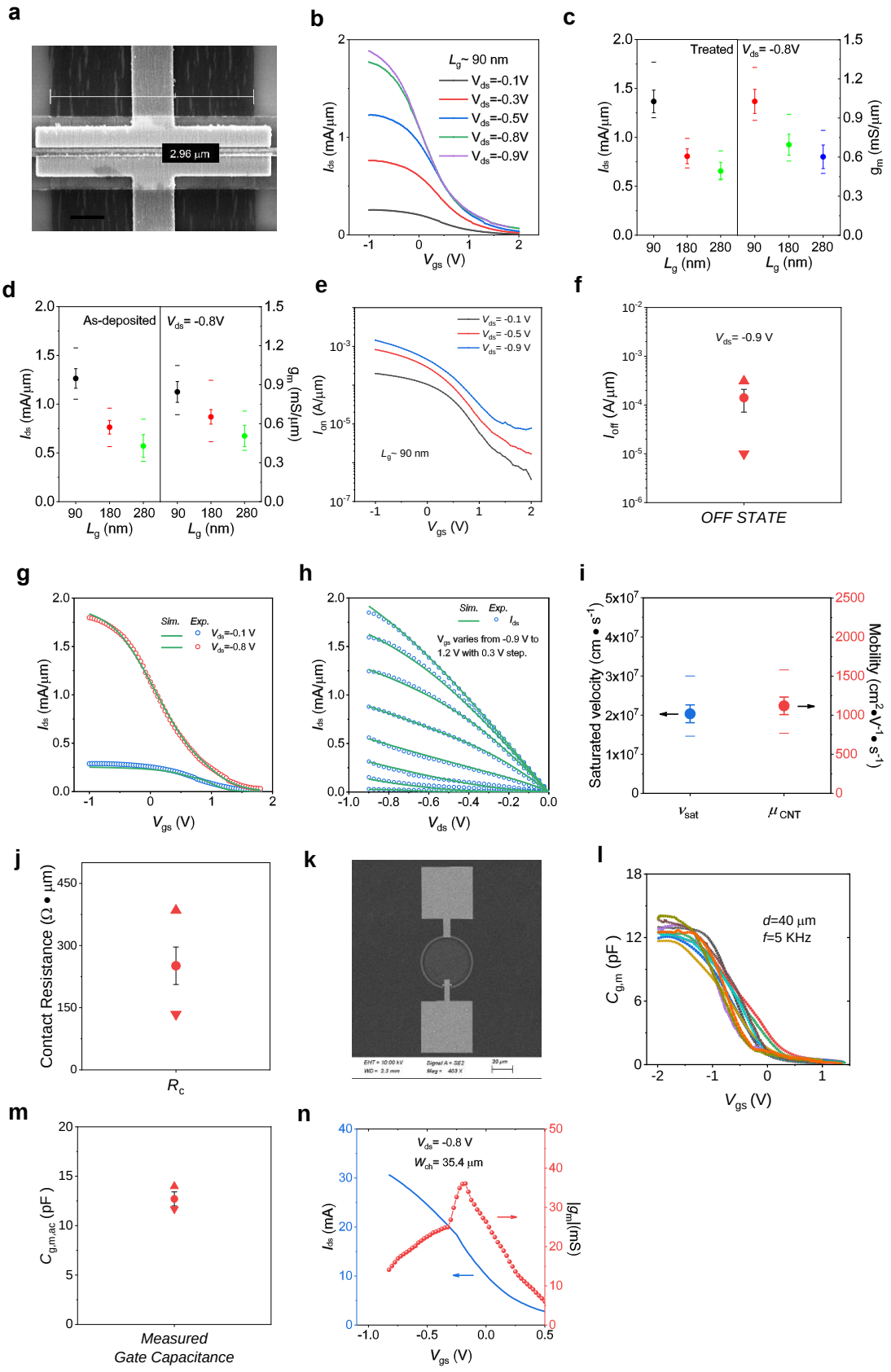
Supplementary Figure 4 | Electrical characterization of s-CNTs purity. a, SEM image showing a typical CNT array-based FET, with L_{ch}/W_{ch}=300 nm/5 μm. Arrays of FETs with identical dimensions are fabricated on the quartz substrate with CNT array density of 70~80 CNTs/μm. Scale bar: 1 μm. **b**, Measured transfer curves of total 40 FETs with V_{ds} of -0.1 V. The existence of any metallic CNT should lead to $I_{off} > 1\ \mu A$ and low on/off ratio of below 100. According to the two criteria, not a single metallic CNT appears in these measured FETs since the lowest current on/off ratio is larger than 100 and none off-state current exceed $1\ \mu A$. We take the CNT density of 70 CNTs/μm and channel width of 4.5 μm as the lower limits, the total number of CNTs is estimated to be at least 12600. From this analysis, the semiconducting CNT purity in this work is better than 99.99%.



Supplementary Figure 5 | Statistical results from contact angle measurements across 4-inch quartz wafer. a, Optical images showing the measurement setup. We exclude the bare substrate area as marked in blue line and the contact angle measurements are performed inside the yellow box area. **b**, Contact angles comparison of measurement data points on the wafer with CNTs (red dots) and bare substrate (blue dots). All the measured angles on wafer with CNTs are higher than 95 degrees and most of them distribute around 100 degrees. Only one point exhibits an exceptional lower value, possibly due to defect in the CNT arrays film. On the contrast, the contact angles at the bare region of the quartz wafer are all below 30 degrees. Therefore, the uniformly distributed contact angles around 100 degrees indicate good uniformity of CNT coverage rate and array density.



Supplementary Figure 6 | SEM images obtained from different regions of CNT arrays in a 4-inch quartz wafer. The starting line represents the initial binary-liquid contact line where the CNTs started to be deposited on the wafer. The area near the boundary usually presents many disorders and defects. While CNT arrays of most other regions away from the starting line present good morphology uniformity (e.g. regions 1-6). Furthermore, we statistically obtained the regional densities across the quartz wafer, which are shown as a wafer map in the left middle panel. Away from the starting line region, the CNT array density distributed typically within 60~80 CNTs/μm across the 4-inch wafer, which manifests the good uniformity of our BLIS-based CNT arrays.



Supplementary Figure 7 | Statistic summary for d.c. performance of CNT array-based transistors with/without pre-treatment (annealing and yttrium oxide coating and de-coating process) on high-resistivity Si/SiO_2 substrates and mobility extraction by VS model. a, SEM

image of the transistor in Fig. 3a. Scale bar: 500 nm. **b**, Transfer curves of the transistor in Fig. 3a. **c**, Box charts of on-state current density (left) and peak transconductance (right) of 45 transistors with pre-treatment at drain-source bias of -0.8 V. **d**, Box charts of on-state current density (left) and peak transconductance (right) of 45 transistors without pre-treatment at drain-source bias of -0.8 V. Comparing **c** and **d** reveals that the pre-treatment results in 10~25% improvement of I_{on} and g_m for our CNT array-based transistors with three different L_gs (90 nm, 180 nm, 280 nm). The smaller margin of d.c. performance improvement after treatment indicates that PCO-BPy with less alkyl chains has a much smaller impact on transistors compared to those based on PCz-sorted CNTs[21,37]. **e**, Typical log-I_d vs V_{gs} curves of CNT array-based transistors. **f**, Box chart of off current for 15 treated transistors (L_g=90 nm). **g**,**h**, Comparison of the simulation results (lines) with measured transfer curves (dots) (**g**) and output curves (dots) (**h**) using virtual source (VS) model for a 90 nm-L_g transistor. Simulation details is described below. **i**, Box chart of mobility of and saturation velocity extracted by the VS model for 45 treated transistors. **j**, Box chart of contact resistance extracted by the VS model for 45 treated transistors. **k**, SEM image for a CNT array-based capacitor. **l**, C-V characterization results for 10 CNT array-based capacitors. **m**, Box charts of measured accumulation capacitance. **n**, V_{gs}-dependent I_{ds} and g_m of a wide CNT array transistor with L_g/W_{ch} = 50 nm/35.4 μm at V_{ds} = -0.8 V.

Calculation of mobility and saturation velocity using the VS model. In the VS model, the drain current can be described by the product of the mobile charge density and the carrier average velocity along the channel. Considering the Gradual channel approximation[64] in the VS, the channel charge density per area is modeled as

$$Q_{xo} = C_{inv}(V_{GSI} + V_{TH})$$
$$C_{g,eff} = C_{ox} \cdot C_q/(C_{ox} + C_q)$$

where $C_{g,eff}$ is the effective gate capacitance, C_{ox} is the gate oxide capacitance of a single CNT FET, C_q is the quantum capacitance of a single CNT in the channel area. For top-gate device geometry, we use the capacitance model proposed by Deng and Wong[65]

$$C_{ox} = \frac{2\pi k_{ox}\varepsilon_0}{\cosh^{-1}\left(\frac{2(r+t_{ox})}{d}\right) + \lambda_0 \ln\left(\frac{2(r+t_{ox})+2d}{3d}\right)}$$

$$\lambda_0 = (k_{ox} - k_{sub})/(k_{ox} + k_{sub}),\ \mathrm{r} = d/2$$

where k_{ox} is the dielectric constant of the gate oxide, t_{ox} is the thickness of the gate oxide, ε_0 is the vacuum permittivity, and d is the diameter of the CNT. Here we take the average diameter of 1.5 nm for d, k_{ox} of 13 for the ALD-grown HfO_2, t_{ox} of 5.4 nm for thickness of gate oxide, k_{sub} of 3.9 for both silicon substrate and quartz substrate. We can calculate C_q based on the non-equilibrium Green's function formalism validated by Lee *et al.* [44]

$$C_q = c_{qa}\sqrt{q \cdot E_g/(k_B T)} + c_{qb}$$

where the coefficients c_{qa} is 0.087 fF/μm, c_{qb} is 0.16 fF/μm, the bandgap E_g is 0.85/d eV (the unit of d is nm), T is the temperature, q is the electron charge, and k_B is Boltzmann's constant. The VS model transport equations consist of two parts[66]. This above formulation is only for single CNT based device. When we consider CNT arrays based device, we cannot extend the formula simply by multiple the single CNT values, like C_{ox} and C_q, by the CNT density p_{cnt} (here 120 CNT/μm) due to the screening effect between CNTs. We have to make some corrections for CNT array's C_{ox}

and C_q, and these have been detailed earlier in ref. [65].

For on-state current of the CNT array-based FET, the drain current in the linear region is given by

$$I_{D,LIN} = C_{g,eff}(V_{GS} - V_{T,LIN})V_{DS}\frac{\mu_{CNT}}{L_g}$$

and in the saturation region is

$$I_{D,SAT} = C_{g,eff}(V_{GS} - V_{T,SAT})\upsilon_{sat}$$

where V_{GS} and V_{DS} are the intrinsic gate and drain voltage versus the source, respectively, μ_{CNT} is the apparent carrier mobility, υ_{sat} is the saturation velocity. $V_{T,LIN}$ and $V_{T,SAT}$ are the threshold voltages in the linear region and saturation region, respectively. The DIBL effect impacts the threshold voltage through

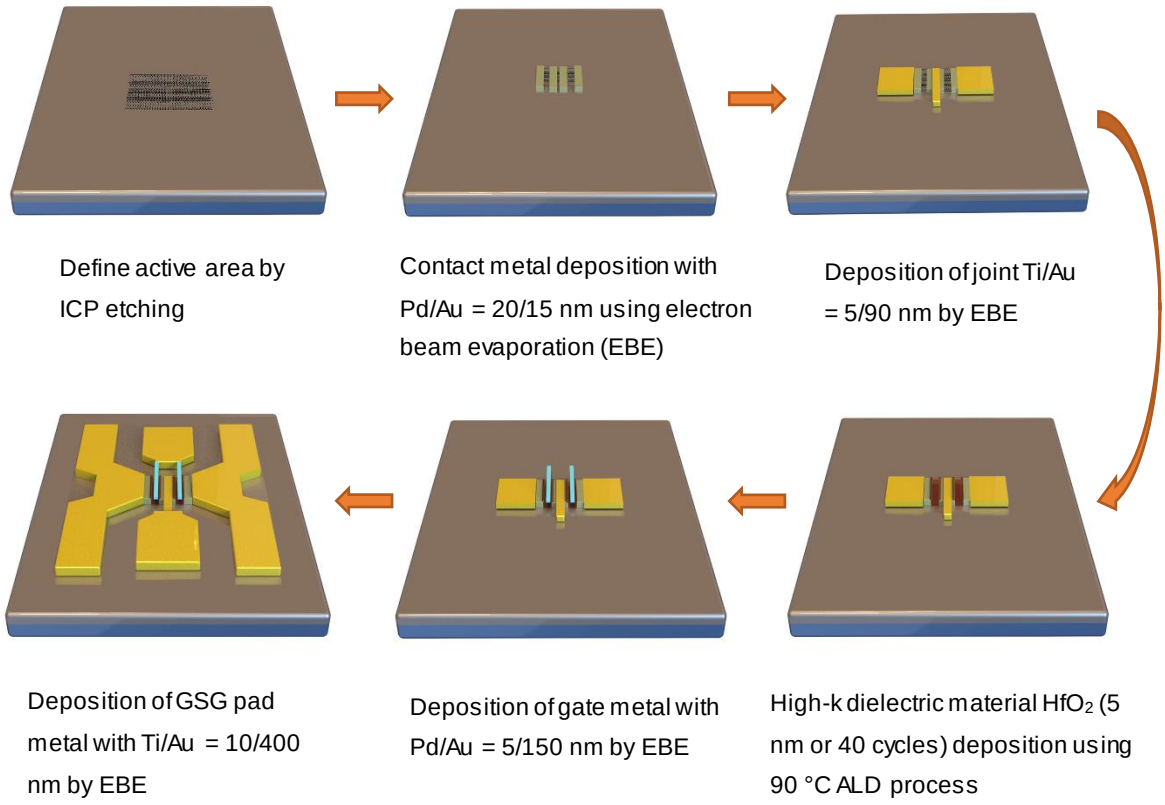
$$V_{T,SAT} = V_{T\mathrm{LIN}} - \delta V_{DS}$$

where δ represents DIBL. The intrinsic bias is calculated by

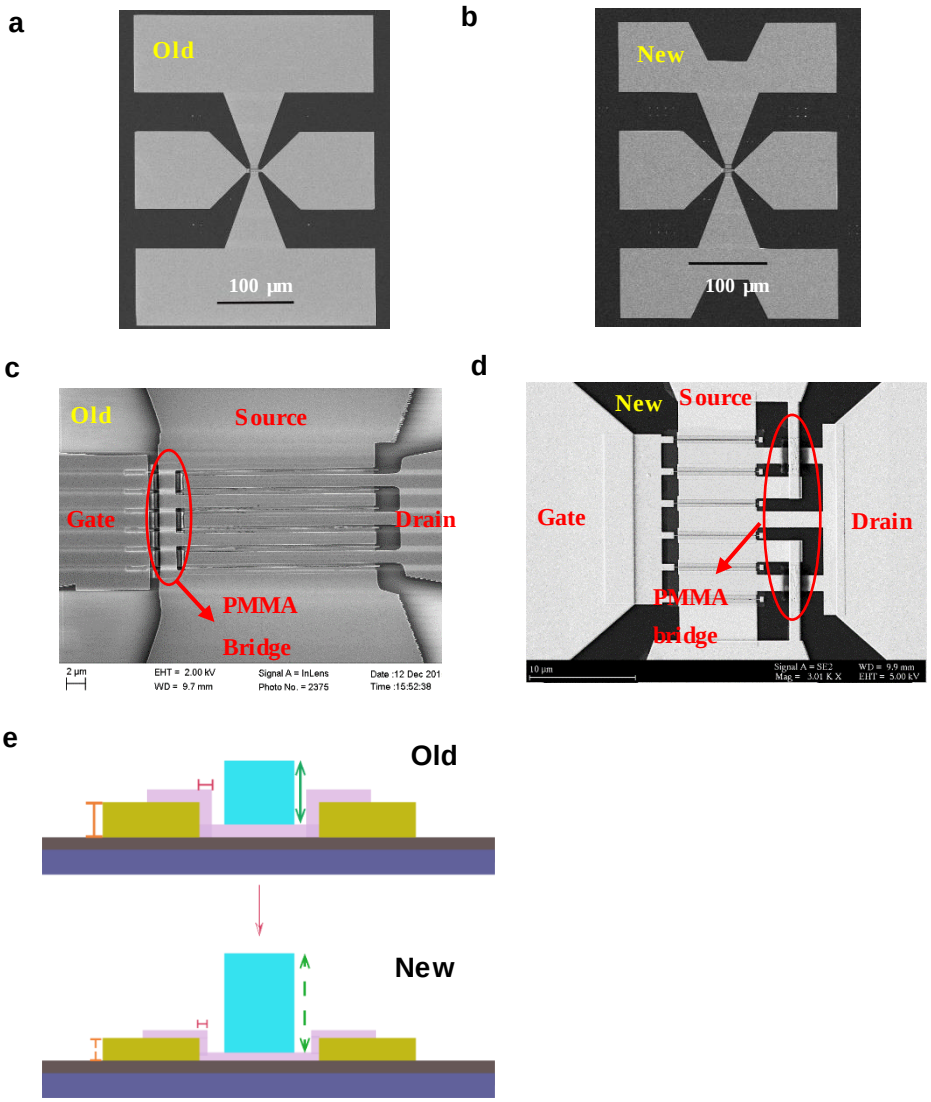
$$V_{GS} = V_{GS,M} - R_S I_{DS,M}$$
$$V_{DS} = V_{DS,M} - 2R_S I_{DS,M}$$

where R_S (R_D) is the S/D contact resistance, $V_{DS,M}$ and $I_{DS,M}$ are the measurement results. Then we can extract the carrier mobility μ_{CNT} and saturation velocity υ_{sat} by fitting *VS model* to transfer and output characteristics of our CNT FETs.

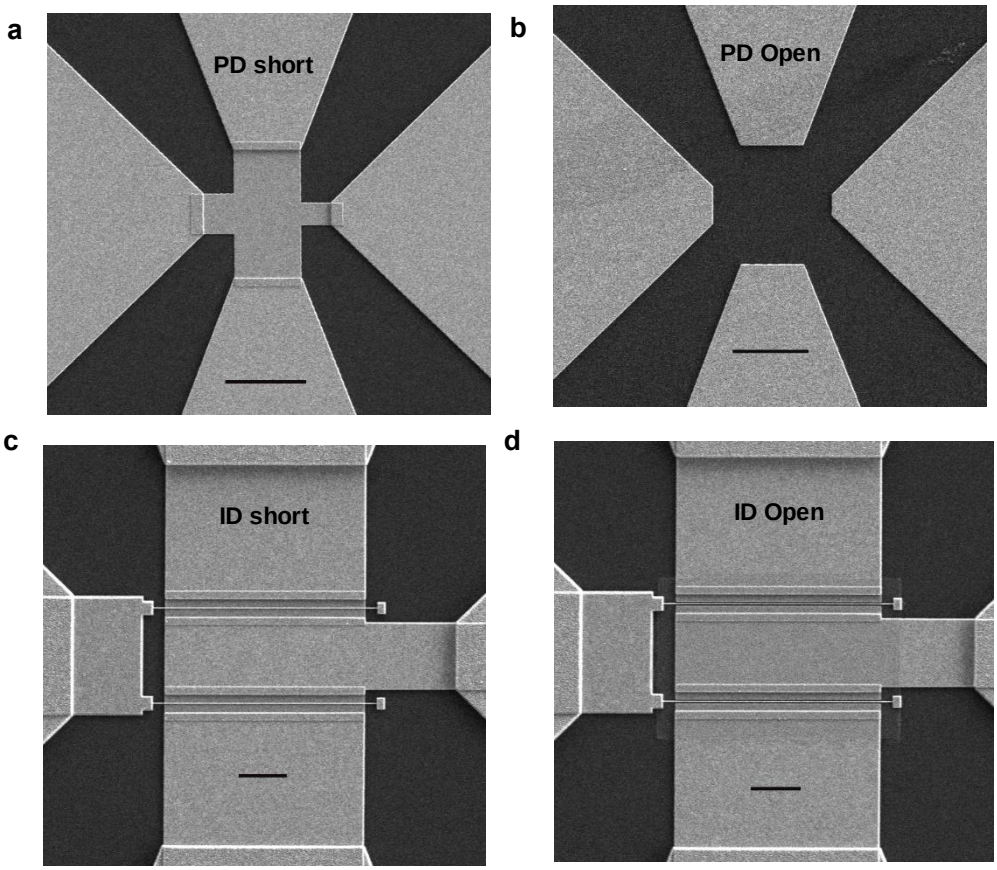
The parameters used in simulating Supplementary Figure 7g-i using the VS model and thus in extracting carrier mobility and saturated velocity are shown in Supplementary Table 2. It should be noted that the contact resistance (Supplementary Figure 7j) does affect device performance especially in such short channel length devices, in which the carrier transport is quasi-ballistic so the contact resistance dominates transistor's performance. Due to the excellent metal/CNT contact, the contact resistance values of our devices are quite low. According to the calculation of the VS model, the contact resistance is as low as 130 Ω•μm (as a result of the high array density and excellent metal/CNT contact achieved here). The statistical results of contact resistance are shown in Supplementary Fig. 7j. As for the gate capacitance, we utilized the C-V MOS structure similar with our previous work[67] and obtained the C-V curves shown in Supplementary Fig. 7l. The CNT films for capacitors were from the same wafer as the devices in Fig.1h to ensure the consistency of the results. ALD-grown HfO_2 layer thickness used is 10 nm, since thinner HfO_2 layer may lead the electric breakdown and leakage due to the large MOS capacitor area. The working voltage range is in accumulation region and so we use measured capacitance under 5 KHz in accumulation region for obtaining real transistor C_g. However, the ALD-grown HfO_2 layer of our transistors is 5.4 nm, which means we should re-calculate C_g for thicker oxide layer. The k value of ALD-grown HfO_2 layer is 13, which is identical to previous work of our group[21,67]. If we utilize the 10 nm HfO_2 thickness, the calculated C_g in the VS model is approximately 1.06×10^{-6} F/cm^2. As shown in Supplementary Figure 7m, we counted all the measured results of the accumulation capacitance values (10 devices). We can see that C_g values vary from 11.9 pF to 14.0 pF, which is very close to the calculation values for the C-V MOS structure (1.06×10^{-6} F/cm^2) in the VS model. The calculated C_g using the VS model can accurately represent the device gate capacitance in our work, and the validity of the extracted carrier mobility and saturated velocity values is thus verified.



Supplementary Figure 8 | Schematic diagram showing the fabrication process of high-speed CNT transistors. See methods for process details.

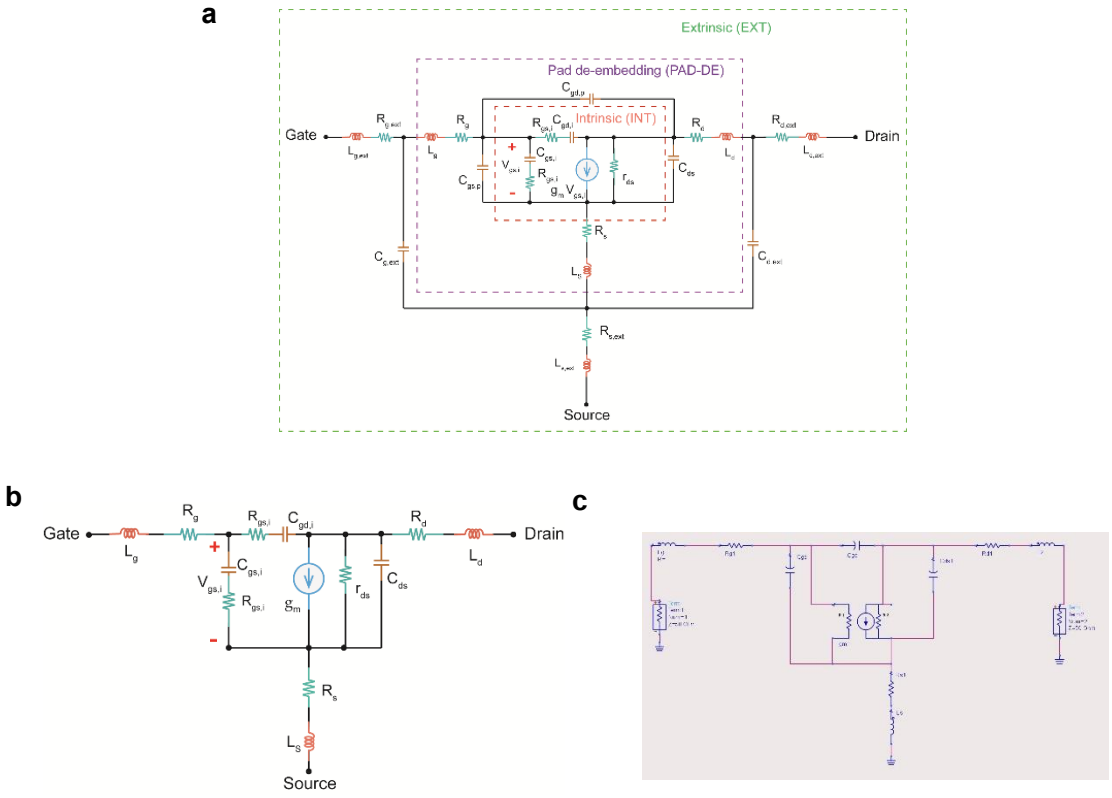


Supplementary Figure 9 | Structure improvement of CNT high-speed FETs. a, SEM image of an earlier design CNT transistor[19] (left) and **b**, present CNT transistor used in this work with GSG pads. The calculated results shows a 16% area reduction. Scale bar, 100 µm. **c,** SEM image of an earlier design CNT transistor (left) and **d**, present CNT transistor used in this work with different bridge structure. The difference between the two structures is the parasitic capacitance values of C_{gs} and C_{ds}. Drain-side bridge structure has lower C_{gs} and higher C_{ds} than gate-side structure. ADS simulation results show that C_{gs} matters more to frequency performance than C_{ds}, which indicates that drain-side bridge structure may perform better by approximately 15% in terms of f_T. Also, the drain-side structure lower the gate resistance by reducing the gate metal length. **e**, Schematic diagram of structure improvement. The green arrow indicates a taller gate metal stack in the new structure to reduce the gate resistance, the red indicatrix shows the thinner dielectric layer to enhance g_m and reduce the parasitic capacitance with smaller effective k value; the orange indicatrix shows the thinner S/D contact metal to reduce the overlap with the gate stack, which can reduce C_{pd} and C_{ps}. However, the use of air-gap will induce long ungated channel regions and thus increase the series resistance, which can be alleviated by the real spacer.



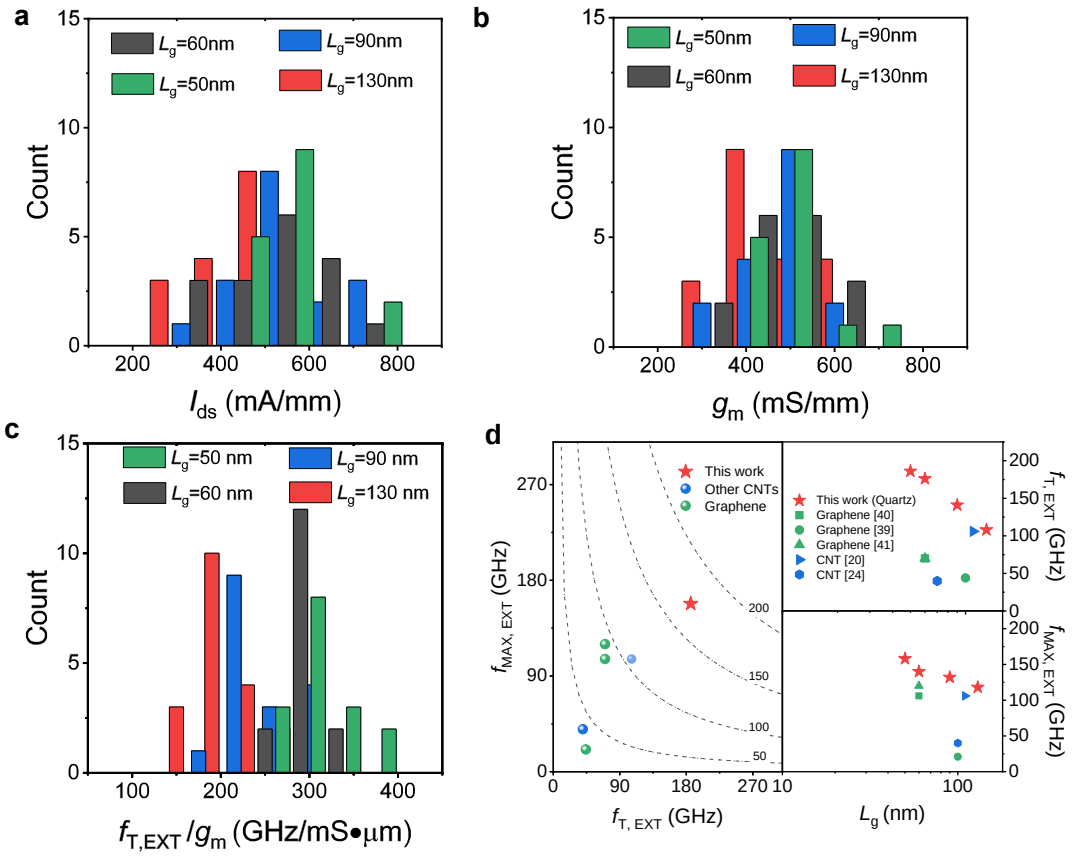
Supplementary Figure 10 | Structures of 'Open' and 'Short' for intrinsic de-embedding (ID) and pad de-embedding (PD). a-d, PD Short /Open and ID Short /Open structures are necessary for extracting pad de-embedding parameters and intrinsic parameters, respectively. PD Short /Open structures are fabricated by using a blank-open square area/ a metallic-short square area to replace the active region. ID Open structure is fabricated by etching the channel-area CNT arrays. ID Short structure is fabricated by shorting the S/D electrode. Etching the channel-area CNT arrays is performed in all structures. Scale bar in (**a**) and (**b**), 10 μm. Scale bar in (**c**) and (**d**), 2 μm.

The PD is usually used in practical application, and the ID is used to reveal the intrinsic potential of the material. The de-embedding schematic is described by an AC small-signal equivalent model, as shown in Supplementary Fig. 11. The open/short structures are precisely identical to the active device to ensure the high fidelity in the de-embedding process. The sweeping frequency is from 100 MHz to 40 GHz with a step of 100 MHz.

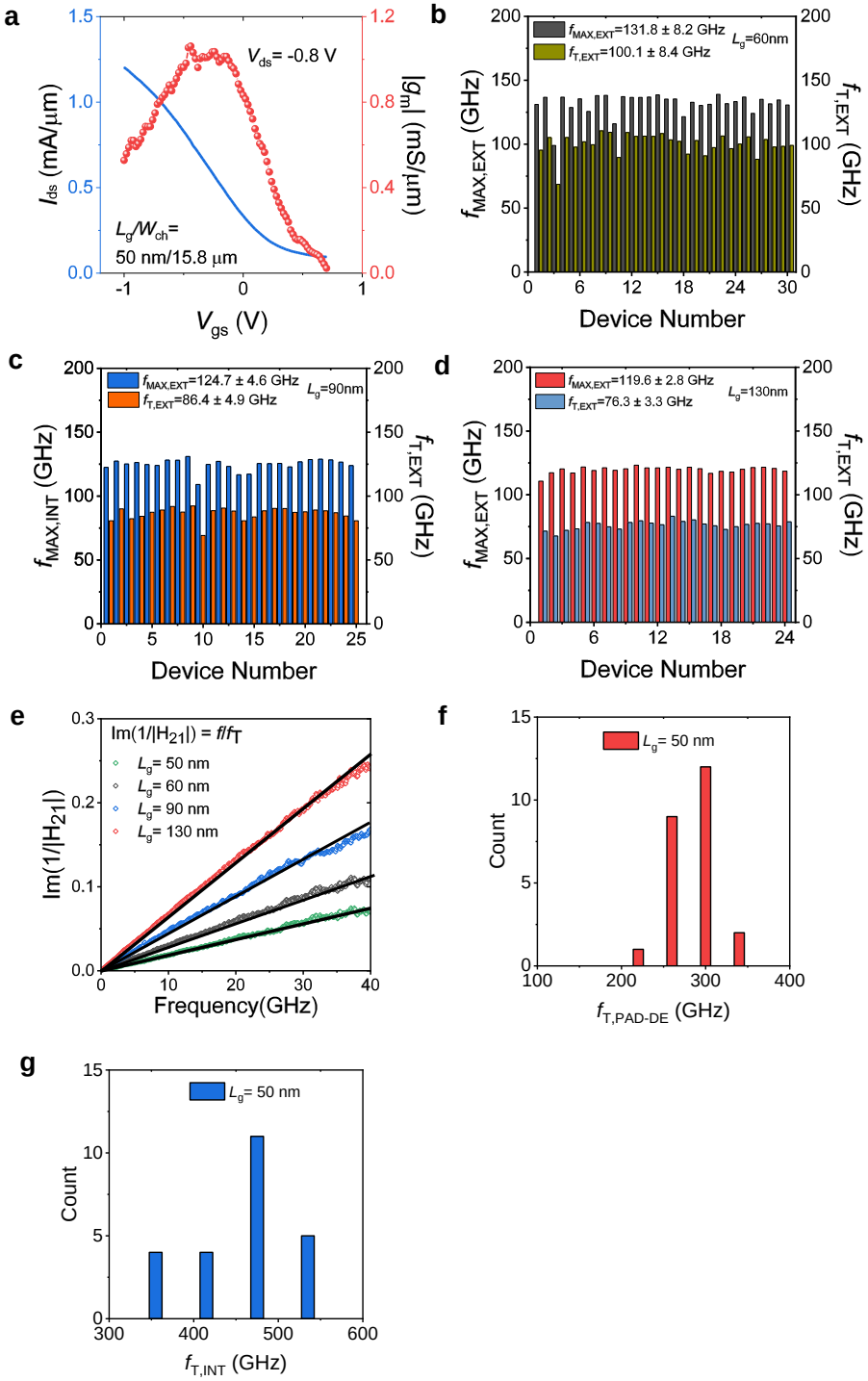


Supplementary Figure 11 | AC equivalent circuit modeling for CNT transistors. a, In the orange pane, intrinsic gate-to-source resistance and capacitance, intrinsic gate-to-drain resistance and capacitance, transconductance, the voltage on $C_{gs,i}$ divided from gate-to-source voltage and drain-to-source output differential resistance are represented by $R_{gs,i}$, $C_{gs,i}$, $R_{gd,i}$, $C_{gd,i}$, g_m, $V_{gs,i}$,and r_{ds}, respectively. In the purple pane, drain serial inductance, source serial inductance, gate serial inductance, parasitic gate-to-source capacitance, parasitic gate-to-drain capacitance, drain-to-source capacitance, source serial resistance, drain serial resistance and gate resistance are represented by L_d, L_s, L_g, $C_{gs,p}$, $C_{gd,p}$, C_{ds}, R_s, R_d and R_g, respectively. In the green pane, all external parasitic (*e.g.* GSG pads and substrate) inductance, resistance and capacitance are represented by $L_{d,ext}$, $L_{s,ext}$, $L_{g,ext}$, $C_{g,ext}$, $C_{d,ext}$, $R_{g,ext}$, $R_{d,ext}$ and $R_{d,ext}$. **b**, The simplified AC small-signal equivalent circuit model (Pad de-embedding part) for CNT transistors. C_{gs} is the sum of $C_{gs,i}$ and $C_{gs,p}$, and C_{gd} is the sum of $C_{gd,i}$ and $C_{gd,p}$. **c**, Small signal equivalent circuit model for the CNT array-based FET using Advanced Design System.

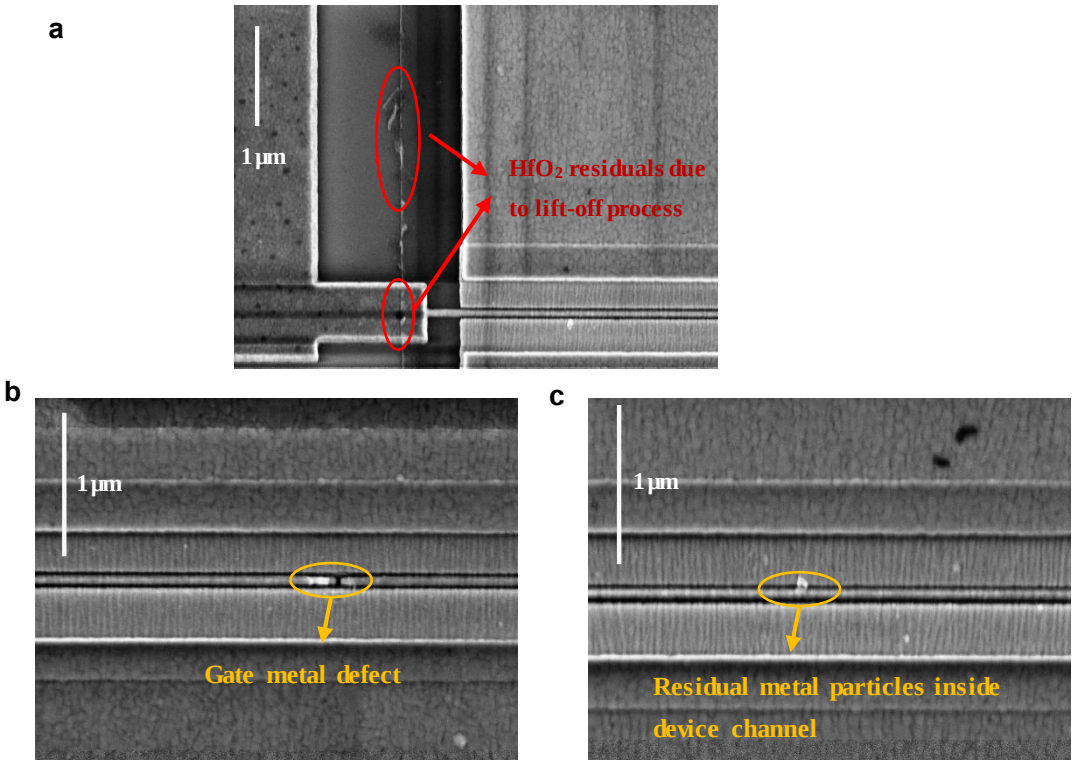
The AC small signal equivalent circuit model in Supplementary Figure 11a contains non-static effects that are usually originated from two points[68,69]. First, the substrate possesses the lossy dielectric property and the substrate effect becomes increasingly important to predict RF performance in high-frequency region. Second, the channel region is distributed in the lateral direction under gate oxide and this may result in the channel propagation delay by RC transmission line effect. The bias-dependent RC distributed channel effects are considered by connecting non-quasi-static channel resistance ($R_{gs,i}$, $R_{gd,i}$) in series with channel capacitances ($C_{gs,i}$, $C_{gd,i}$), respectively. In addition, the high frequency substrate region is modeled by connecting the series substrate resistance to C_{ds}. For the purpose of enhancing the model accuracy, overlap and fringing components ($C_{gs,p}$, $C_{gd,p}$) are separated from channel ones. The parameter of R_g models the effective gate resistance accounting for the distributed transmission line effect. The frequency dispersion of devices can be attributed to the traps at channel/substrate interface.



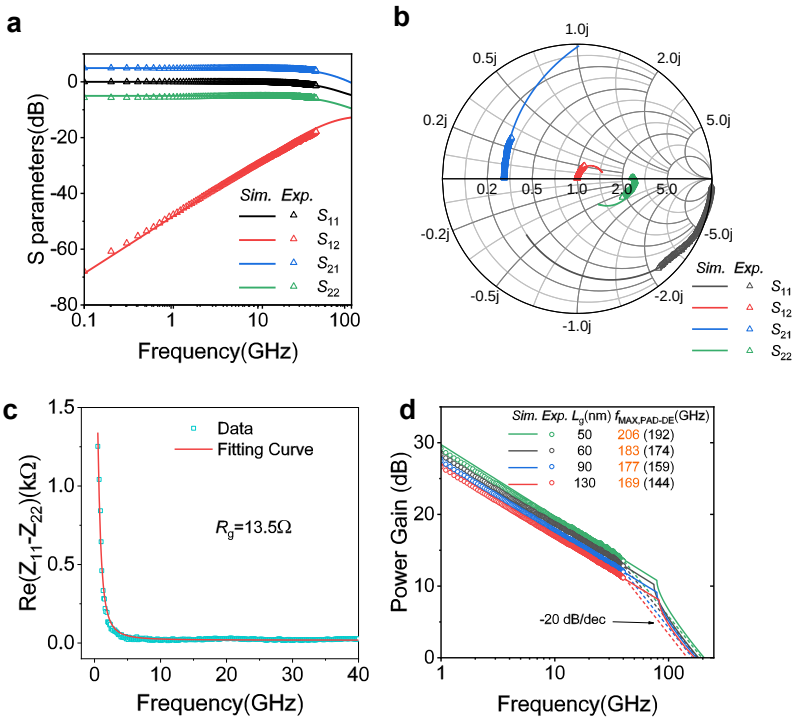
Supplementary Figure 12 | Statistic summary for 70 high-speed transistors on quartz substrates. a,**b**, On-state current density (**a**) and transconductance (**b**) distributions for totally 70 CNT FETs. The measured V_{ds} is -0.8 V. **c,** f_T/g_m ratio distributions for CNT transistors with four different L_gs. According to $f_T = g_m/2\pi C_g$, the f_T/g_m ratio is related to the parasitic capacitance of the RF devices, the higher the ratio, the smaller the parasitic capacitance. Notably, the ultralow substrate parasitics of quartz are verified by a high f_T/g_m ratio, inversely proportional to the parasitic capacitance, up to 400 GHz mS^{-1} μm. In contrast, this ratio is 145 GHz mS^{-1} μm for the CNT FETs on high-resistivity Si/SiO_2 substrates. **d**, Comparison of extrinsic f_{MAX}/f_T between reported CNT/graphene transistors and our champion RF transistor of this work. The left panel shows absolute comparison of f_{MAX}/f_T, and the right panel shows comparison of f_T (upper) and f_{MAX} (lower) at various gate lengths[20,24,39-41]. We fabricated and measured 104 CNT array transistors on quartz substrates and 70 FETs work successfully, which indicates the yield is up to 67%.



Supplementary Figure 13 | Statistic summary for 103 high-speed transistors on high-resistivity Si/SiO$_2$ substrates. a, On-state current density (I_{on}) and transconductance (g_m) of a typical 50 nm-L_g CNT array FET (V_{ds}= -0.8 V). **b-d**, Extrinsic cutoff frequency and power gain cutoff frequency statistical bar graphs of FETs with gate lengths of 60 nm (**b**), 90 nm (**c**) and 130 nm (**d**). The standard deviations of high-speed FETs for four gate lengths are listed in Supplementary Table 5. **e**, Linear fitting curves using Gummel's method for the four intrinsic f_Ts of transistors in Fig. 4b (right panel), which is identical to the extrapolated values. **f**,**g**, Distributions of $f_{T,INT}$ (**f**) and $f_{T,PAD-DE}$ (**g**) for the 50 nm devices in Fig. 4a. We fabricated and measured 140 CNT array transistors on high-resistivity Si/SiO$_2$ substrates and 103 FETs work successfully, which indicates the yield is up to 74%.



Supplementary Figure 14 | SEM images illustrating possible failure mechanisms in CNT array-based FETs. a, SEM image showing HfO_2 residuals due to film lift-off process. The residual HfO_2 at gate region may result in electrical insulation between the upper connection metal wire and gate metal. **b**, SEM image showing gate metal defects. The gate metal breakage will directly lead to electric insulation between the metal wire and gate metal. **c**, SEM image showing residual metal particle inside the channel region. These particles would short the gate and source (or drain). In summary, the failure rate of RF performance may be attributed to result mainly from the transistor failure induced in fabricating processes.



Supplementary Figure 15 | Measured and simulation data of CNT RF transistors based on AC small-signal equivalent circuit model. a,**b**, Measured (triangle) and simulation (line) of pad de-embedding scattering parameters (**a**) and in Smith curve (**b**) using Advanced Design System for 60 nm-L_g CNT transistors. V_{gs} and V_{ds} are -0.3 V and -1.4 V, respectively. The equivalent circuit is shown in Supplementary Fig. 11. **c**, Extracted gate resistance from the Z-parameters formulations based on the small-signal equivalent circuit model for a 60 nm-L_g CNT transistor[70]. **d**, Comparison of $f_{MAX,PAD-DE}$ extracted by -20 dB/dec extrapolation from available measured maximum available/stable gain terminus of 40 GHz (dash line) and simulated maximum available/stable gain (solid line). The simulation frequency is from 100 MHz to 220 GHz with a step of 200 MHz. The parameter values of CNT RF transistors are shown in Supplementary Table 6. The higher simulated results (orange numbers) indicate the slight underestimation of the extrapolation method (black numbers in parentheses). According to the measured S-parameters, the current gain (H_{21}), the maximum stable gain (MSG) and maximum available gain (MAG) of the CNT FET can be extracted by following equations

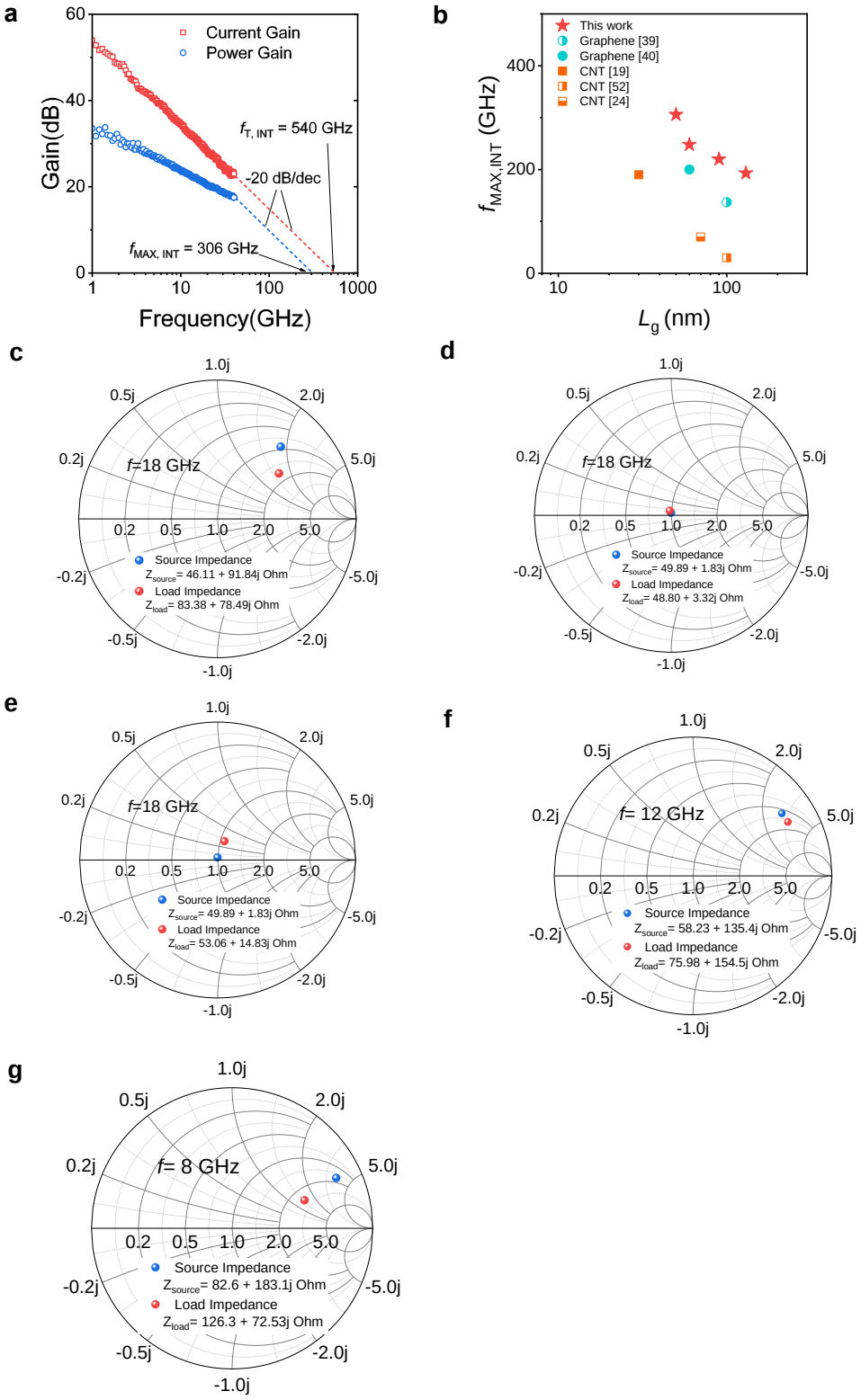
$$H_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{21})+S_{12}S_{21}}$$

$$\mathrm{MSG} = \left|\frac{S_{21}}{S_{12}}\right| (K \le 1)$$

$$\mathrm{MAG} = \left|\frac{S_{21}}{S_{12}}\left(K-\sqrt{K^2-1}\right)\right| (K > 1)$$

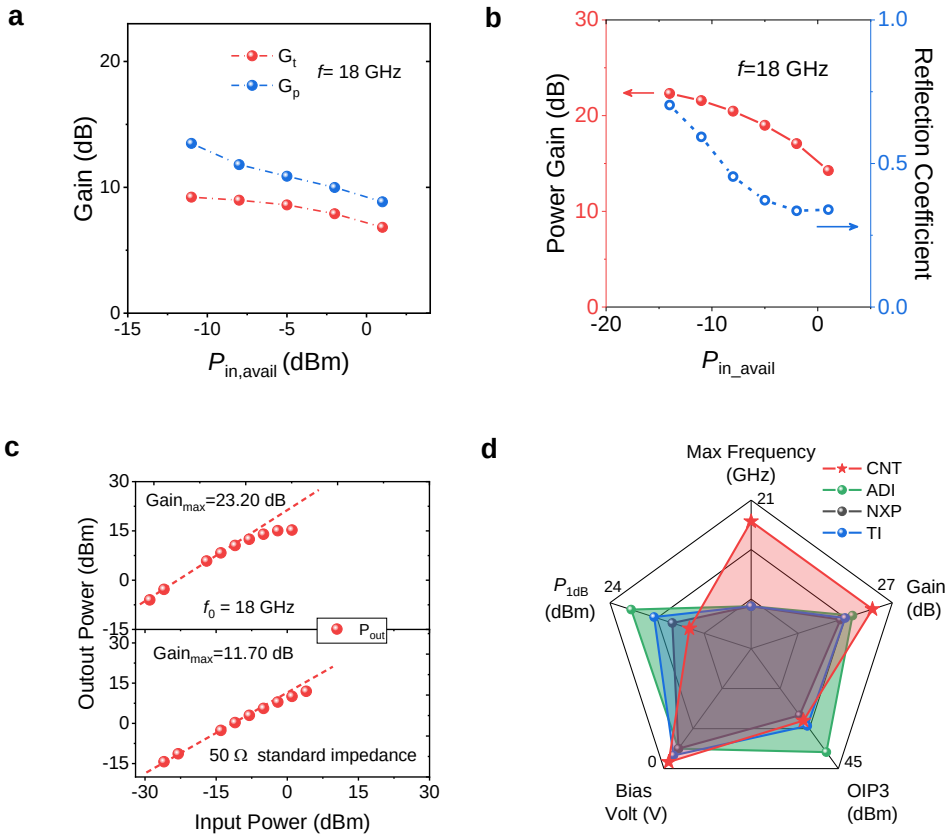
where K is the stability factor and is given by

$$K = \frac{1+|S_{11}S_{22}-S_{12}S_{21}|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{12}S_{21}|}$$



Supplementary Figure 16 | Characteristics of the champion CNT array-based FET with maximum intrinsic f_T/f_{MAX} and Smith charts showing the source and load pull impedance matching. a, Intrinsic current gain and maximum available/stable gain versus frequency of the

champion CNT transistor with L_g = 50 nm. The slope of the extension lines is -20 dB/dec. **b**, Benchmarking of intrinsic f_{MAX} with other reported carbon-based FETs[19,24,39,40,52]. **c**, The source and load impedance matching conditions of the load pull measurements for the upper panel of Fig.5b and left panel of Fig.5c @18 GHz. The source and load impedances are 46.11+91.84j Ohm and 83.38+78.49j Ohm, respectively. **d**, The source and load impedance matching condition of the load pull measurements for the bottom panel of Fig.5b @18 GHz. The source and load impedance of the measurements are 49.89+1.83j Ohm and 48.80+3.32j Ohm, respectively. **e**, The source and load impedance matching condition of the load pull measurements for Fig. 5e @18 GHz. The source and load impedance of the measurements are 49.89+1.83j Ohm and 53.06+14.83j Ohm, respectively. **f**, The source and load impedance matching condition of the load pull measurements for the left panel of Fig.5c @12 GHz. The source and load impedance of the measurements are 58.23+135.4j Ohm and 75.98+154.5j Ohm, respectively. **g**, The source and load impedance matching condition of the load pull measurements for the left panel of Fig.5c @8 GHz. The source and load impedance of the measurements are 82.6+183.1j Ohm and 126.3+72.53j Ohm, respectively. The corresponding bias conditions are (V_{gs}, V_{ds}) = (0.20, -1.65) V, (0.05, -1.65) V, (-0.15, -1.65) V for Supplementary Figure 16e-g, respectively.



Supplementary Figure 17 | Characterization for load pull measurements and comparison of commercial products with our CNT array-based amplifier. a, Comparison of G_p and G_t values in the same device. **b**, Reflection coefficient characterizations for load pull measurements. **c**, Gain curves from low input power to P_{1dB} point. **d**, Radar diagram for comparison of several figure of metrics with commercial devices. The extracted data is shown in Supplementary Table 7.

CNT arrays			
Reference number	**CNT density (CNTs/μm)**	**Mobility ($cm^2 \cdot s^{-1} \cdot V^{-1}$)**	**Metallic CNT purity (%)**
This work	**100-120**	**770-1580**	**0.01**
27	**500**	**130**	**1**
35	**50**	**410**	**0.01**
33	**30**	**650**	**33**
36	**30**	**30**	**0.1**

Supplementary Table 1 | CNT density, carrier mobility and metallic CNTs purity data for Fig. 1h.

L_{CH} (nm)	100/180/280
T_{OX} (nm)	5.4
k_{OX}	13
k_{SUB}	3.9
d (nm)	1.5
c_{qa} (fF/μm)	0.087
c_{qb} (fF/μm)	0.16
E_g (eV)	0.57
C_g (μF/cm^2)	1.6

Supplementary Table 2 | Simulation parameters used in extracting carrier mobility using the VS model for Fig. 1h.

	Supply Voltage $\|V_{dd}\|$ (V)	I_{on} (mA/μm) (N/P)	I_{off} (μA/μm) (low V_{th})
This work (L_g=90nm)	0.9	1.9	100
Si MOSFET '0.13 μm' node	1.3	1.17/0.6	10^{-1}
Si MOSFET '0.18 μm' node	1.5	0.94/0.46	10^{-2}
Si MOSFET '0.25 μm' node	1.8	0.7/0.32	10^{-3}
Si MOSFET '0.35 μm' node	2.5	0.64/0.32	10^{-3}

Supplementary Table 3 | Comparison of key metrics for silicon MOS FETs and our CNT array-based FETs for Fig. 3d.

DEVICE NUMBER	*#1*	*#2*	*#3*
L_g/ L_{ch} (nm)	**130/170**	**90/130**	**60/100**
v_{sat} $(cm \cdot s^{-1})$	$\mathbf{1.65 \times 10^7}$	$\mathbf{1.90 \times 10^7}$	$\mathbf{2.2 \times 10^7}$
Estimated f_T by $f_T=v_{sat}/2\pi L_g$ (L_{ch}) (GHz)	**202/154**	**336/233**	**584/350**
g_m (mS/um)	**1.20**	**1.25**	**1.28**
C_g(μF/cm^2)	**1.13**	**1.13**	**1.13**
Estimated f_T by $f_T=g_m/2\pi C_g$ (GHz)	**130**	**196**	**300**
As-measured f_T (GHz)	**83**	**92**	**108**
Pad de-embedding f_T (GHz)	**130**	**161**	**235**
Intrinsic f_T (GHz)	**156**	**238**	**340**

Supplementary Table 4 | Comparison of estimated f_T by dc figures of merit and actual pad de-embedding and intrinsic f_T.

L_g (nm)	50	60	90	130
$f_{T,EXT}$ deviation (%)	7.82%	6.23%	3.70%	2.12%
$f_{MAX,EXT}$ deviation (%)	11.10%	8.42%	5.74%	4.36%

Supplementary Table 5 | Standard deviations of our CNT array-based FETss' extrinsic f_T and f_{MAX} with four different L_gs for Fig. 4a and Supplementary Fig. 13b-d.

L_{gate} /nm	C_{gd}(aF /um)	C_{ds}(aF /um)	C_{gs}(aF /um)	g_m(mS /mm)	g_{ds}(mS /mm)	R_d(Ω · μm)	R_g(Ω)	R_s(Ω · μm)	$f_{MAX,PAD-DE}$ from Simulation (GHz)	$f_{MAX,PAD-DE}$ from 20dB/dec extrapolation (GHz)
50	94.0	125.7	380.6	1242.9	868.7	409.5	21.11	262.9	206	192
60	106.0	131.4	588.9	1290.3	502.8	350.0	12.92	325.9	183	174
90	140.3	154.3	783.1	1247.7	403.7	353.5	8.51	315.4	177	159
130	143.1	265.7	1128.6	1218.9	363.2	255.2	4.82	367.9	169	144

Supplementary Table 6 | Parameter values of the CNT high-speed transistors for the simulation results shown in Supplementary Fig. 15d using ADS software.

	A-CNT This work	NXP MMG38151B	TI TRF37C73	ADI ADL5610
Frequency(GHz)	8-18	0.001-6	0.04-6	0.03-6
Gain (dB)	23.2 @ 18 GHz	17.1@3.8 GHz	18 @ 2 GHz	19.4@0.9 GHz
Output P_{1dB}(dBm)	10.5 @ 18 GHz	13.4@3.8GHz	16.5 @ 2 GHz	20.4@0.9 GHz
Bias voltage (V)	1.65	5	3.3	5
OIP3 (dBm)	27@18 GHz	25@3.8 GHz	28.5@2 GHz	38.8@0.9 GHz

Supplementary Table 7 | Comparison of key metrics for RF gain amplifiers and our CNT array-based amplifier for Supplementary Fig. 17d.

Convert Y to S	Convert S to Y
$S_{11}=\frac{(1-Y_{11})(1+Y_{22})+Y_{12}Y_{21}}{\Delta_1}$	$Y_{11}=\frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{\Delta_2}$
$S_{12}=\frac{-2Y_{12}}{\Delta_1}$	$Y_{12}=\frac{-2S_{12}}{\Delta_2}$
$S_{21}=\frac{-2Y_{21}}{\Delta_1}$	$Y_{21}=\frac{-2S_{21}}{\Delta_2}$
$S_{22}=\frac{(1+Y_{11})(1-Y_{22})+Y_{12}Y_{21}}{\Delta_1}$	$Y_{22}=\frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{\Delta_2}$
Extract R_g from Z-parameters	
$\mathrm{Re}(Z_{11}-Z_{12})=R_g+\frac{A_g}{\omega^2+B}$	

Where, $\Delta_1=(1+Y_{11})(1+Y_{22})-Y_{12}Y_{21}$, $\Delta_2=(1+S_{11})(1+S_{22})-S_{12}S_{21}$, Z_{11} and Z_{12} are Z parameters, A_g and B are constant values at fixed bias, and ω is circular frequency.

Supplementary Table 8 | Equations of parametric conversions and extractions.

References

64 Frank, D. J., Taur, Y. & Wong, H.-S. Generalized scale length for two-dimensional effects in MOSFETs. *IEEE Electron Device Letters* **19**, 385-387 (1998).

65 Deng, J. & Wong, H.-S. P. Modeling and analysis of planar-gate electrostatic capacitance of 1-D FET with multiple cylindrical conducting channels. *IEEE Transactions on Electron Devices* **54**, 2377-2385 (2007).

66 Majumdar, A. & Antoniadis, D. A. Analysis of carrier transport in short-channel MOSFETs. *IEEE Transactions on Electron Devices* **61**, 351-358 (2014).

67 Xu, L.; Gao, N.; Zhang, Z.; Peng, L.-M., Lowering interface state density in carbon nanotube thin film transistors through using stacked Y2O3/HfO2 gate dielectric. *Applied Physics Letters* **2018,** *113* (8).

68 Lee, S. & Yu, H. K. Determining non-quasi-static small-signal equivalent circuit of a RF silicon MOSFET. *Solid-State Electronics* **45**, 359-364 (2001).

69 Bagheri, M. & Tsividis, Y. A small signal dc-to-high-frequency nonquasistatic model for the four-terminal MOSFET valid in all regions of operation. *IEEE Transactions on Electron Devices* **32**, 2383-2391 (1985).

70 Lee, S. & Yu, H. K. Parameter extraction technique for the small-signal equivalent circuit model of microwave silicon MOSFETs. *1997 Proceedings IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits*, 182-191 (1997).