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Supplementary information

High-performance flexible nanoscale transistors based on transition metal dichalcogenides

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Supplementary Information

High-performance flexible nanoscale transistors based on transition metal dichalcogenides

Alwin Daus[1], Sam Vaziri[1], Victoria Chen[1,†], Çağıl Köroğlu[1,†], Ryan W. Grady[1], Connor S. Bailey[1], Hye Ryoung Lee[2], Kirstin Schauble[1], Kevin Brenner[1] and Eric Pop[1,3,*]

[1]Department of Electrical Engineering, Stanford University, Stanford, CA 94305, U.S.A.

[2]Geballe Laboratory for Advanced Materials, Stanford University, Stanford, CA 94305, U.S.A.

[3]Department of Materials Science & Engineering, Stanford University, Stanford, CA 94305, U.S.A.

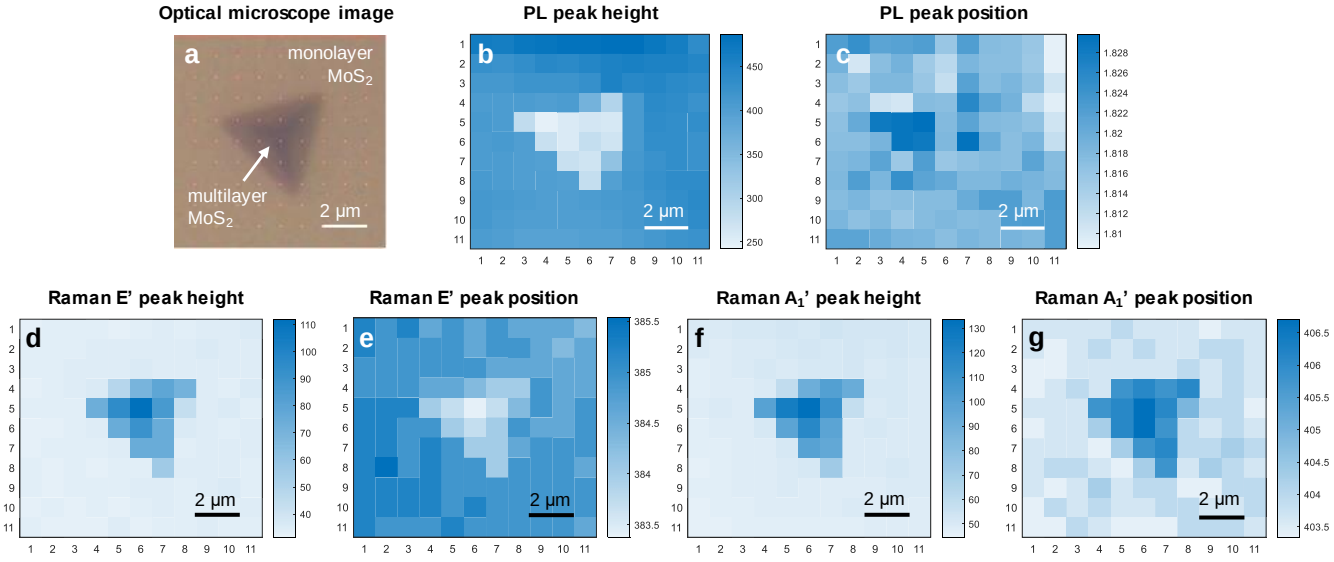
[†]These two authors contributed equally. [*]Corresponding author email: epop@stanford.edu

1. MoS_2 film properties, growth conditions, SiO_2/Si substrate preparation

MoS_2 was synthesized by CVD growth as described in prior work.[27,28] The SiO_2/Si substrates were pretreated by hexamethyldisilazane (HMDS) vapor to provide a hydrophobic surface for the subsequently applied seeding promoter (PTAS, i.e. perylene-3,4,9,10 tetracarboxylic acid tetrapotassium salt dissolved in DI water and dried on a hot plate) on the edges of the chip, which prevents spreading towards the chip center. The same substrate treatments were applied for the growth of the other TMDs. The MoS_2 growth from solid precursors (MoO_3 and S) then forms large single crystal triangles with sizes in the order of tens of microns which coalesce into a continuous film in the chip center, and non-continuous areas closer to the chip edge (see Fig. 1 in previous work[27]).

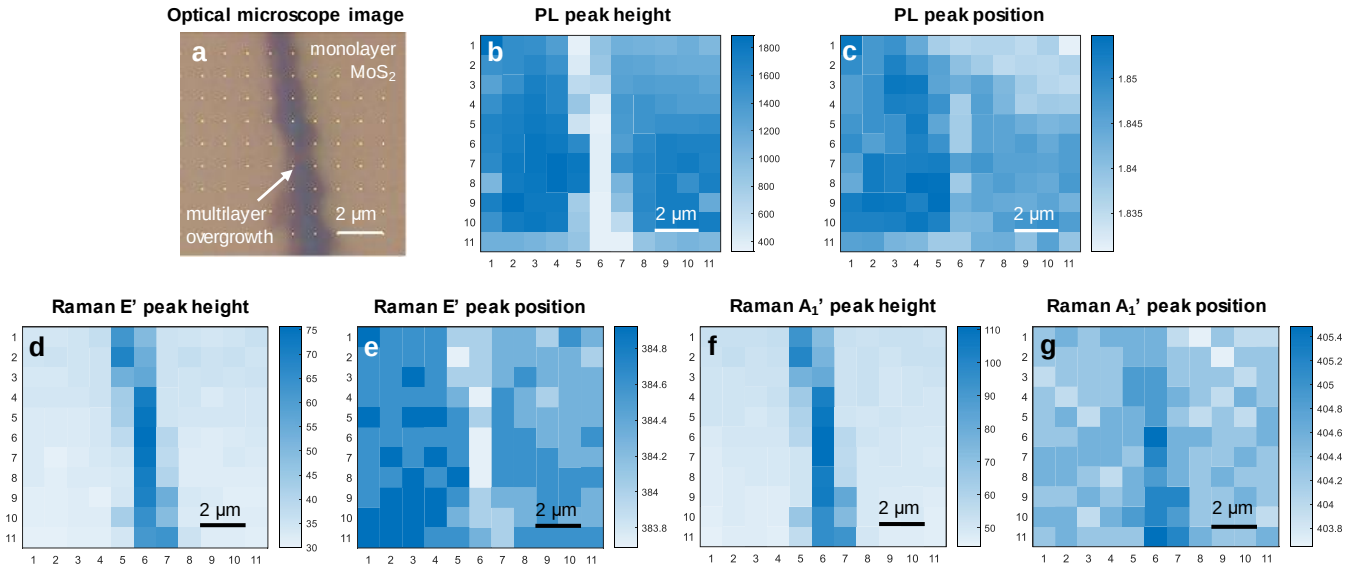
Although the MoS_2 film can essentially be characterized as a monolayer film, some small multilayer islands and overgrowth are present at grain boundaries or nucleation sites. Supplementary Fig. 1 and 2 display Raman and photoluminescence (PL) mapping of a multilayer region and grain boundary, respectively, each surrounded by monolayer MoS_2. As visible from the peak positions, the Raman peak separation is increased in these multilayer regions suggesting a thickness of about 2-3 MoS_2 layers.[59]

The amount of overgrowth and multilayers can vary depending on the location on the sample (edge vs. center) and between growths. This is further quantified by optical image analysis performed on samples used for flexible devices based on the transfer process described in this work. Supplementary Fig. 3a,b shows examples where unpatterned MoS_2 was transferred together with contacts (for *Type A* devices)

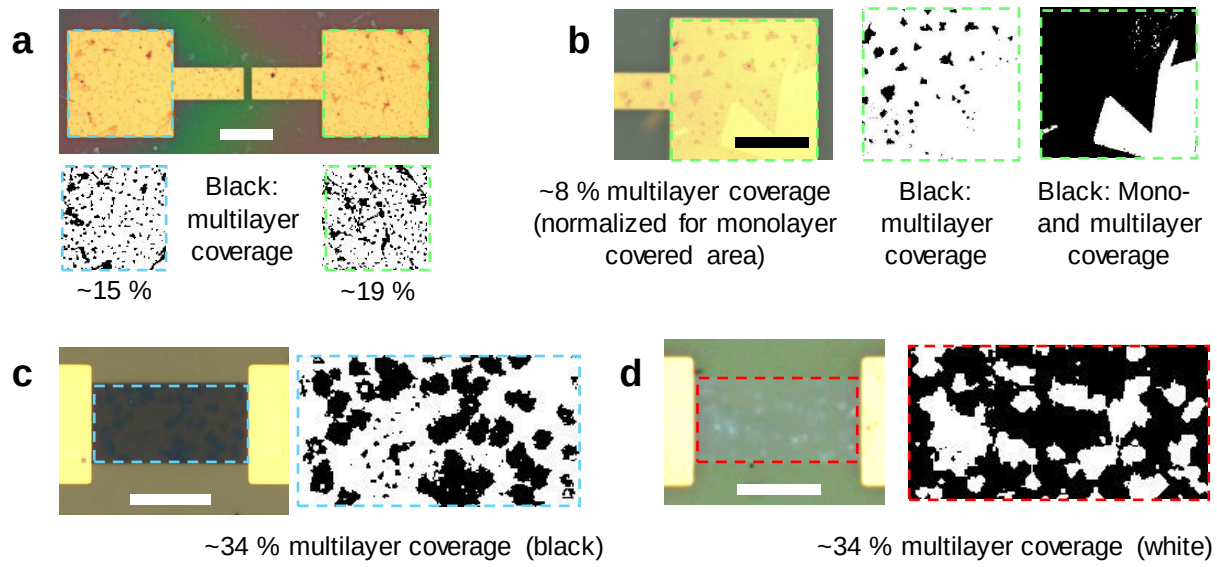


Supplementary Fig. 1 | Raman and photoluminescence (PL) mapping of an MoS_2 multilayer island surrounded by monolayer MoS_2 on SiO_2/Si. a, Optical image of mapped area. **b**, PL peak height. **c**, PL peak position. **d**, Raman E' peak height. **e**, Raman E' peak position. **f**, Raman A_1' peak height. **g**, Raman A_1' peak position.

from the center of the chip (a) and from the chip edge (b). The threshold brightness analysis of these images indicates a multilayer coverage of 8-19%. For another example of *Type B* devices during processing (located in chip center), we find that the multilayer coverage can be as high as 34 %



Supplementary Fig. 2 | Raman and photoluminescence (PL) mapping of an MoS_2 grain boundary surrounded by monolayer MoS_2 on SiO_2/Si. a, Optical image of mapped area. **b**, PL peak height. **c**, PL peak position. **d**, Raman E' peak height. **e**, Raman E' peak position. **f**, Raman A_1' peak height. **g**, Raman A_1' peak position.

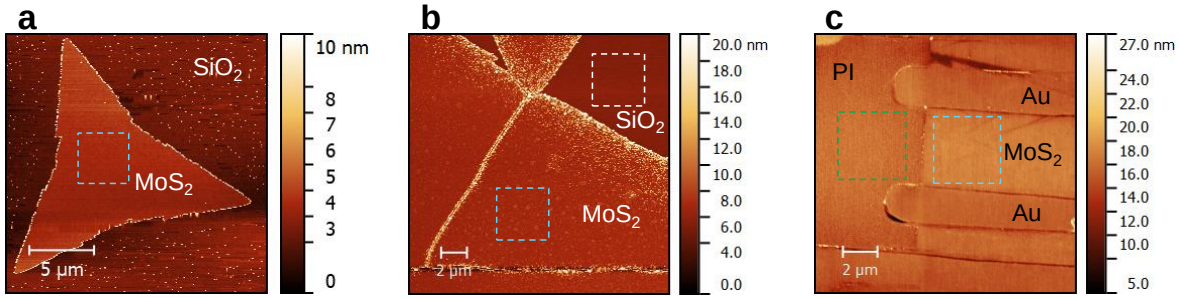


Supplementary Fig. 3 | Optical analysis of mono- vs. multilayer regions of MoS_2. a, Continuous MoS_2 film in chip center of a *Type A* device after transfer, scale bar: 50 µm. **b**, Non-continuous MoS_2 region in chip edge of a *Type A* device after transfer, scale bar: 50 µm. **c**, Etched MoS_2 film of a *Type B* device before transfer, scale bar: 20 µm. **d**, Etched MoS_2 film of a *Type B* device after transfer, scale bar: 20 µm.

(Supplementary Fig. 3c,d). Thus, for micron-scale devices we can assume that the channel will be mostly composed of monolayer MoS_2 (including multilayer islands), while most nanoscale channels will likely be monolayers with the occasional chance of continuous bilayers in the channel gap.

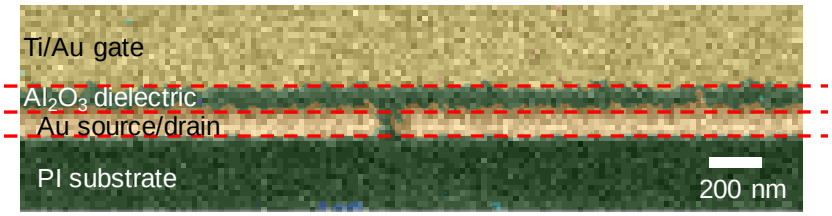
2. Surface analysis before and after transfer

To investigate the surface morphology of the MoS_2 covered regions before and after transfer, we performed atomic force microcopy (AFM). We find that the as-grown MoS_2 has a root-mean-square (rms) roughness of 0.18 – 0.45 nm depending on growth run and sample location, which is comparable to or slightly larger than the nominal SiO_2 roughness (Supplementary Fig. 4). In addition, we have also measured the roughness after transfer and capping with 35 nm Al_2O_3 (evaporated Al seed layer + atomic-layer deposition as described in Methods), which yielded a roughness of 0.39 nm on the MoS_2 covered region and 0.44 nm where MoS_2 was etched prior to transfer. This confirms that the extremely smooth MoS_2 surface is preserved even after transfer. In addition, the AFM reveals that the height difference between MoS_2 and Au surfaces is less than 2 nm which confirms that the 45 nm thick contacts are embedded in the substrate and topography is effectively eliminated. This is further visualized in the cross-section SEM image after completed device fabrication in Supplementary Fig. 5, where Al_2O_3 and Au cover the contacts and channel without any “steps” in surface topography.



Note: Al_2O_3 capped across the entire area.

Supplementary Fig. 4 | Atomic Force Microscopy (AFM) of **a,** a single MoS_2 triangle on SiO_2/Si with a root mean square (rms) roughness of 0.18 nm measured in region of light blue dashed box, **b,** an MoS_2 on SiO_2/Si region of coalescing grains with rms roughness of 0.45 nm for MoS_2 (light blue dashed box) and 0.23 nm for the bare SiO_2 surface (white dashed box), and **c,** the MoS_2 and Au structures on polyimide after transfer and alumina capping (on the entire area) with rms roughness of 0.39 nm on the region with MoS_2 (light blue dashed box) and of 0.44 nm on the region where MoS_2 was etched (green dashed box).



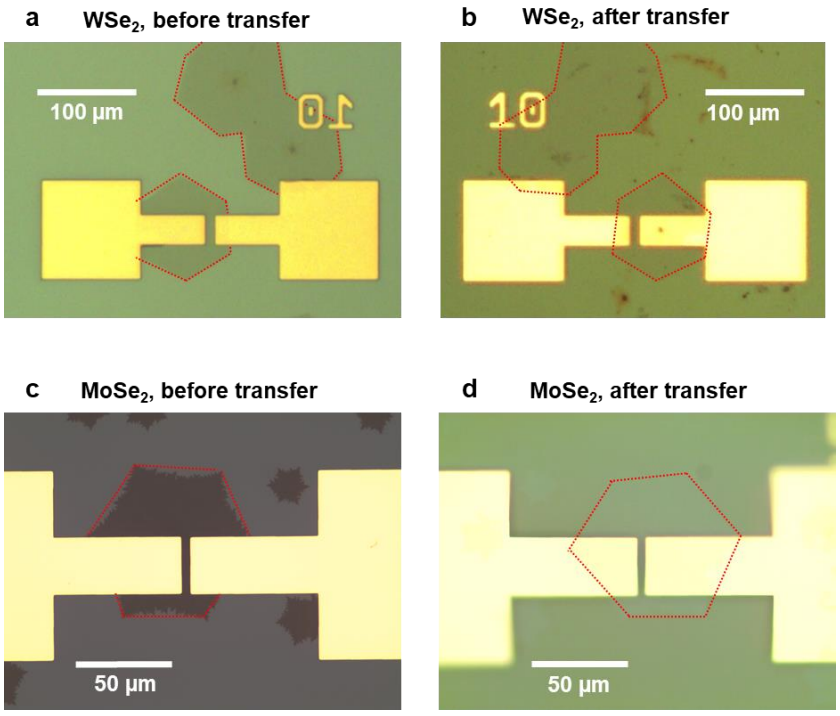
Supplementary Fig. 5 | Scanning-electron microscopy (SEM) cross-section of a ~100 nm long channel MoS_2 transistor, colorized version of Fig. 3a. Red dashed lines show the source and drain electrodes are embedded in the PI, and no "steps" in surface topography can be discerned.

3. Optical microscope images for WSe_2 and $MoSe_2$ before and after the transfer process

Supplementary Fig. 6a,c displays the hexagonally shaped WSe_2 and $MoSe_2$ crystal grains grown on SiO_2/Si substrates after the patterning of source/drain metal contacts, and *before* the transfer. As visible here, the Au contacts are on top of the TMDs. When the polyimide (PI) is applied on top, it uniformly covers and embeds the contacts. After releasing the PI together with metals and TMDs from the SiO_2/Si substrates (main text Fig. 1b), the substrate is flipped over as visible in the numbering ("10") when comparing Supplementary Fig. 6a,b. This also leads to a reversal of the material stack, where the TMDs are on top of Au/PI or PI, as visible in Supplementary Fig. 6b,d.

4. Raman spectroscopy and Photoluminescence measurements before and after transfer process

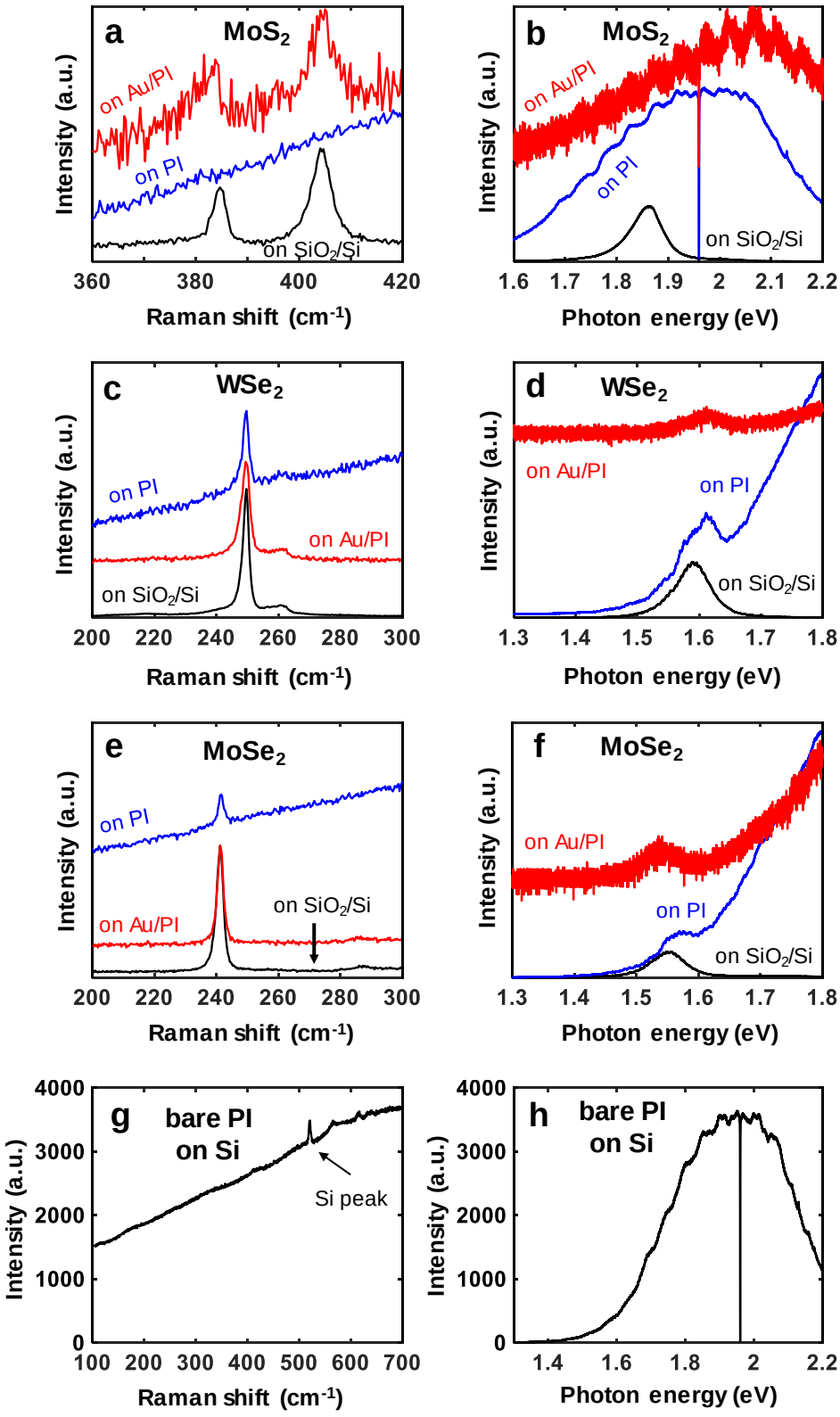
The different TMDs were monitored with Raman spectroscopy and photoluminescence (PL) throughout the transfer process to investigate any changes in material properties. Supplementary



Supplementary Fig. 6 | Microscope images of WSe_2 and $MoSe_2$ with patterned Au metal electrodes. a, WSe_2 on SiO_2/Si before transfer. **b**, WSe_2 on polyimide (PI) after transfer. **c**, $MoSe_2$ on SiO_2/Si before transfer. **d**, $MoSe_2$ on PI after transfer.

Fig. 7a-f display the spectra for MoS_2, WSe_2 and $MoSe_2$ before and after transfer. Because we have deposited and patterned metal contacts before the transfer, released all materials together, and flipped the flexible PI substrate, we were able to measure the TMDs after transfer on the metal surface and on the PI surface.

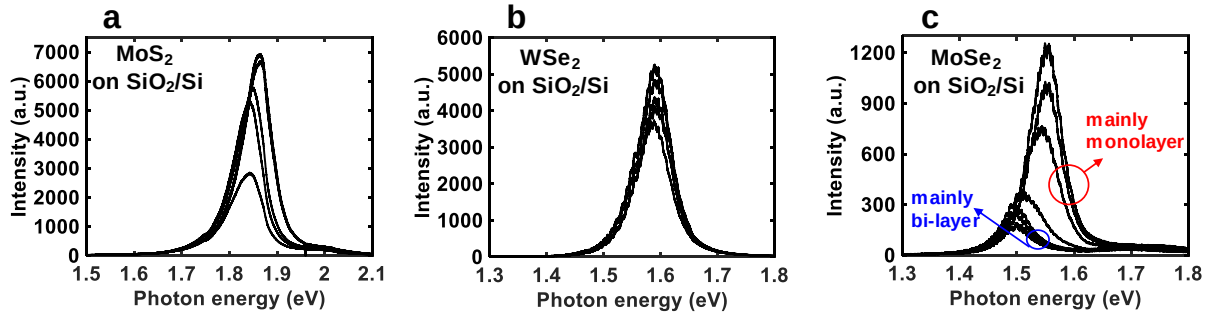
We observed that the measurements directly on PI (without a metal in between the TMD and PI) have a broad background signal, which is absent on the SiO_2/Si substrates and on Au surfaces. This background signal is in the range where we expect the vibrational modes of the TMDs, and there is, for instance, a significant overlap with the PL energy maximum of monolayer MoS_2 (Supplementary Fig. 7b). The Raman and PL measurements for bare PI (on Si) are shown in Supplementary Fig. 7g,h for comparison. Because of this background signal, the MoS_2 Raman and PL peaks are buried and not visible in our measurements on PI. However, the peaks of WSe_2 and $MoSe_2$ on the PI surface can be resolved (Supplementary Fig. 7c-f). We note that a Raman laser with shorter wavelength could possibly help to reduce the background signal from PI and improve detection of TMDs.[60] Further, the insertion of Au between PI and the TMD suppresses this background signal and enables the detection of the Raman signature of all three TMDs.



Supplementary Fig. 7 | Raman (left column) and photoluminescence (right column) spectra. **a,b,** MoS_2. **c,d,** WSe_2. **e,f,** $MoSe_2$. **g,h** bare polyimide (PI) on silicon.

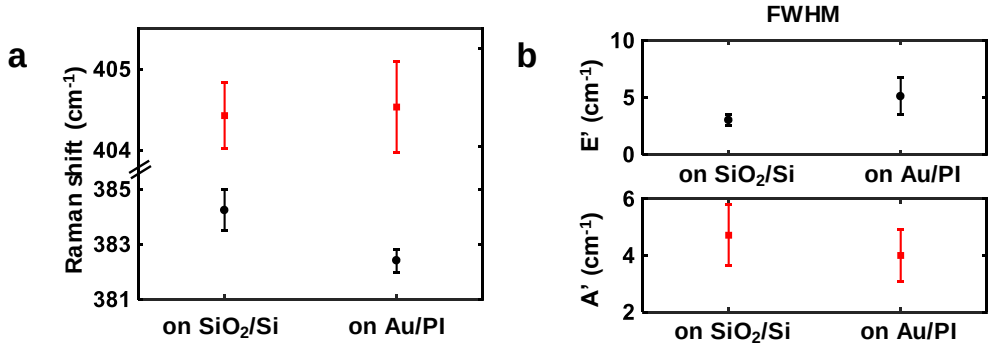
We find that the PL peaks for WSe_2 and $MoSe_2$ can be detected on PI and Au/PI despite the strong PL quenching that is known to appear on Au surfaces.[33,34] The PL peak energies of MoS_2, WSe_2 and $MoSe_2$ are ~1.86 eV, ~1.59 eV and ~1.54 eV, all indicating monolayer thickness.[29,61-63] While these results were consistent for MoS_2 and WSe_2 across the substrate, we found that $MoSe_2$ had areas with monolayers and bilayers (~50%) (Supplementary Fig. 8), where the PL peak is shifted towards ~1.50 eV and its intensity is significantly reduced. The noticeable spread in PL energies for MoS_2 can be attributed to a variety of effects such as nanoscale bilayer regions[27,28] or small local variations in strain or doping. For $MoSe_2$, however, we find two sets of PL energy peak positions, which indicate that some areas mainly consist of monolayers and some mainly of bilayers (~50% each).[29,61]

Changes in the Raman and PL spectra before vs. after transfer can be interpreted as strain release effects or phonon interactions with the bottom surfaces (PI or Au), as will be discussed in the following. For MoS_2 on Au, we find that the E' peak shifts by about -1.8 cm^{-1} and its full-width-half-maximum (FWHM) increases, whereas the A'_1 peak does not change discernably (see Supplementary Fig. 9), which has been observed for non-transferred Au/MoS_2 stacks and thus cannot be correlated with the transfer process. Possible mechanisms for this E' peak shift and broadening can be tensile strain induced from the Au deposition[64,65] or electron-phonon interactions due to Au plasmons.[66,67] For WSe_2, the changes in the Raman and PL spectra are small (Supplementary Fig. 10). The minor shifts in the PL peak position and Raman E' peak of about +0.02 eV and -0.1 to -0.2 cm^{-1}, respectively cannot be consistently correlated with any strain release during transfer,[68] and may be related to small effects from interactions with the substrate.[69] It is difficult to deduce any strain effects from PL and Raman for $MoSe_2$, due to small changes and existence of mono- and bilayers adding uncertainty to the Raman and PL analysis. Still, the results suggest the possibility of slight strain changes in tensile and compressive directions on Au/PI and PI surfaces, respectively (see Supplementary Fig. 11).[70-72]

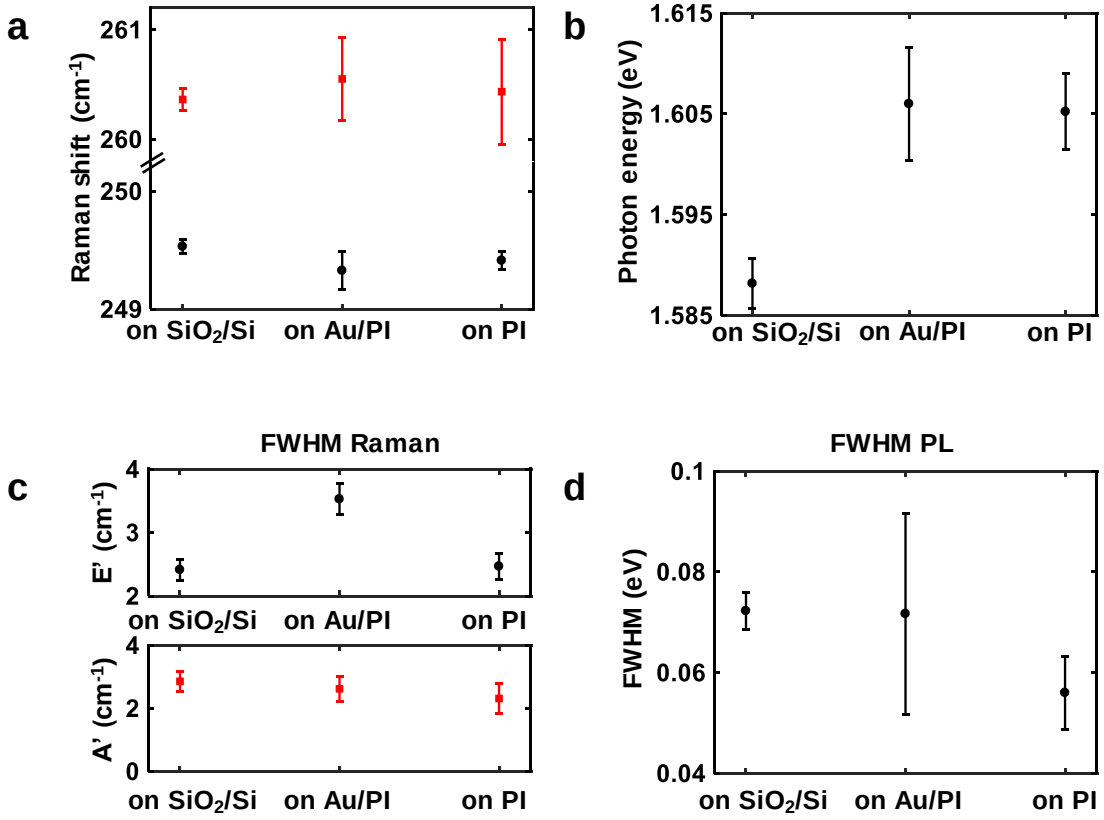


Supplementary Fig. 8 | PL measurements before transfer of **a,** MoS_2, **b**, WSe_2 and **c**, $MoSe_2$.

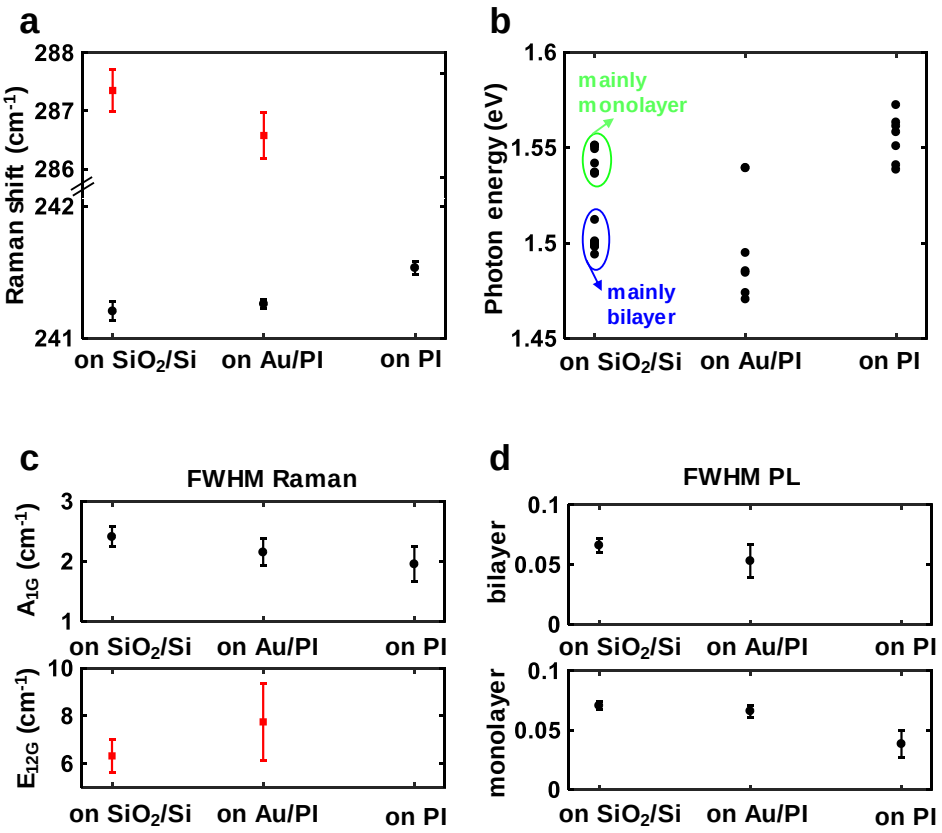
Overall, the FWHM of the Raman and PL peaks for all the TMDs do not increase except on Au electrodes, where previously discussed plasmonic effects could be the leading cause. This indicates that the disorder, which would be affected by crystal grain size or defect density, in the materials is not increased throughout the transfer process.[73,74] This conclusion is also supported by the good electrical



Supplementary Fig. 9 | Averaged Raman (over ~5 spots on the same chip) **a**, peak positions and **b**, Full-width-half-maximum (FWHM) of MoS_2 before transfer (as-grown, on SiO_2/Si substrate) and after transfer (on Au/PI).



Supplementary Fig. 10 | Averaged (over ~5 spots on the same chip) **a**, Raman and **b**, photoluminescence (PL) peak positions of WSe_2 before and after transfer. Averaged full-width-half-maximum (FWHM) for **c,** the Raman and **d**, the PL measurements.



Supplementary Fig. 11 | a, Averaged Raman (over ~5 spots on the same chip) and **b,** photoluminescence (PL) peak positions of $MoSe_2$ before and after transfer. Averaged full-width-half-maximum (FWHM) for **c**, the Raman and **d**, the PL measurements (~10 spots across two chips). Note, missing data e.g., for the Raman E_{12G} peak on PI means that these peaks could not be detected on that particular surface.

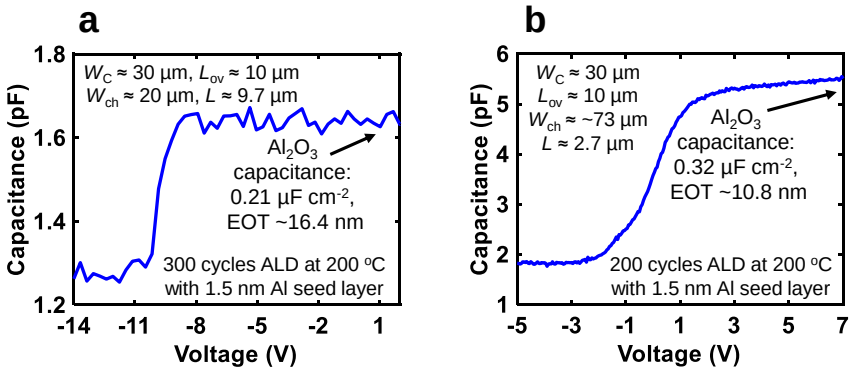
properties, which are comparable on the materials after transfer with those before transfer (i.e. on rigid SiO_2/Si substrates) from previous studies using the same CVD material type.[27,28,35]

5. Mobility, Gate Capacitance, and Threshold Voltage Extraction

We performed the extraction of the extrinsic field-effect mobility $\mu_{FE,ext}$ and threshold voltage V_T from the g_m maximum based on the following equation (valid for small drain-source voltages V_{DS}):

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\mu_{FE,ext} C_{ox} V_{DS} W}{L},$$

where the I_D plotted vs. V_{GS} can be fitted linearly to obtain $\mu_{FE,ext}$. Furthermore, the intercept with the V_{GS} axis yields V_T.[75,76] The channel width W and the channel length L are given by the device geometry. The gate oxide capacitance per unit area (C_{ox}) is determined by connecting source and drain of the



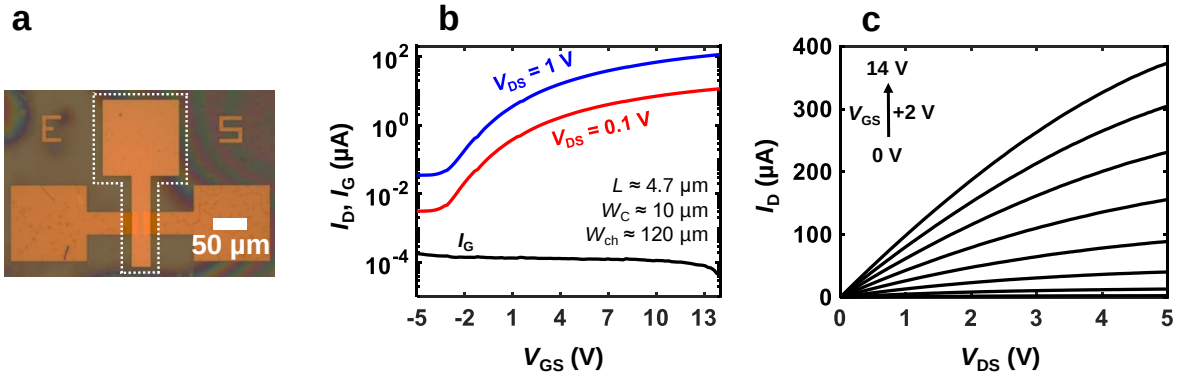
Supplementary Fig. 12 | Measured capacitance-voltage (*C*-*V*) characteristics of flexible TMD-FETs. Typical *C*-*V* for **a**, MoS_2 FETs and **b**, $MoSe_2$ and WSe_2 FETs, where the calculated Al_2O_3 capacitance density and equivalent oxide thickness (EOT) represent average values (~5 devices). L_{ov} is the overlap length between the gate electrode and the source/drain electrodes.

transistors to ground, and applying a voltage to the gate electrode. We then perform small-signal capacitance-voltage (*C*-*V*) measurements where the direct-current (dc) voltage is swept while applying an alternating-current (ac) voltage with an amplitude = 100 mV and frequency = 20 kHz. The results for Al_2O_3 gate dielectrics (including 1.5 nm Al seed layer) deposited in 300 cycles (MoS_2 FETs) and 200 cycles (WSe_2 and $MoSe_2$ FETs) are shown in Supplementary Fig. 12a and b, respectively.

As all transistors are *n*-channel devices, we estimate the capacitance of the Al_2O_3 gate dielectrics at positive bias voltage (when the channel is in accumulation) by dividing the measured capacitance (Supplementary Fig. 12) with the overlap area of the gate with the source, drain, and semiconductor channel.[36] For MoS_2 FETs the extracted $C_{ox} \approx 0.21$ µF cm^{-2} or an equivalent oxide thickness (EOT) ~16.4 nm, and for WSe_2 and $MoSe_2$ FETs we obtain $C_{ox} \approx 0.32$ µF cm^{-2} or EOT ~ 10.8 nm. Estimating the relative dielectric constant ε_r from C_{ox} and the Al_2O_3 thickness obtained by ellipsometry, we find $\varepsilon_r \approx$ 7-8, which is in the expected range.[77,78] Note, the ellipsometric thickness of 200 cycles and 300 cycles of atomic-layer deposited (200°C) Al_2O_3 measured on silicon is around 22 nm and 35 nm, respectively. However, for the transistor capacitance the 1.5 nm oxidized Al seed layer adds to the overall thickness, while the optical lithography and lift-off process of the top (gate) electrode exposes the Al_2O_3 to the basic photoresist developer which can etch the material, thus slightly reducing its thickness.

6. Flexible MoS_2 Field-Effect Transistors of *Type A*

Supplementary Fig. 13 displays a top-down optical microscope image and the electrical characteristics of a flexible MoS_2 field-effect transistor (FET) of *Type A* with 4.7 µm channel length. The device exhibits an extrinsic field-effect mobility $\mu_{FE,ext}$ ~14.2 cm^{2}V^{-1}s^{-1}, on-current I_D ~ 5.5 µA µm^{-1} at a drain-

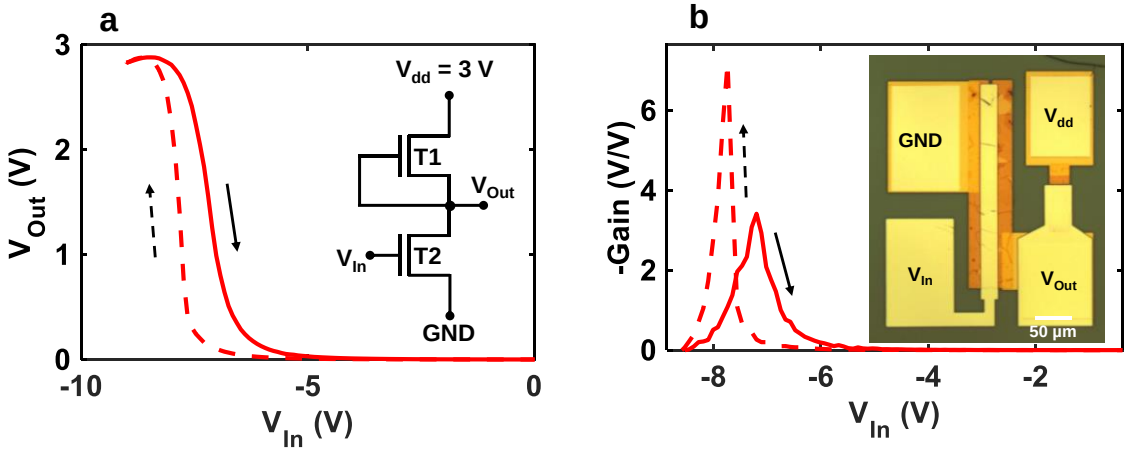


Supplementary Fig. 13 | MoS_2 field-effect transistors (FETs) of *Type A*. a, Top-down optical microscope image, white dotted line marks the outline of the MoS_2 area. **b**, Measured transfer characteristics. Red and blue lines represent drain current, I_D. **c**, Output characteristics.

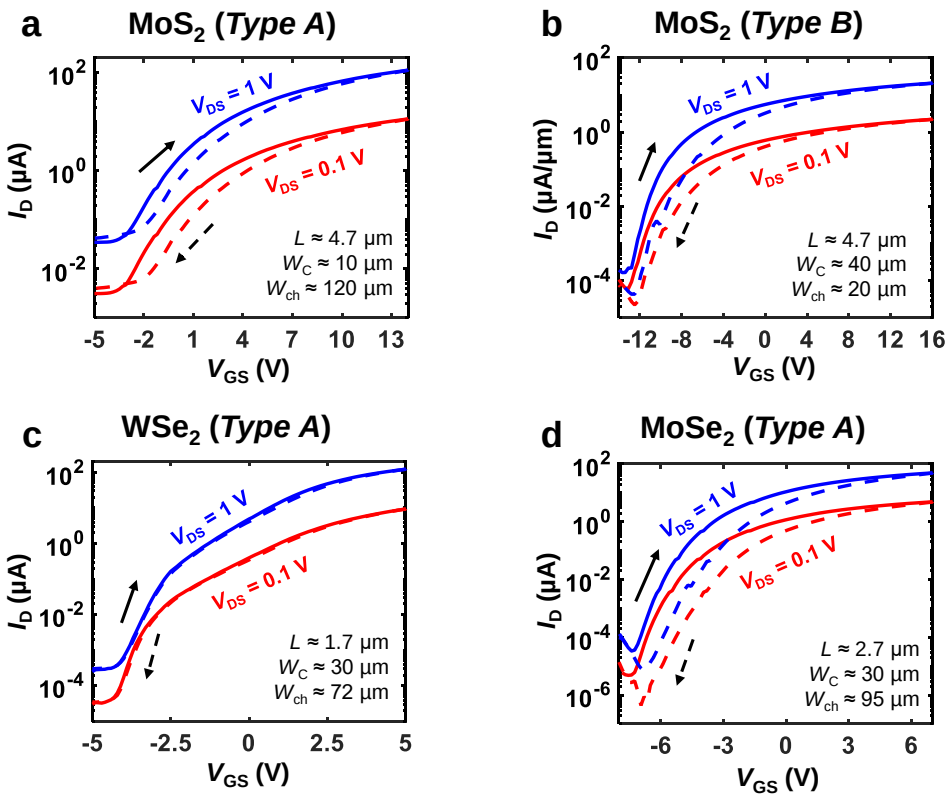
source voltage V_{DS} = 1 V, threshold voltage V_T = 3.9 V, minimum subthreshold swing SS ≈ 1.7 V dec^{-1} and on/off ratio ~3.6×10^3. Note that $\mu_{FE,ext}$ and I_D have been corrected for current spreading, which is described in Section 15 below.

7. Flexible MoS_2 Inverter based on *Type B* device fabrication process

The fabrication process for *Type B* devices further facilitates the realization of circuits because MoS_2 is already defined before gate dielectric deposition and the second metallization, which simplifies connecting bottom and top metallization layers. For instance, these are useful for practical circuits, where the gates and source/drain contacts of some transistors need to be connected (see inset of Supplementary Fig. 14a). Supplementary Fig. 14 shows the characteristics of a proof-of-concept flexible inverter realized with two *n*-type MoS_2 transistors.



Supplementary Fig. 14 | Flexible inverter with *Type B* MoS_2 transistors. a, Transfer characteristic of the inverter. Inset shows the schematic circuit diagram with transistors T1 (W_{ch}/L ≈ 20/39.7 µm) and T2 (W_{ch}/L ≈ 300/4.7 µm) **b**, Gain of the inverter shown in a. Inset shows an optical microscope image of the inverter after fabrication.



Supplementary Fig. 15 | Hysteresis in flexible transition metal dichalcogenide field-effect transistors. a, MoS_2 (*Type A*). **b**, MoS_2 (*Type B*). **c**, WSe_2 (*Type A*). **d**, $MoSe_2$ (*Type A*).

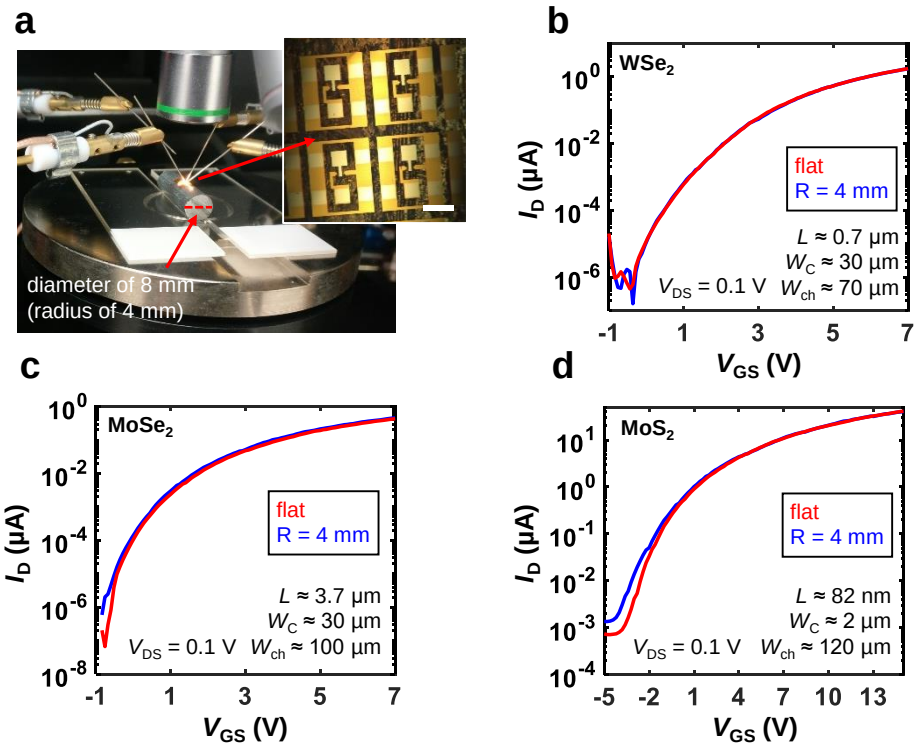
8. Hysteresis

Comparing hysteresis[37] for *Type A* and *Type B* devices, we find similar maximum values of ~1.2 V for MoS_2 FETs, which indicates that the additional etch step before transfer does not deteriorate the TMD interfaces (Supplementary Fig. 15a,b). The WSe_2 FET displays low hysteresis ~0.1 V (Supplementary Fig. 15c), and the $MoSe_2$ FET has maximum hysteresis of ~1.6 V (Supplementary Fig. 15d).

9. Bending of flexible TMD FETs

Flexible electronics need to remain unaltered when mechanically deformed, for instance, by bending the substrate. While the ductility of materials matter for the maximum strain that flexible electronics can sustain,[79] the easiest way to minimize impacts of strain on flexible electronic devices is to minimize the substrate thickness. The strain at a given bending radius can be approximated as:[80]

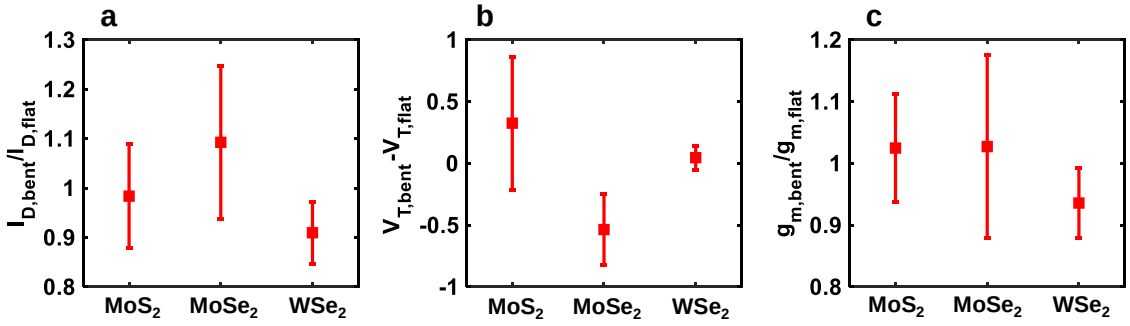
$$strain = \frac{d}{2r},$$



Supplementary Fig. 16 | Mechanical bending of flexible TMD-FETs. a, Photograph and microscope image (scale bar: 200 µm) of the measurement setup where the FETs are bent to a tensile radius of 4 mm. Measured transfer characteristics of **b**, WSe_2 (*Type A*), **c,** $MoSe_2$ (*Type A*) and **d**, MoS_2 (*Type A*). All show no significant changes on substrate bending at the 4 mm radius.

where d is the substrate thickness and r is the radius of curvature. Thus, by minimizing d to a few micrometers, the strain at common bending radii on the order of millimeters is minimized. We show this by using a ~5 µm thick PI substrate and bending it to a radius of 4 mm, which results in ~0.063% of strain. Consequently, the electrical characteristics of the TMD FETs remain visually unaltered in this condition as shown in Supplementary Fig. 16.

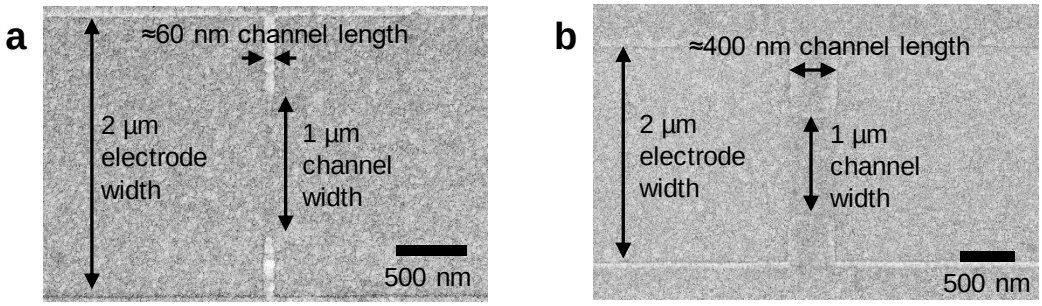
For a detailed quantitative evaluation, we have further analyzed transistor parameters such as drain current I_D, threshold voltage V_T and transconductance g_m (see Supplementary Fig. 17). Average I_D and g_m changes remain within 10% of the flat state values and absolute V_T shifts are mostly < 0.5 V. Given that the applied strain is low even at r = 4 mm, we conclude that no systematic correlations of strain with device performance parameters can be deduced from these results and we successfully confirmed the bending stability of our devices.



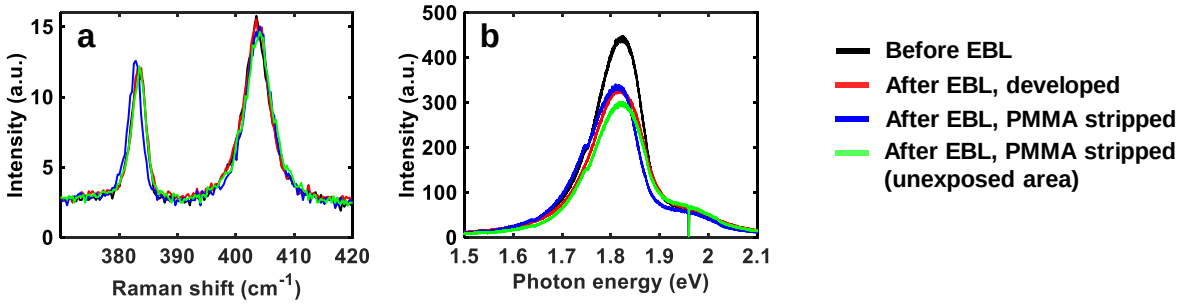
Supplementary Fig. 17 | Quantitative analysis of TMD transistors under bending to a radius of 4 mm. For MoS_2, $MoSe_2$ and WSe_2, displayed values represent the average and standard deviation of 12, 6 and 3 devices, respectively. a, Maximum drain current I_D under bending normalized by its value in flat condition. **b**, Threshold voltage shift $V_{T,bent} - V_{T,flat}$. **c,** Maximum transconductance g_m normalized by its value in flat condition.

10. SEM images of transistor channels fabricated with electron-beam lithography (EBL)

We verified the channel dimensions in our transistors by performing scanning-electron microscopy (SEM), which reveals the channel lengths and widths even after the top gate metal is deposited. Supplementary Fig. 18 shows two exemplary *Type B* devices with channel lengths of ~60 nm and ~400 nm. Note that the surface consists of Au across the whole area displayed since everything is covered with the top gate. Nevertheless it is possible to discern the edges where the MoS_2 has been etched. The MoS_2 etch mask consists of 2 µm wide metal leads (left and right) and photoresist covering the 1 µm wide channel region, which results in no discernable edge across the MoS_2 on Au and the MoS_2 in the channel. This is consistent with the absence of "steps" in surface topography from the SEM cross-sections (Supplementary Fig. 5) and AFM images (Supplementary Fig. 4). In our EBL process, the intended channel length was 50 nm, and after evaluating Supplementary Fig. 18a, we



Supplementary Fig. 18 | SEM top-view images of *Type B* transistors. a, Device with a channel length ~60 nm. **b**, Device with a channel length ~400 nm.

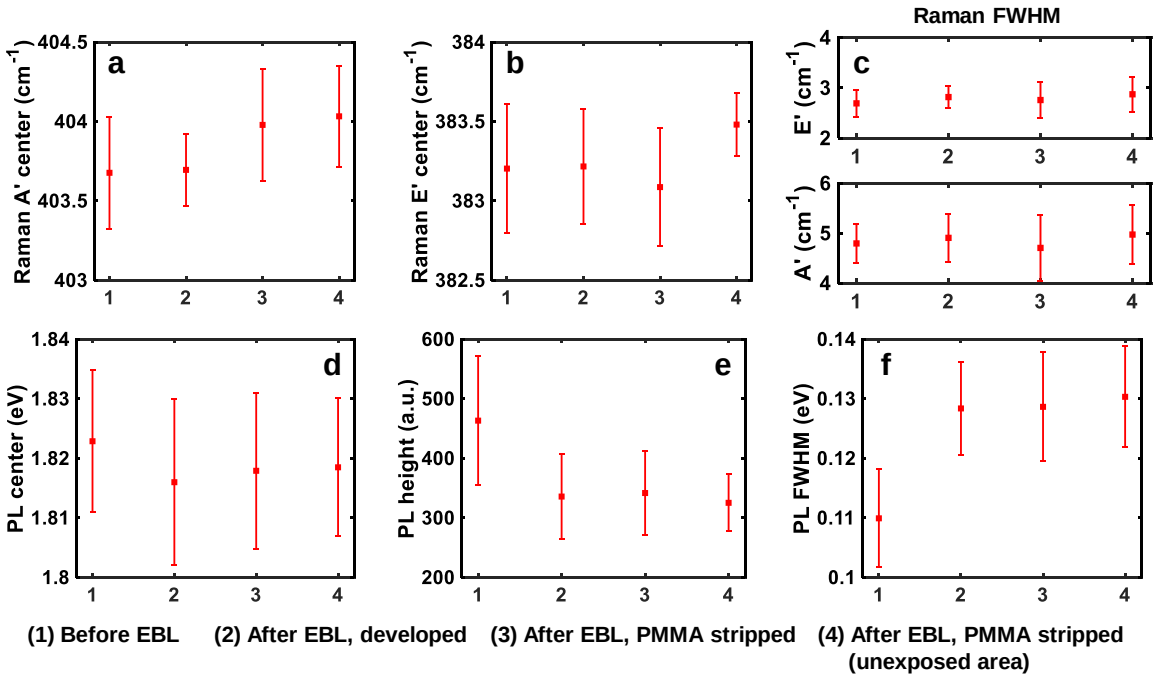


Supplementary Fig. 19 | Optical material analysis of MoS_2 throughout an electron-beam lithography (EBL) process involving spin-coating and stripping of poly(methyl methacrylate) (PMMA). a, Raman spectra. **b**, Photoluminescence spectra.

estimate its actual length is 63 ± 7 nm. Analyzing 9 devices with sub-micron channels we find that on average the channel length is ~12 nm longer than intended in our device layout. Thus, we have corrected our extractions and evaluations on devices fabricated by EBL by ΔL = +12 nm. Similarly, we applied ΔL = -0.3 µm for devices fabricated by optical lithography based on SEM measurements.

11. Electron Beam Lithography on top of MoS_2

Previous reports have indicated that MoS_2 could be damaged by highly energetic electron beams which cause strain and defect formation.[81-84] We investigated this for our EBL process (details in the Methods section) performing Raman and PL measurements before and after the electron beam exposure and development of the poly(methyl methacrylate) (PMMA) layer that was used for the lift-off of the later deposited source/drain metal. Supplementary Fig. 19 displays exemplary Raman and PL spectra, while Supplementary Fig. 20 provides the analysis of Raman and PL peak center shifts as well as the changes in the intensity and FWHM of the PL spectra. We found negligible differences in the Raman spectra. The slight reduction in the PL intensity (Supplementary Fig. 19b) occurs independently of the exposure to the electron beam, and may be caused by PMMA residues or minor effects from processing and aging of the material. Thus, we conclude that here we do not cause significant damage during the EBL process, which may have been due to our 200 nm thick high molecular weight (950K) PMMA layer on top that should reduce the impact energy and dosage of electrons that hit the MoS_2. The other parameters of our EBL process and the device fabrication can be found in the Methods section.



Supplementary Fig. 20 | Averaged optical material analysis of MoS_2 during electron-beam lithography (EBL) with spin-coating and stripping of poly(methyl methacrylate) (PMMA). a, Raman A' peak center. **b**, Raman E' peak center. **c**, Averaged full-width-half-maximum (FWHM) of the Raman peaks. **d**, Photoluminescence (PL) peak center. **e**, PL peak height. **f**, PL FWHM.

12. Temperature Rise Estimates

We estimate the MoS_2 and PI substrate temperature rises in a short-channel (L ~ 82 nm, W_C = 2 μm) *Type A* MoS_2 device. This particular "hero" device was chosen because it achieved the highest power dissipation, and is therefore expected to reach the highest temperatures during device operation. The operating point simulated is V_{GS} = 16 V, V_{DS} = 1.2 V and I_D = 1.225 mA, which corresponds to the highest power (1.47 mW) demonstrated in Fig. 3f. In order to account for interface thermal resistances and various heat paths and current spreading, we perform 3D steady-state thermal finite element method (FEM) simulations, with the device geometry shown in Supplementary Fig. 21a. The 5 μm thick PI substrate is attached to a heat sink at $T_0 \approx 20$°C via photoresist (SPR 3612, Shipley), which serves as the thermal interface material. For simulations, a thermal contact resistance of 0.1 K·cm^2/W was assumed at the bottom of the PI substrate (typical of contact resistances in device packaging[85]), although the exact value has little effect on simulated peak temperatures in this case, because its contribution to the total thermal resistance is much less than the thermal resistance of the PI substrate and the device thermal circuit. The thermal conductivities of the materials used in the simulations and the thermal boundary resistances (TBR) of material pairs are given in Supplementary Table 1.

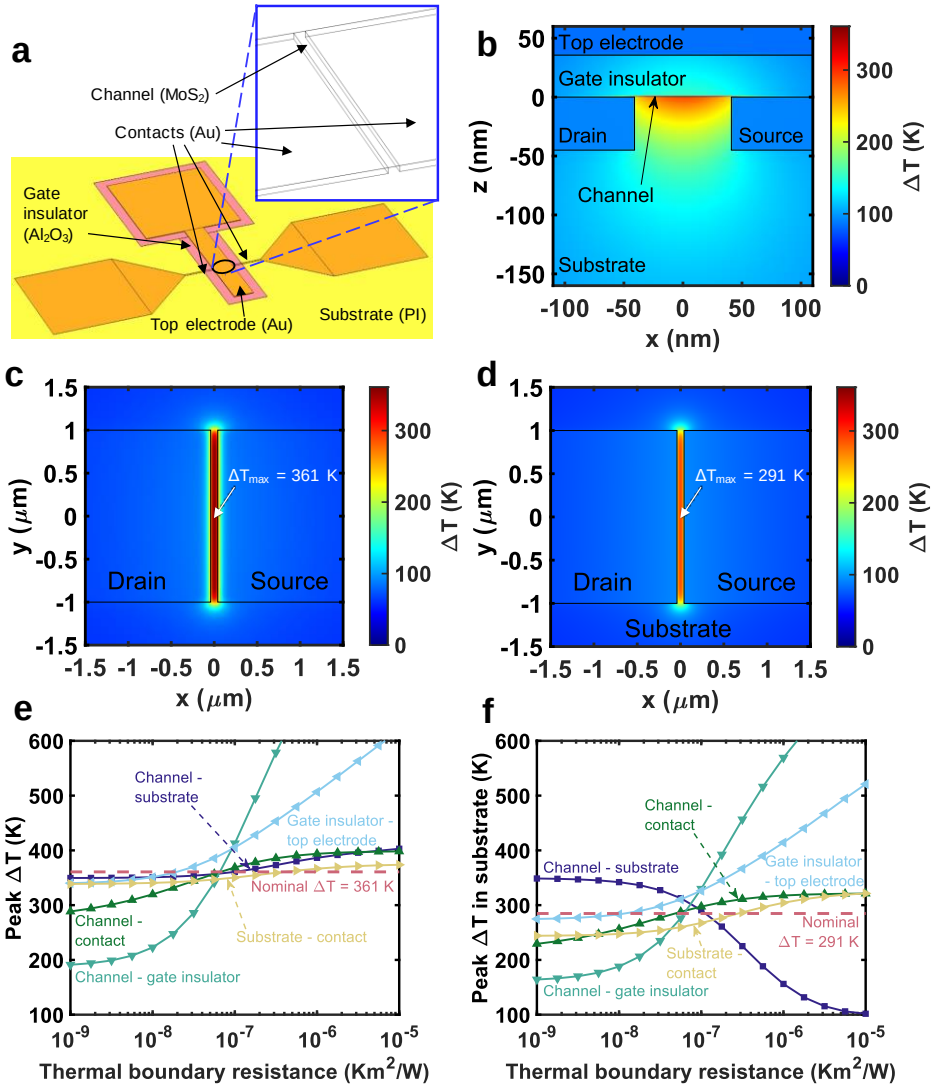
Material	Thermal conductivity ($Wm^{-1}K^{-1}$)	Material interface	Thermal boundary resistance (Km^2/GW)
MoS_2[86]	20 (in-plane)	MoS_2 – polyimide[87]	100
Polyimide (PI)[88]	0.2	MoS_2 – Au[89]	67
Au[90]	150	MoS_2 – Al_2O_3[89]	67
ALD Al_2O_3[91,92]	2.5	Au/Ti – ALD Al_2O_3[92-95]	20
		Au – polyimide[96]	400

Supplementary Table 1: Nominal values of material thermal properties in the simulations. Some thermal boundary resistance (TBR) values not available in literature were approximated by TBRs for pairs of similar and/or better-studied materials, using the larger estimates to model a worst-case scenario. Actual values can vary depending on the material/interface quality and deposition conditions. For Au, the thermal conductivity of films with comparable thickness (not bulk) is used.[90] For PI and Al_2O_3, the thermal conductivities above room temperature (in the 100-200°C range) are used.

To estimate the temperature rise, we first obtain the current distribution in the device. With $V_{DS} < V_{GS} - V_T$, the device was assumed to be in the linear region, where the MoS_2 film is characterized by a uniform sheet resistance and the current density is symmetric about the center of the device. With an assumed contact resistance of 400 Ω·μm and a contact transfer length of 50 nm (in this "hero" device), 2D electrical simulations were performed as described in Supplementary Section 15 to account for current spreading, and a mobility of 25 $cm^2V^{-1}s^{-1}$ was found to yield the correct device current. The power dissipated per unit area in the channel and across the contact interface were calculated from the simulated current densities and potential drops across the contact-MoS_2 interfaces. This power distribution was then used in the thermal simulation with the complete 3D geometry.

With the nominal thermal properties specified in Supplementary Table 1, the Supplementary Fig. 21 shows the 2D temperature rise distributions (b) in a vertical device cross section, (c) within the MoS_2 film and (d) immediately below the MoS_2 film, showing temperatures in the upper surface of the PI substrate and the Au contacts. We determine a peak temperature rise $\Delta T \sim 361$ K in MoS_2 and 291 K in PI (The difference between the two is due to the TBR between MoS_2 and PI.). Because TBRs across interfaces depend strongly on materials and the interface quality, the TBRs in the actual device might differ from the values given in Supplementary Table 1. Thus, we performed sensitivity analysis of the peak MoS_2 and PI temperature rise on the TBRs (for all interfaces), in Supplementary Fig. 21e,f.

Supplementary Fig. 21e shows that peak device temperatures are most sensitive to channel-gate insulator (MoS_2-Al_2O_3) and gate insulator-top electrode (Al_2O_3-Ti/Au) TBRs, which indicates that TBRs that control heat flow into the gate stack have the greatest influence. This also indicates the heat



Supplementary Fig. 21 | Thermal simulations. a, Simulated *Type A* device geometry. Inset: closer view of the channel, with the top gate stack not shown. **b**, Cross section of temperature rise along the direction of current flow. Note the gate has significant overlap with the source/drain. **c**, Top view of temperature rise in the MoS_2 channel, where the highest temperatures occur. **d**, Top view of temperature rise at the top of the PI substrate and Au contacts, just below the MoS_2 channel. **e**, The variation of the device peak temperature rise as a function of the TBR of each material pair. **f**, The variation of the highest temperature rise in the PI substrate as a function of the TBR of each material pair. In **e** and **f** the horizontal dashed lines indicate the peak temperature rise, and the intersection of each curve with this line occurs at each nominal TBR value.

generated in the device spreads (at first) mainly through the gate stack, which has substantial overlap (~10 μm) with the source/drain electrodes. As the heat sink is at the bottom of the PI substrate, after spreading via the gate insulator and top gate, the heat flows back down into PI via MoS_2 and the Au contacts. We note that only ~10% of the heat flows from MoS_2 directly into the PI (the channel-substrate TBR), thus even if the PI surface were severely compromised (e.g. due to heating during

device operation), the device could continue to function by dissipating heat into the gate and contacts. The PI glass transition temperature[97] is 360°C and the decomposition temperature is 620°C. Thus, for the nominal properties in Supplementary Table 1, these devices have additional headroom to operate at higher power, thanks to heat spreading through their gate and source/drain electrodes.

13. Additional *Type A* Device Data and Overall Variability

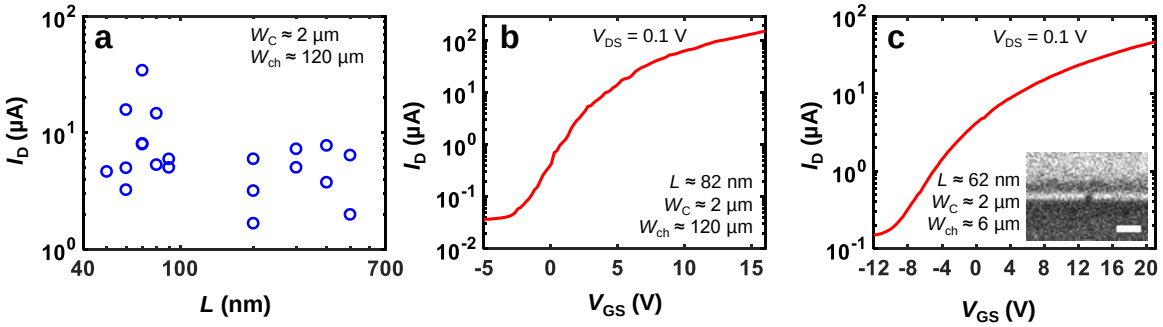
The variability of I_D for *Type A* devices shows a similar distribution compared to devices of *Type B* (compare Supplementary Fig. 22a with Fig. 3d). The transfer characteristic of the device with the highest on-current is displayed in Supplementary Fig. 22b. The shortest channel lengths which we realized were ~60 nm and an exemplary electrical characteristic and scanning-electron microscopy cross-section are shown in Supplementary Fig. 22c.

In Supplementary Fig. 23 we display the V_T histogram for all MoS_2 devices measured. Academic fabrication and growth variations (e.g., variations in S vacancy concentration[98,99]) cause V_T variability, which could be much improved with industrial process optimization (beyond the scope of this work).

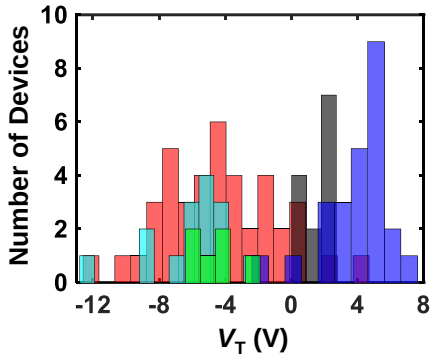
14. Drain current vs channel length in flexible MoS_2 FETs and Modeling

The drain current I_D that is obtained when probing a short-channel FET typically has contributions from the channel resistance R_{ch} and contact resistance R_C, which makes the accurate extraction of the intrinsic mobility μ_{FE} difficult. Furthermore, since short-channel devices can be contact dominated, an estimation of R_C is also important. Taking into account R_{ch} and equal source and drain R_C we can estimate the overall resistance R_{tot} (all normalized by device width W, in units Ω·m) as follows:

$$R_{tot}/W = 2R_C/W + R_{ch}/W.$$



Supplementary Fig. 22 | MoS_2 *Type A* transistors. **a**, Drain current I_D vs. channel length at a drain-source voltage V_{DS} = 0.1 V and an overdrive voltage $V_{GS} - V_T$ = 8 V. **b**, I_D vs. V_{GS} of the device with the highest on-current (also see Fig. 3f). **c**, Electrical characteristic of a *Type A* flexible MoS_2 field-effect transistor with the shortest channel length of ~60 nm. Inset shows a scanning electron microscopy cross-section of such a ~60 nm channel. Scale bar: 200 nm.



Supplementary Fig. 23 | Threshold voltage (V_T) variability of all flexible MoS_2 FETs. V_T extracted with the linear extrapolation method. Most data are for EOT ~16.4 nm and some data for EOT ~13.7 nm (black). The different colors indicate separate growth and fabrication runs. We measured~100 *Type A* and *Type B* devices, and the geometry, process flows or channel length did not discernably correlate with any V_T changes.

In the linear transistor operating region (at small V_{DS}), R_{ch} can be approximated as

$$R_{ch} = \frac{V_{DS}}{I_D} W \approx \frac{L}{\mu_{FE} C_{ox} (V_{GS} - V_T)},$$

where I_D, L, μ_{FE}, C_{ox}, V_{GS} and V_T are the drain current, channel length, intrinsic field-effect mobility, gate oxide capacitance per unit area, gate-source voltage and threshold voltage, respectively. Hence, taking into account R_{tot} when measuring the drain current ($I_{D,meas}$) while applying a voltage between drain and source ($V_{DS,appl}$), we obtain the following for $I_{D,meas}$ (normalized by W, unit: A m^{-1}):

$$I_{D,meas} = \frac{V_{DS,appl}}{R_{tot}} = \frac{V_{DS,appl}}{2R_C + \frac{L}{\mu_{FE} C_{ox} (V_{GS} - V_T)}}.$$

Thus, we have an expression for $I_{D,meas}$ where the denominator has two competing components which limit the maximum $I_{D,meas}$ that can be obtained. Further, we can find that for ultra-scaled transistors in the limit $L \rightarrow 0$, the maximum $I_{D,meas}$ is fully limited by R_C. In contrast, at long channel devices (here, $L \geq 10$ µm) the R_C no longer has significant impact and $I_{D,meas}$ is mainly defined by μ_{FE}, given the electrostatics and carrier concentration are fixed (C_{ox}, V_{GS} and V_T constant).

In the following, we use this model to identify lower and upper bounds for R_C and μ_{FE} based on our experimentally obtained results in flexible MoS_2 FETs with channel lengths ranging from ~10 µm down to ~60 nm. For that we extract $I_{D,meas}$ at V_{DS} = 0.1 V (Fig. 3d) at an overdrive gate voltage (V_{ov} = $V_{GS} - V_T$ = 8 V) using a V_T extracted from a linear fit of g_m vs V_{GS}. In addition, our model needs C_{ox}, which in this case is 0.21 µF cm^{-2} or EOT ~16.4 nm (Supplementary Fig. 12a). With that, we can use

R_C and μ_{FE} as fitting parameters. We obtain upper bounds for R_C = 2.3 kΩ µm and μ_{FE} = 27 $cm^2V^{-1}s^{-1}$ for *Type B* devices. Taking into account also the best Type A devices, the upper bounds become R_C = 0.25 kΩ µm and μ_{FE} = 30 $cm^2V^{-1}s^{-1}$ indicating a remarkably reduced R_C for the *Type A* device at L ~82 nm. Furthermore, it becomes evident that at channel lengths of ~10 µm the devices are dominated by μ_{FE} as changes in R_C do not significantly impact I_D (dotted blue and solid black lines converge in Fig. 3d). This gives us the opportunity to fix the μ_{FE} range at L ~10 µm and then subsequently fit R_C to the highest data points at the smallest channel lengths, where R_C has a larger impact then μ_{FE}, which gives us an estimate for the best R_C. We performed the fitting at V_{DS} = 0.1 V (Fig. 3d) to ensure that the devices are in the linear operating regime. We show in Fig. 3c,f that the devices with the highest I_D display effects of self-heating and velocity saturation even below V_{DS} values that would warrant channel pinch-off, which can be commonly observed for sub-100 nm channel length in MoS_2 FETs.[7,39] However, this does not impact our model because we only use it at low V_{DS}. The model can also be used to predict the extrinsic field-effect mobility $\mu_{FE,ext}$. The above equations can be modified to:[40]

$$\mu_{FE,ext} = \frac{\mu_{FE}}{1+\frac{\mu_{FE}C_{ox}(V_{GS}-V_T)2R_C}{L}}.$$

We used the same input parameters (R_C and μ_{FE}) for $\mu_{FE,ext}$ as for our I_D fitting. The result shown in Fig. 3e agrees with our extracted $\mu_{FE,ext}$ based on the maximum g_m method, confirming our calculations.

15. Correction for Lateral Current Spreading in *Type A* FETs

In all our TMD FETs of *Type A*, where the semiconductor width is greater than the electrode width, fringe currents can contribute non-negligibly to the total measured current depending on a number of factors including contact width and spacing, contact resistance and semiconductor mobility. In order to provide an accurate extraction and comparison of I_D and $\mu_{FE,ext}$ for *Type A* devices and estimate the fringe current effects, we define a dimensionless correction factor:

$$\mathrm{CF} = \frac{I_D}{W I_{D,1\mathrm{D}}}$$

where I_D is the total current (in µA), W is width of the contact and semiconductor overlap, and $I_{D,1D}$ is the width-normalized current (in µA μm^{-1}) in a FET with the same electrical parameters (sheet and contact resistances) but a channel geometry without current spreading. For FETs without a well-defined patterned channel, CF > 1, reflecting the contribution of fringe currents. In the linear regime of the transistor, given R_C, μ_{FE} and bias voltages; $I_{D,1D}$ can be calculated as $V_{DS}\cdot W^{-1}\cdot R_{tot}^{-1}$, with R_{tot}

calculated as defined in the previous section. I_D depends on the device and contact geometry as well: we estimate it using 2D finite element method (FEM) simulations using COMSOL Multiphysics to calculate the current distribution. With CF so obtained, width-normalized corrected currents are then

$$I_{D.corr} = \frac{1}{\mathrm{CF}} \frac{I_{D,meas}}{W}.$$

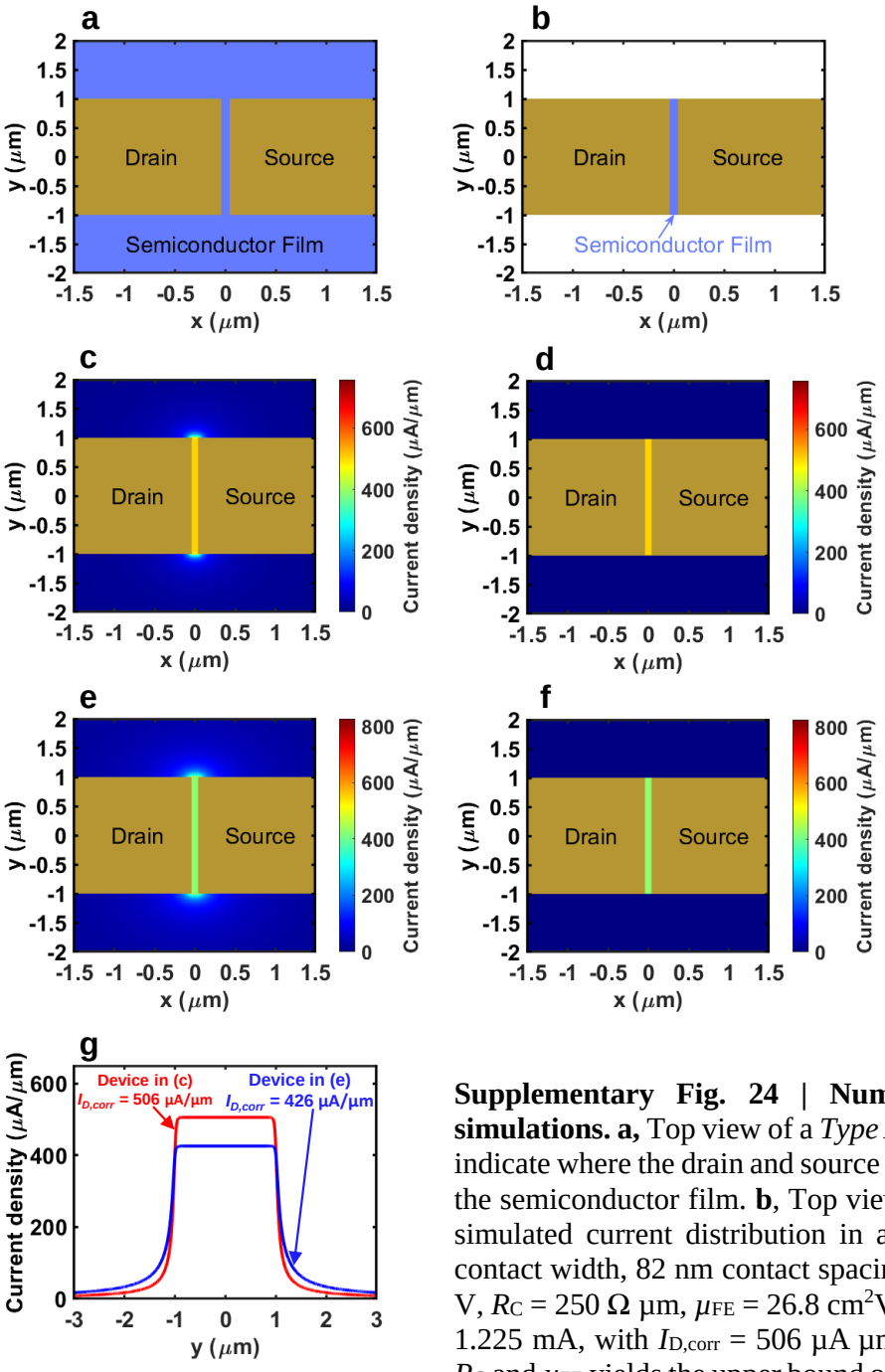
In FEM simulations, the transistor is assumed to be in the linear region of operation with $V_{DS} \ll V_{GS} - V_T$, so the semiconductor sheet resistance is assumed to be the same everywhere (except where the semiconductor overlaps with contacts), and given by

$$R_{sh} = \frac{1}{\mu_{FE} C_{ox} (V_{GS} - V_T)}.$$

For purposes of calculating this current distribution, the contacts are assumed to be edge contacts[100] with a contact resistance per unit width of R_C. The edge contact assumption is equivalent to contacts with current transfer length[24] $L_T < 50$ nm.

The two unknown electrical parameters that influence CF are μ_{FE} and R_C. However, for devices without a patterned channel, it is not straightforward to extract these directly from electrical data while simultaneously correcting for fringe currents: a range of CF are possible for different combinations of μ_{FE} and R_C. For the lower end of this range, we assume an $R_C = 250\ \Omega\ \mu m$ (best prior reported results for CVD MoS_2 with Au contacts),[28] and fit μ_{FE} to get the measured I_D. For the upper CF estimate, we assume μ_{FE} about 2-fold higher than in our best devices (for CVD MoS_2 a similar value to best prior results on silicon)[28] resulting in $\mu_{FE} = 56\ cm^2V^{-1}s^{-1}$ for MoS_2, $5\ cm^2V^{-1}s^{-1}$ for $MoSe_2$ and $10\ cm^2V^{-1}s^{-1}$ for WSe_2, then fit R_C to get the measured I_D. The range of CF calculated this way yields a range of $I_{D,corr}$ and $\mu_{FE,ext}$, which is illustrated as vertical bars in e.g., Figs. 3d and 3e.

An example for the current spreading correction is displayed in Supplementary Fig. 24 for an 82 nm long MoS_2 FET. The FEM simulation result displays the current flow paths for two different scenarios of fitted R_C/μ_{FE} (Supplementary Figs. 24c,e). It is visible that the spreading is more pronounced for the scenario with higher μ_{FE} and higher R_C. In Supplementary Figs. 24d and f, the respective I_D distributions with a hypothetical channel width = electrode width are shown which yield $I_{D,1D}$. For this device, we reported in the main manuscript the average values for these two bounds, which is ~466 $\mu A\ \mu m^{-1}$. Finally, Supplementary Fig. 24g displays the current distribution in the *y*-direction (perpendicular to the channel) at the channel center (defined as $x = 0$), which visualizes the current spreading effect for the two different fitting scenarios.



Supplementary Fig. 24 | Numerical current spreading simulations. a, Top view of a *Type A* device. The regions in gold indicate where the drain and source electrodes are in contact with the semiconductor film. **b**, Top view of a *Type B* device. **c**, The simulated current distribution in a *Type A* device with 2 μm contact width, 82 nm contact spacing, $V_{GS} - V_T$ = 10 V, V_{DS} = 1 V, R_C = 250 Ω μm, μ_{FE} = 26.8 $cm^2V^{-1}s^{-1}$. The resulting current is 1.225 mA, with $I_{D,corr}$ = 506 μA μm^{-1} (*CF* = 1.211). This set of R_C and μ_{FE} yields the upper bound of our estimated range of $I_{D,corr}$ values. **d**, The current distribution in the corresponding *Type B* device with the same electrical parameters as in c. The width-normalized current is equal to $I_{D,corr}$ = 506 μA μm^{-1}. **e**, The simulated current distribution in a *Type A* device with 2 μm contact width, at the same bias conditions as in c but with R_C = 821 Ω μm, μ_{FE} = 56 $cm^2V^{-1}s^{-1}$. The resulting current is also 1.225 mA, with $I_{D,corr}$ = 426 μA μm^{-1} (*CF* = 1.438). This set of R_C and μ_{FE} yields the lower bound of our estimated range of $I_{D,corr}$ values. **f,** The current distribution in the corresponding *Type B* device with the same electrical parameters as in e. The width-normalized current is equal to $I_{D,corr}$ = 426 μA μm^{-1}. **g**, The current density midway between the contacts (x = 0) as a function of the y-coordinate. Red and blue curves correspond to the *Type A* devices c and e, respectively.

16. Benchmarking Tables

Reference	Synthesis method	Thickness (nm)	Length (nm)	μ_{FE} or $\mu_{FE,ext}$ ($cm^2V^{-1}s^{-1}$)	I_D at V_{DS} = 1V ($\mu A\,\mu m^{-1}$)
Kwon et al. [44]	exfoliated	30-80	7000	44.8	4.1
Chang et al. [45]	exfoliated	7.9	1000	30*	13
Yoon et al. [46]	exfoliated	3.075 (5 layers)	4000	4.7	0.3
Lee et al. [47]	exfoliated	1.845 (3 layers)	800	29	NA
Salvatore et al. [4]	exfoliated	3.5	4300	19	1.3
Yoo et al. [48]	exfoliated	66.5	8300	83.5	3
Song et al. [49]	exfoliated	79.3	22600	141.3	1.2
Cheng et al. [16]	exfoliated	1.845 (3 layers)	116	NA	48**
Cheng et al. [16]	exfoliated	1.845 (3 layers)	68	NA	135***
Ma et al. [50]	exfoliated	18.3	17500	15.5 ±15.9	0.32
Chang et al [17]	CVD	0.615 (1 layer)	750	31*	66
Amani et al. [51]	CVD	0.615 (1 layer)	13000	18.9*	0.2
Shinde et al. [32]	CVD	0.615 (1 layer)	4000	6.7 ±20	2.2
Woo et al. [52]	CVD	1.538 (2.5 layers)	10000	9	1.4
Park et al. [53]	CVD	1.23 (2 layers)	4000	17.4	0.13

Supplementary Table 2: Literature values for flexible MoS_2 field-effect transistors used to generate Figs. 4a,b. The synthesis method denotes whether the material was mechanically exfoliated or grown by chemical vapor deposition (CVD). * indicates that in these cases the field-effect mobility μ_{FE} was extracted by the y-function method and contact resistance R_C is excluded. For the other cases the method was either not specified or the transconductance g_m maximum method was used which results in an extrinsic μ_{FE} ($\mu_{FE,ext}$). The drain current I_D is in most cases specified at a drain-source voltage V_{DS} = 1 V, unless labeled: ** V_{DS} = 2 V, *** V_{DS} not specified.

Reference	Channel material	Length (nm)	on/off ratio	I_D at V_{DS} = 0.5 V ($\mu A\,\mu m^{-1}$)
Park et al. [55]	graphene	140	1.5	248
Yeh et al. [56]	graphene	200	8.8	516
Zhai et al. [54]	single-crystal silicon (c-Si)	150	6×10^7	369
Shahrjerdi et al. [43]	single-crystal silicon (c-Si)	30	2×10^5	714
Wang et al. [57]	InSnO (ITO)	160	7×10^8	34
Münzenrieder et al. [58]	InGaZnO (IGZO)	160	7.1	119
Cheng et al. [16]	MoS_2	116	2×10^6	48*
Cheng et al. [16]	MoS_2	68	10^6	135**

Supplementary Table 3: Literature values for flexible field-effect transistors with channel lengths ≤ 200 nm used to generate Fig. 4c. The drain current I_D is in most cases specified at a drain-source voltage V_{DS} = 0.5 V, unless labelled: * V_{DS} = 2V, ** V_{DS} not specified.

17. Estimation of the transit frequency

The scope of this work has been to demonstrate nanoscale flexible TMD transistors with high dc performance. The top gate, fabricated after release of the flexible substrate, is currently still limited by available process accuracy for alignment and feature size in the optical lithography on the ultra-thin flexible substrate. This leads to a large overlap area, and hence high overlap capacitance, which will

limit the ac device performance. The reduction of parasitic overlaps will be addressed in future work. Nevertheless, to evaluate the potential of our devices for high frequency applications, we calculated the expected transit frequency f_T of our transistors with highest performance. We have used the extracted $\mu_{FE,ext}$ at V_{DS} = 1 V, which lumps together material parameters (μ_{FE}) and other device parasitics (R_C), and hence we can estimate f_T, based on the following equation (adapted from other works[40,101]):

$$f_T = \frac{\mu_{FE,ext} V_{DS} C_{ox} W_{ch}}{2\pi L_{ch} C_{tot}}$$

where C_{tot} is the total capacitance and other variables were previously defined (see Supplementary Section 14). C_{tot} has several components: 1) the total gate oxide capacitance including overlaps ($C_{ox,tot}$), 2) the parasitic capacitance from the sidewall of the gate (C_{side}), and 3) the fringing parasitic capacitance from the top surface of the gate (C_{top}).

$$C_{tot} = C_{ox,tot} + 2\left(C_{side} + C_{top}\right)$$

$C_{ox,tot}$, C_{side} and C_{top} are then estimated as follows:[40,101,102]

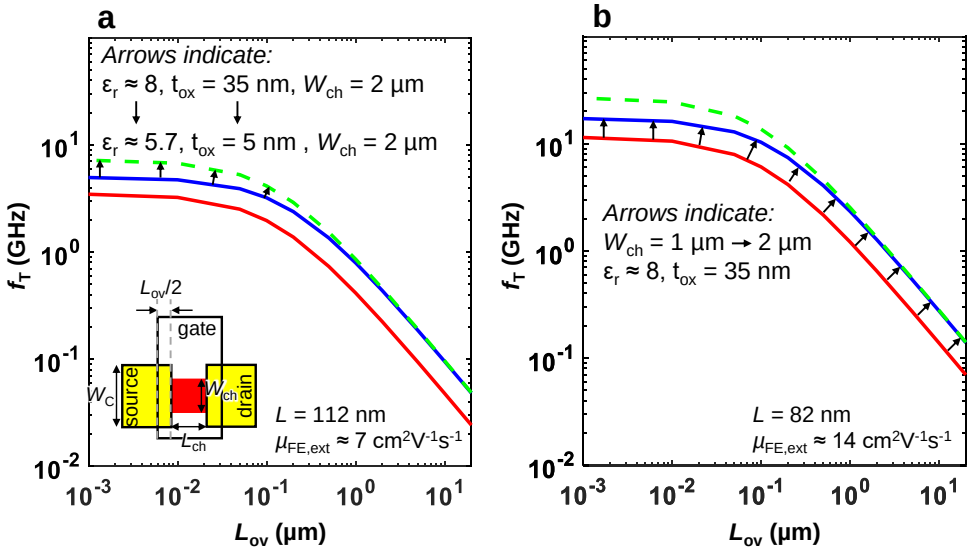
$$C_{ox,tot} = C_{ox}(L_{ch} W_{ch} + L_{ov} W_C)$$

$$C_{side} = \frac{W_C \varepsilon_0 \varepsilon_r}{\pi} ln\left[(K^2 - 1)\left(\frac{K^2}{K^2 - 1}\right)^{K^2}\right]$$

$$C_{top} = \frac{W_C \varepsilon_0 \varepsilon_r}{\pi} ln\left[1 + \frac{L_{ch} + L_{ov}}{t_{ox} + t_{gate}}\right]$$

where $K = 1 + t_{gate}/t_{ox}$ with t_{gate} as the gate metal thickness and t_{ox} as the gate oxide thickness, ε_0 as the vacuum permittivity, ε_r as the relative gate oxide permittivity, L_{ov} is the gate-source/drain overlap length (see inset of Supplementary Figure 25) and other variables were previously defined.

Thus we calculate f_T as a function of L_{ov}, which is displayed in Supplementary Figure 25 taking the corresponding dc data from the devices shown in Fig. 3c,f. Initially, we assumed similar device geometry as in our *Type B* devices with our measured $C_{ox} \approx 0.21$ µF cm^{-2}, $\varepsilon_r \approx 8$, $t_{ox} \approx 35$ nm (see Supplementary Section 5), t_{gate} = 65 nm, W_{ch} = 1 µm and W_C = 2 µm. The inset sketches the different geometrical parameters in top view. The resulting f_T is displayed in red. We find a strong dependence on L_{ov} for large overlaps > 0.1 µm where the parasitic overlap capacitance dominates. A general improvement in f_T can be expected when W_{ch} is increased to a value equal to W_C (blue lines, and arrows in Supplementary Figure 25b). In addition, decreasing the gate oxide thickness will only lead to higher f_T if gate-source/drain overlaps are minimized (< 0.1 µm, green dashed lines, and arrows in Supplementary Figure 25a). We have estimated here the case for reducing our Al_2O_3 gate dielectric thickness to 5 nm, which would lead to a lower ε_r due to interface effects and C_{ox} would become ≈ 1 µF cm^{-2}.[77,103] The maximum f_T estimated after these modifications reaches ~26 GHz, and could be increased slightly more by reducing t_{gate} which for instance would lead to ~27 GHz for t_{gate} = 15 nm.



Supplementary Fig. 25 | Calculated transit frequency f_T as a function of gate-to-source/drain overlap length L_{ov}. The calculation was done based on dc characteristics shown in **a**, Fig. 3c and **b**, Fig. 3f. The inset in **a** sketches the geometry used for the calculations.

These results indicate that the first priority should be minimizing L_{ov} which could be done by advanced lithography techniques or fabrication tricks (like self-alignment[104]). However, it should be noted that an underlapped device structure, which avoids parasitic overlap capacitance overall could significantly increase the access resistance (and R_C)[17] without a stable and reliable TMD doping technology. Thus, a careful optimization of the device geometry will be necessary. Nevertheless, our estimation of maximum f_T of ~7 GHz and ~27 GHz for the two selected devices demonstrate the potential of high frequency operation in flexible MoS_2 transistors.

Additional References

59 Lee, C. *et al.* Anomalous lattice vibrations of single-and few-layer MoS_2. *ACS Nano* **4**, 2695-2700 (2010).

60 Medina, H. *et al.* Wafer-scale growth of WSe_2 monolayers toward phase-engineered hybrid WO_x/WSe_2 films with sub-ppb NO_x gas sensing by a low-temperature plasma-assisted selenization process. *Chem. Mater.* **29**, 1587-1598 (2017).

61 Tonndorf, P. *et al.* Photoluminescence emission and Raman response of monolayer MoS_2, $MoSe_2$, and WSe_2. *Opt. Express* **21**, 4908-4916 (2013).

62 Liu, B. *et al.* Chemical vapor deposition growth of monolayer WSe_2 with tunable device characteristics and growth mechanism study. *ACS Nano* **9**, 6119-6127 (2015).

63 Plechinger, G. *et al.* A direct comparison of CVD-grown and exfoliated MoS_2 using optical spectroscopy. *Semicond. Sci. Technol.* **29**, 064008 (2014).

64 Gong, C. *et al.* Metal contacts on physical vapor deposited monolayer MoS_2. *ACS Nano* **7**, 11350-11357 (2013).

65 Wang, Y., Cong, C., Qiu, C. & Yu, T. Raman spectroscopy study of lattice vibration and crystallographic orientation of monolayer MoS_2 under uniaxial strain. *Small* **9**, 2857-2861 (2013).

66 Mukherjee, B. *et al.* Exciton emission intensity modulation of monolayer MoS_2 via Au plasmon coupling. *Sci. Rep.* **7**, 41175 (2017).

67 Schauble, K. *et al.* Uncovering the effects of Metal contacts on monolayer MoS_2. *ACS Nano* **14**, 14798-14808 (2020).
68 Ahn, G. H. *et al.* Strain-engineered growth of two-dimensional materials. *Nat. Commun.* **8**, 608 (2017).
69 Schneider, L. *et al.* The impact of the substrate material on the optical properties of 2D WSe_2 monolayers. *Semiconductors* **52**, 565-571 (2018).
70 Horzum, S. *et al.* Phonon softening and direct to indirect band gap crossover in strained single-layer $MoSe_2$. *Phys. Rev. B* **87**, 125415 (2013).
71 Chang, C.-H., Fan, X., Lin, S.-H. & Kuo, J.-L. Orbital analysis of electronic structure and phonon dispersion in MoS_2, $MoSe_2$, WS_2, and WSe_2 monolayers under strain. *Phys. Rev. B* **88**, 195420 (2013).
72 Ji, J. *et al.* Strain-modulated excitonic gaps in mono-and bi-layer $MoSe_2$. *Chinese Phys. B* **25**, 077802 (2016).
73 Mignuzzi, S. *et al.* Effect of disorder on Raman scattering of single-layer MoS_2. *Phys. Rev. B* **91**, 195411 (2015).
74 Shi, W. *et al.* Phonon confinement effect in two-dimensional nanocrystallites of monolayer MoS_2 to probe phonon dispersion trends away from brillouin-zone center. *Chinese Phys. Lett.* **33**, 057801 (2016).
75 Uemura, T. *et al.* On the extraction of charge carrier mobility in high-mobility organic transistors. *Adv. Mater.* **28**, 151-155 (2016).
76 Ortiz-Conde, A. *et al.* A review of recent MOSFET threshold voltage extraction methods. *Microelectron. Reliab.* **42**, 583-596 (2002).
77 Daus, A. *et al.* Ferroelectric-like charge trapping thin-film transistors and their evaluation as memories and synaptic devices. *Adv. Electron. Mater.* **3**, 1700309 (2017).
78 Groner, M., Elam, J., Fabreguette, F. & George, S. M. Electrical characterization of thin Al_2O_3 films grown by atomic layer deposition on silicon and various metal substrates. *Thin Solid Films* **413**, 186-197 (2002).
79 Münzenrieder, N. *et al.* Investigation of gate material ductility enables flexible a-IGZO TFTs bendable to a radius of 1.7 mm. In *2013 Proc. European Solid-State Device Research Conference (ESSDERC).* 362-365 (IEEE, 2013), DOI: 10.1109/ESSDERC.2013.6818893.
80 Lewis, J. Material challenge for flexible organic devices. *Mater. Today* **9**, 38-45 (2006).
81 Matsunaga, M. *et al.* Nanoscale-barrier formation induced by low-dose electron-beam exposure in ultrathin MoS_2 transistors. *ACS Nano* **10**, 9730-9737 (2016).
82 Zan, R. *et al.* Control of radiation damage in MoS_2 by graphene encapsulation. *ACS Nano* **7**, 10167-10174 (2013).
83 Parkin, W. M. *et al.* Raman shifts in electron-irradiated monolayer MoS_2. *ACS Nano* **10**, 4134-4142 (2016).
84 Komsa, H.-P., Kurasch, S., Lehtinen, O., Kaiser, U. & Krasheninnikov, A. V. From point to extended defects in two-dimensional MoS_2: Evolution of atomic structure under electron irradiation. *Phys. Rev. B* **88**, 035301 (2013).
85 Prasher, R. Thermal interface materials: historical perspective, status, and future directions. *Proc. IEEE* **94**, 1571-1586 (2006).
86 Gabourie, A. J., Suryavanshi, S. V., Farimani, A. B. & Pop, E. Reduced thermal conductivity of supported and encased monolayer and bilayer MoS_2. *2D Mater.* **8**, 011001 (2021).
87 Epstein, J., Ong, W.-L., Bettinger, C. J. & Malen, J. A. Temperature dependent thermal conductivity and thermal interface resistance of pentacene thin films with varying morphology. *ACS Appl. Mater. interfaces* **8**, 19168-19174 (2016).
88 Laumer, T. *et al.* Fundamental investigation of laser beam melting of polymers for additive manufacture. *J. Laser Appl.* **26**, 042003 (2014).
89 Yalon, E. *et al.* Temperature-dependent thermal boundary conductance of monolayer MoS_2 by Raman thermometry. *ACS Appl. Mater. Interfaces* **9**, 43013-43020 (2017).

90 Lugo, J. & Oliva, A. Thermal properties of metallic films at room conditions by the heating slope. *J. Thermophys. Heat Trans.* **30**, 452-460 (2016).

91 Cappella, A. *et al.* High temperature thermal conductivity of amorphous Al_2O_3 thin films grown by low temperature ALD. *Adv. Eng. Mater.* **15**, 1046-1050 (2013).

92 Paterson, J., Singhal, D., Tainoff, D., Richard, J. & Bourgeois, O. Thermal conductivity and thermal boundary resistance of amorphous Al_2O_3 thin films on germanium and sapphire. *J. Appl.Phys.* **127**, 245105 (2020).

93 Lee, S.-M. *et al.* Thermal conductivity and thermal boundary resistances of ALD Al_2O_3 films on Si and sapphire. *Int. J. Thermophys.* **38**, 176 (2017).

94 Chien, H.-C., Yao, D.-J. & Hsu, C.-T. Measurement and evaluation of the interfacial thermal resistance between a metal and a dielectric. *Appl. Phys. Lett.* **93**, 231910 (2008).

95 Olson, D. H., Freedy, K. M., McDonnell, S. J. & Hopkins, P. E. The influence of titanium adhesion layer oxygen stoichiometry on thermal boundary conductance at gold contacts. *Appl. Phys. Lett.* **112**, 171602 (2018).

96 Miyazaki, K., Kuriyama, K. & Yabuki, T. Printable Thermoelectric Device. In *J. Phys. Conf. Ser.* 012057 (IOP Publishing).

97 *Parameters to make Polyimide Film (PI-2600) with Thickness more than 100 um*, <https://www.researchgate.net/post/Parameters_to_make_Polyimide_Film_PI-2600_with_Thickness_more_than_100_um> (accessed July 28, 2020).

98 Leong, W. S. *et al.* Tuning the threshold voltage of MoS_2 field-effect transistors via surface treatment. *Nanoscale* **7**, 10823-10831 (2015).

99 Kim, I. S. *et al.* Influence of stoichiometry on the optical and electrical properties of chemical vapor deposition derived MoS_2. *ACS Nano* **8**, 10551-10558 (2014).

100 Szabó, Á., Jain, A., Parzefall, M., Novotny, L. & Luisier, M. Electron transport through metal/MoS_2 interfaces: edge-or area-dependent process? *Nano Lett.* **19**, 3641-3647 (2019).

101 Klauk, H. Will we see gigahertz organic transistors? *Adv. Electron. Mater.* **4**, 1700474 (2018).

102 Suzuki, K. Parasitic capacitance of submicrometer MOSFET's. *IEEE Trans. Electron Devices* **46**, 1895-1900 (1999).

103 English, C. D., Smithe, K. K., Xu, R. L. & Pop, E. Approaching ballistic transport in monolayer MoS_2 transistors with self-aligned 10 nm top gates. In *2016 IEEE International Electron Devices Meeting (IEDM).* 5.6. 1-5.6. 4 (IEEE), DOI: 10.1109/IEDM.2016.7838355.

104 Münzenrieder, N. *et al.* Flexible self-aligned amorphous InGaZnO thin-film transistors with submicrometer channel length and a transit frequency of 135 MHz. *IEEE Trans. Electron Devices* **60**, 2815-2820 (2013).