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Supplementary information

Graphene-assisted metal transfer printing for wafer-scale integration of metal electrodes and two-dimensional materials

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Supplementary Information

Graphene-assisted metal transfer printing for wafer-scale integration of metal electrodes and two-dimensional materials

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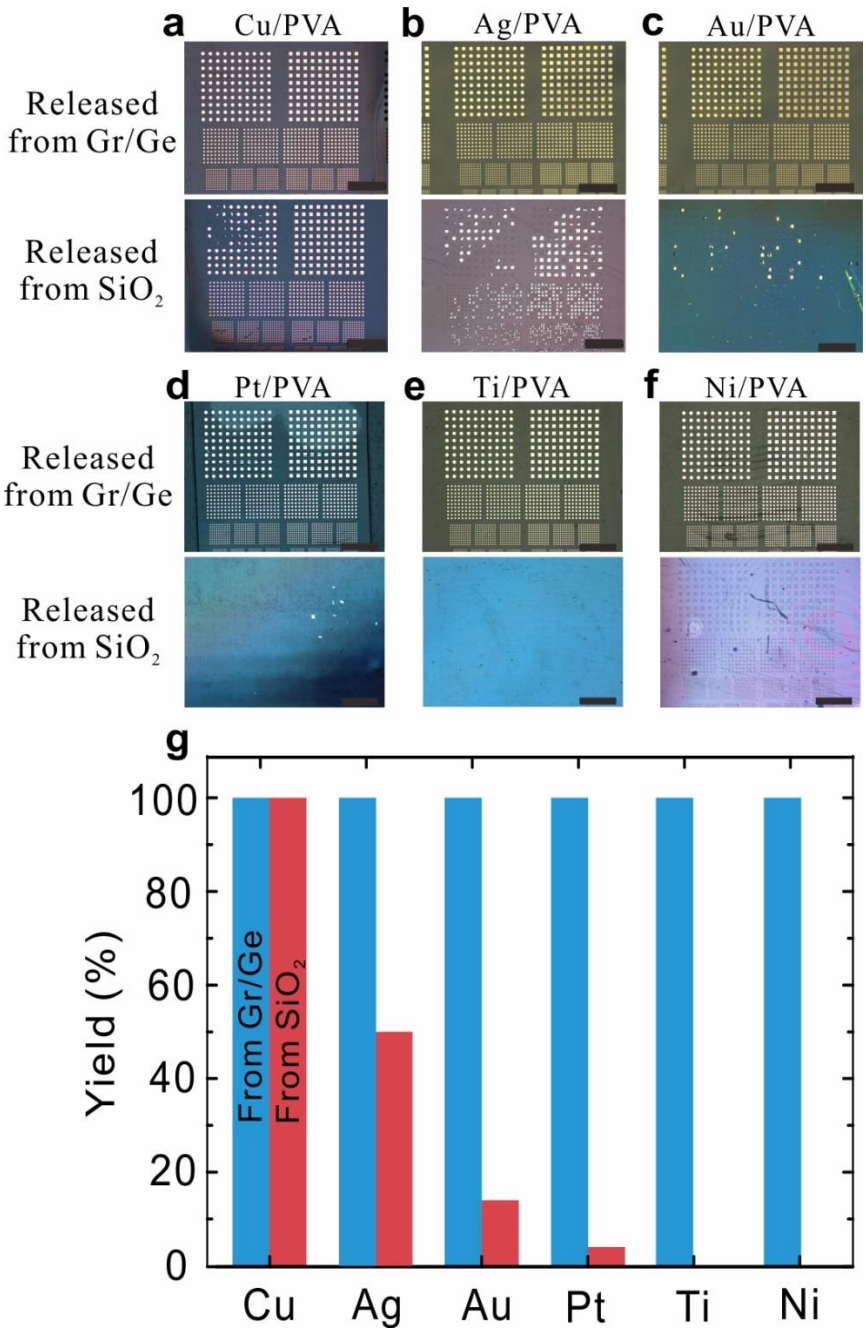
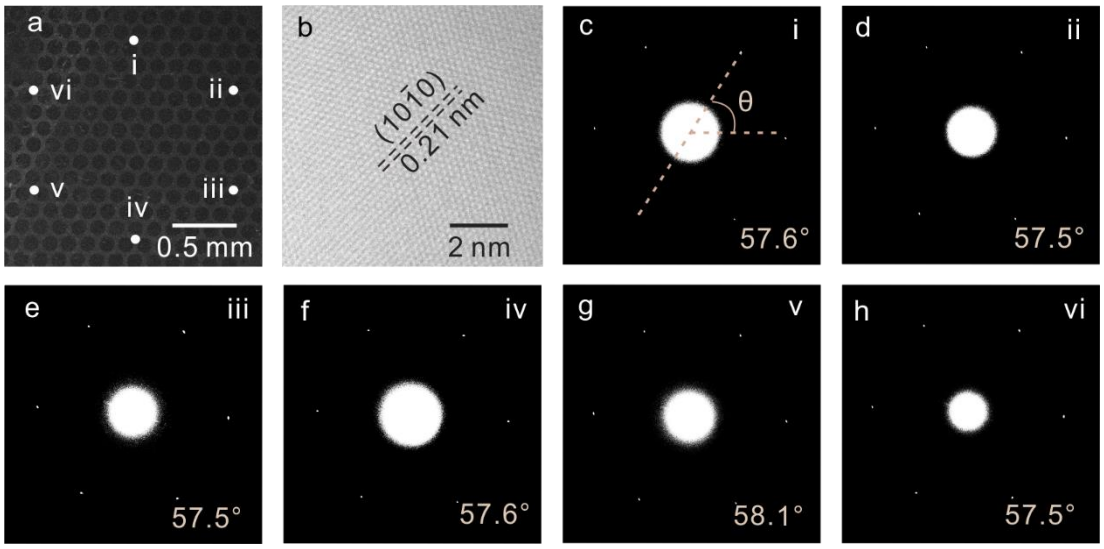


Supplementary Figure 1. (a-f) Optical images of **(a)** Cu, **(b)** Ag, **(c)** Au, **(d)** Pt, **(e)** Ti, and **(f)** Ni contacts transferred onto the PVA films from the Gr/Ge and SiO_2 substrates, respectively (Scale bars: 1 mm); **g** Statistical yields of various metal contacts transferred from the Gr/Ge and SiO_2 substrates to PVA films.

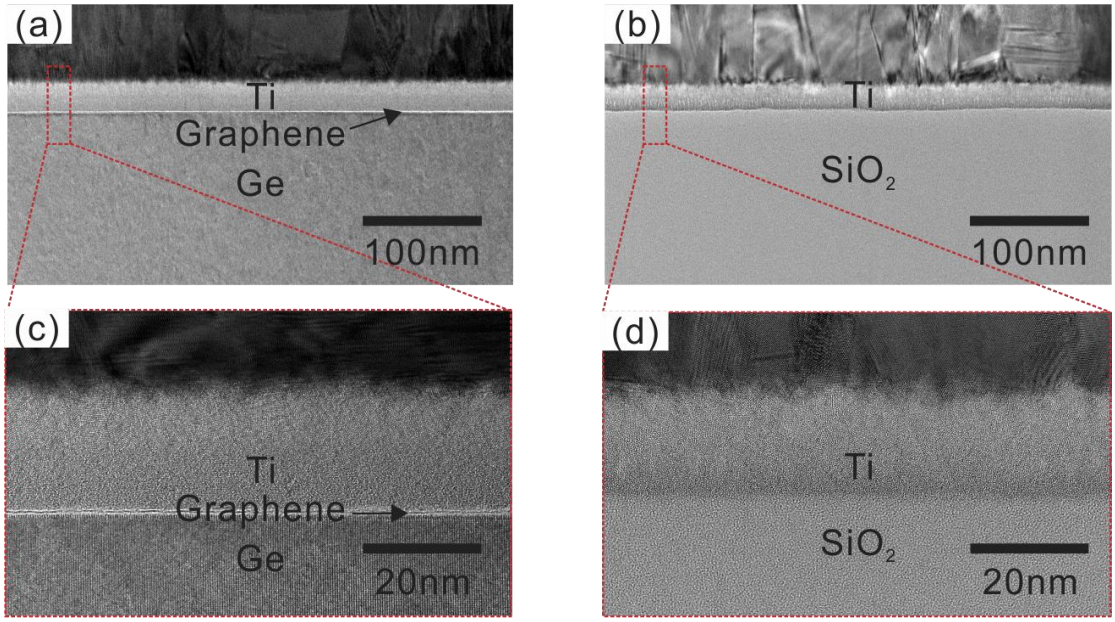
The peeling tests for different metals are conducted on both Gr/Ge and SiO_2 substrates and the yields for different metals transferred onto the PVA film are

compared. The metal pattern consists of several 10×10 matrices of circles and squares with different sizes. In the statistical analysis of the transfer yield, the number of 100 μm squares (top right corner of the pattern) transferred completely onto PVA is counted. With regard to weakly adhering metals including Cu, Ag, and Au, the transfer yield onto Gr/Ge for all the patterns is 100%, as shown in **Supplementary Figures 1 (a-c**). However, the yield decreases when the substrate is changed from Gr/Ge to SiO_2. In particular, the transfer yield of Ag and Au from SiO_2 is lower than that of Cu. Although the transfer yield of the Cu metal contact is high, it is relatively difficult to transfer Cu patterns with a circular shape compard to those with a square shape. For the strongly adhering metals such as Pt, Ti and Ni, the transfer yield of all the patterns from Gr/Ge is 100%, as shown in **Supplementary Figures 1 (d-f)**. In contrast, the transfer yields of Pt, Ti, and Ni from SiO_2 are 4%, 0%, and 0%, respectively. Supplementary Figure 1g shows that metal patterns transfer from Gr/Ge are more efficient than that from SiO_2.



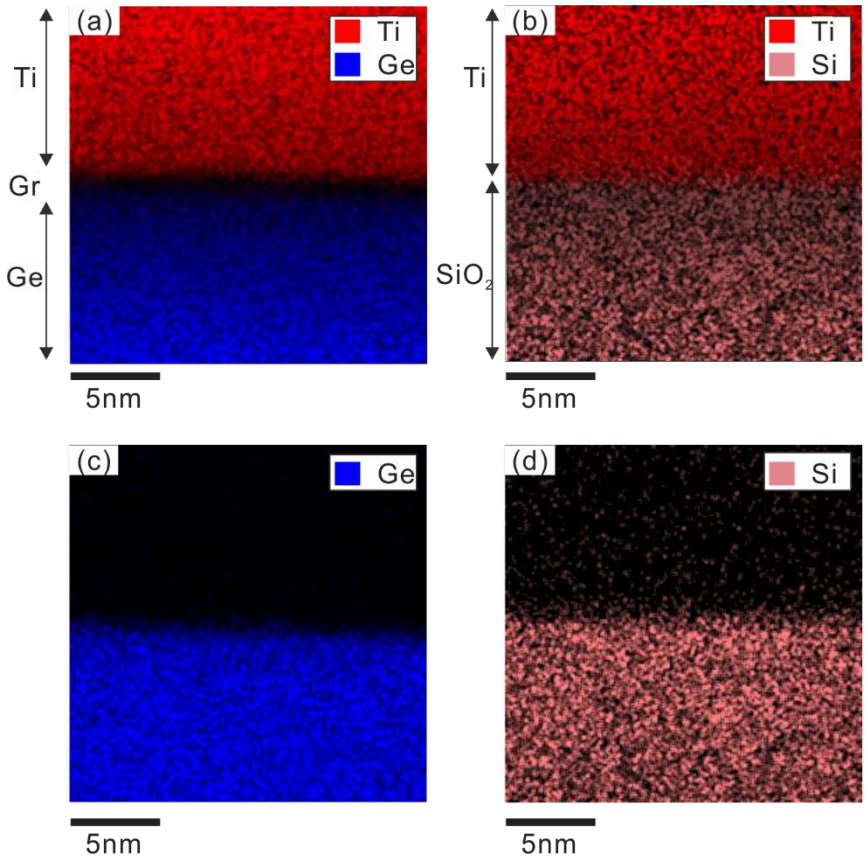
Supplementary Figure 2. **(a)** SEM image of large area monolayer graphene film tramsferred on a TEM grid. **(b)** HRTEM image of single-crystal graphene. The d-spacing of (10$\bar{1}$0) plane is 0.210 nm. **(c-h)** SAED patterns taken from six representative regions marked in **(c)**. The orientations of the diffraction patterns (θ) are mainly distributed at ~57.6° among six SAED patterns.

Supplementary Figure 2 (a) shows scanning electron microscope (SEM) image of the large area monolayer graphene film on a transmission electron microscopy (TEM) grid. The honeycomb structure of graphene is revealed by high resolution TEM (HRTEM) image, as shown in **Supplementary Figure 2 (b)**. In addition, d-spacing of 0.21 nm at (10$\bar{1}$0) plane is in good agreement with the lattice parameter of graphene.[1] The selected area electron diffraction (SAED) patterns (**Supplementary Figure 2 (c-h)**) are taken from six representative regions across 2mm×2mm marked as i-vi in **Supplementary Figure 2 (a)**. It is found that all six SAED patterns share the similar set of six-fold symmetric diffraction spots. In addition, the rotation angles of six diffraction patterns are mainly distributed at ~57.6°, which affirms the single-crystalline property of graphene grown on Ge (110) substrate.[1]



Supplementary Figure 3. Low-magnification TEM images collected from broad areas near **(a)** Ti/Gr/Ge interface and **(b)** Ti/SiO_2 interface. **(c)** and **(d)** shows the magnified cross-sectional view of **(a)** and **(b)**, respectively.

Low-magnification TEM images collected from broad areas near Ti/Gr/Ge interface and Ti/SiO_2 interface have been shown in **Supplementary Figure 3**. **Supplementary Figure 3 (a)** and **(c)** demonstrate Ti/Gr/Ge multilayer with an atomically clean and sharp interface, which suggests the complete suppression of interfacial products formation. In contrast, the interface of Ti/SiO_2, shown in **Supplementary Figure 3 (b)** and **(d)**, is not distinct and a transition layer seems to be formed due to the inter-diffusion between Ti layer and SiO_2 layer.



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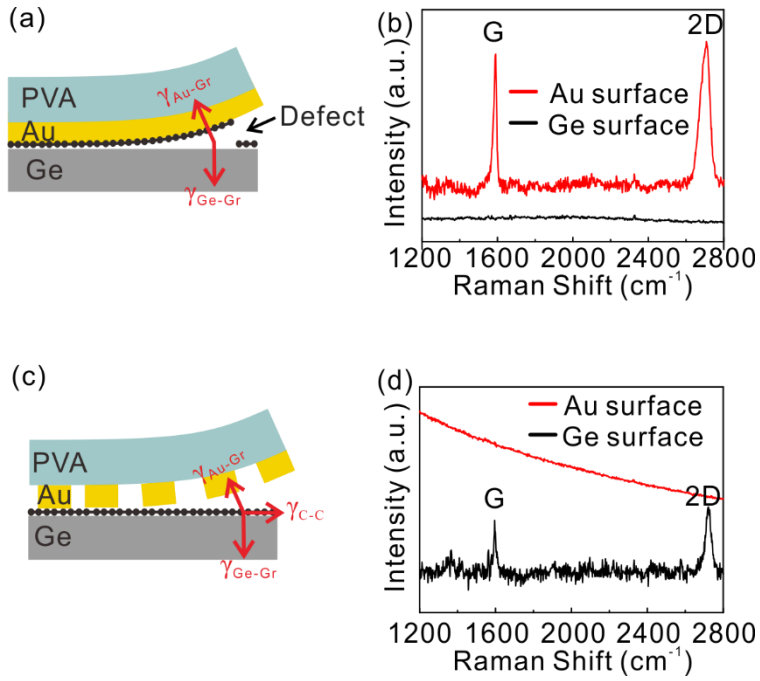
101 **Supplementary Figure 4.** EDS mapping images of **(a)** Ti/Gr/Ge interface and **(b)**
102 Ti/SiO_2 interface. **(c)** Ge and **(d)** Si atom distributions near Ti/Gr/Ge interface and
103 Ti/SiO_2 interface, respectively.

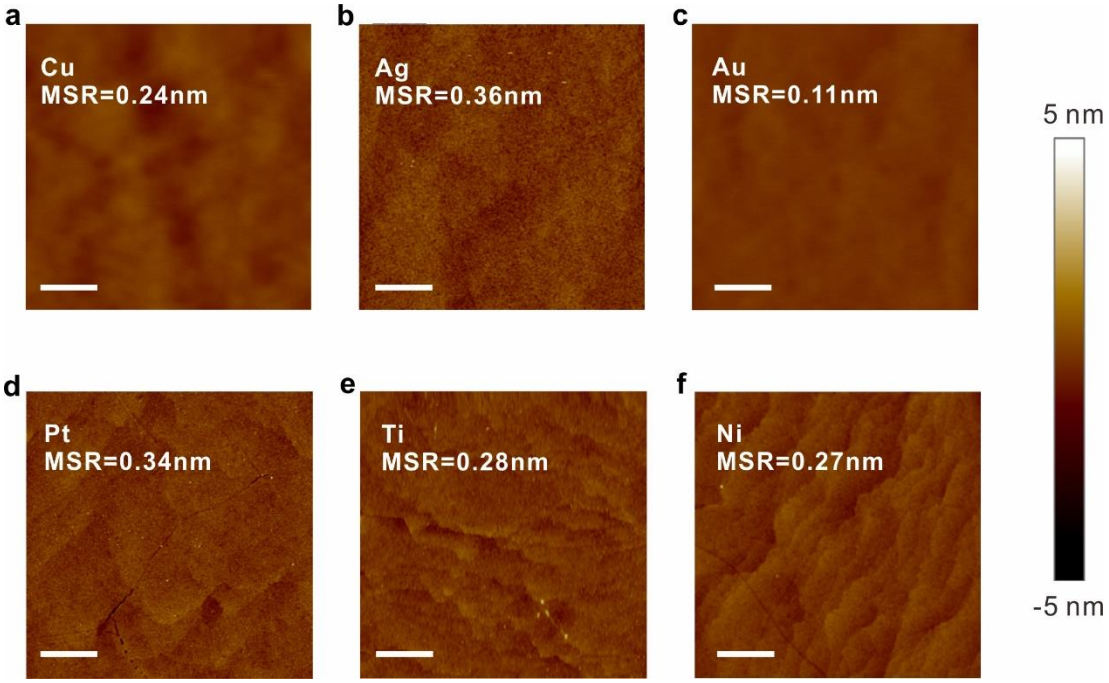
104 The EDS mapping across the interface regions of Ti/Gr/Ge and Ti/SiO_2 are shown in
105 **Supplementary Figure 4 (a)** and **(b)**, respectively. It is apparent that, due to the
106 impermeability of graphene, the inter-diffusion between Ti layer and Ge substrate is
107 fully suppressed and no interfacial products are formed, as shown in **Supplementary**
108 **Figure 4 (a)**. In contrast, the Ti/SiO_2 interface is blurred in **Supplementary Figure 4**
109 **(b)**. The severe inter-diffusion occurring at Ti/SiO_2 is evident by the considerable
110 amount of Si atoms diffused into the Ti layer, as suggested by the comparison
111 between **Supplementary Figure 4 (c)** and **(d)**.



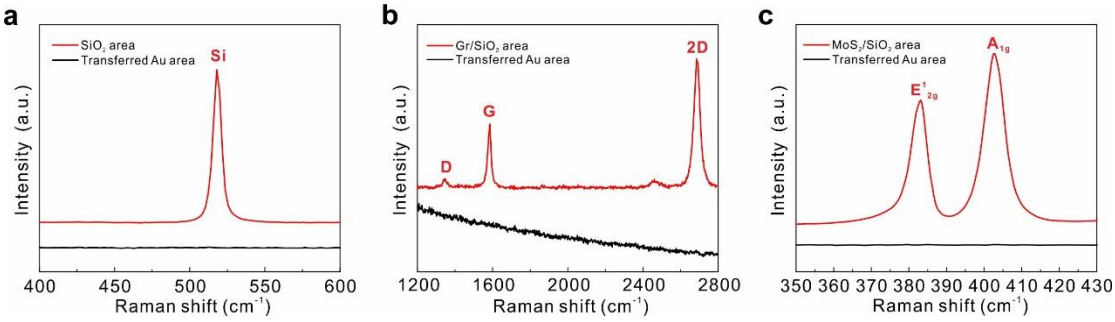
Supplementary Figure 5. (a) Schematical drawing of large-area Au film exfoliated from Gr/Ge substrate with graphene delamination. **(b)** Raman spectra collected from PVA/Au/Gr and Ge substrate after large-area Au film exfoliation. **(c)** Schematical drawing of Au patterns exfoliated from Gr/Ge substrate without graphene delamination. **(d)** Raman spectra collected from PVA/Au and Gr/Ge substrate after Au pattern exfoliation.

In the case of large-area Au film deposited on Gr/Ge, as shown in **Supplementary Figure 5 (a)**, the crack tip easily extends to the Gr-Ge interface from the defective area near the substrate edge. With the propagation of exfoliation process, the graphene can be exfoliated from Ge substrate along with Au film. The Raman spectra shown in **Supplementary Figure 5 (b)** also suggest that graphene is adhered to the Au film after peeled off by PVA, while Ge substrate returns to the pristine state. On the contrary, as wafer-scale Au film changes into Au patterns, the total adhesion energy between Au pattern and graphene is significantly reduced and no longer able to break C-C bonds in graphene, the crack propagation process is prohibited, as schematically drawn in **Supplementary Figure 5 (c)**. Therefore, the graphene will still attach to Ge substrate without any exfoliation after Au patterns are peeled off by PVA, as evident

by Raman spectra shown in **Supplementary Figure 5 (d)**. It should be noted that single crystalline graphene used in our study may be essential for the successful transfer of Au patterns without graphene delamination from Ge substrate, since the defect density of single crystalline graphene is extremely low and insufficient to initiate the crack propagation process. Considering graphene can be transferred with wafer-scale Au film from Ge substrate by PVA, therefore, there should exist critical size for Au pattern with the desired shape, below which Au patterns can be successfully transferred from Gr/Ge by PVA without delamination of graphene. The relevant study needs to be explored in the future. For certain, Au patterns with regular shape smaller than the critical size can be successfully transferred without graphene delamination by PVA, as demonstrated in our study.

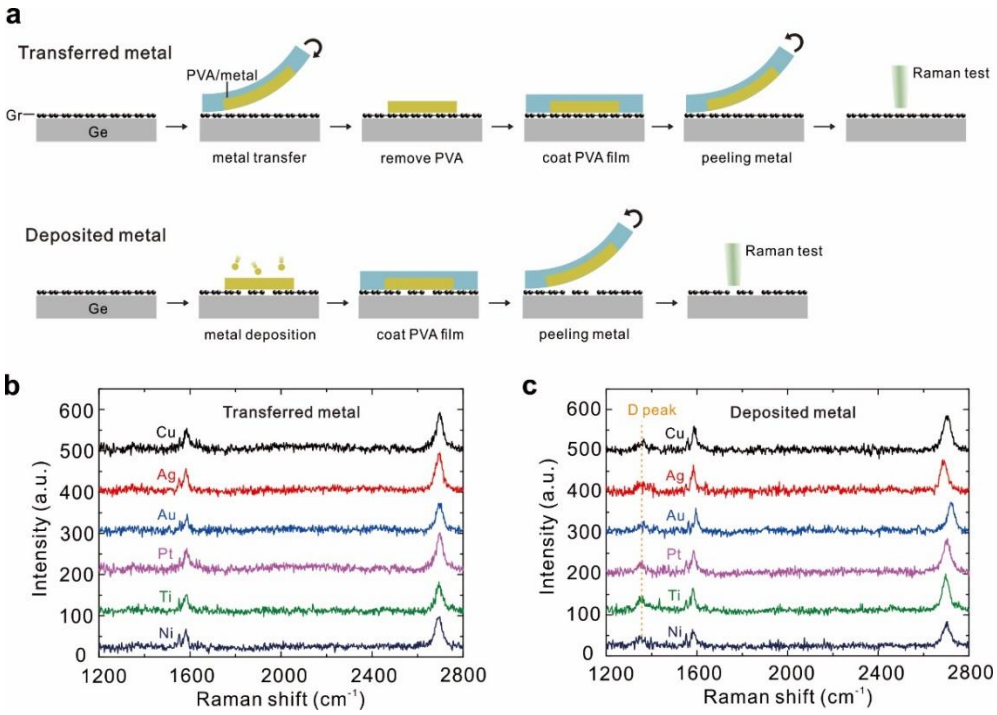


Supplementary Figure 6. Atomic force microscopy images of different metals transferred from the Gr/Ge substrate to SiO_2 substrate. Scale bars: 1 μm. Inherited from the ultra-flat surface of Gr/Ge substrate, the transferred metal strips including Cu, Ag, Au, Pt, Ti and Ni possess atomically flat surfaces with extremely low roughness, and the corresponding values of morphological surface roughness are lower than 0.4 nm.



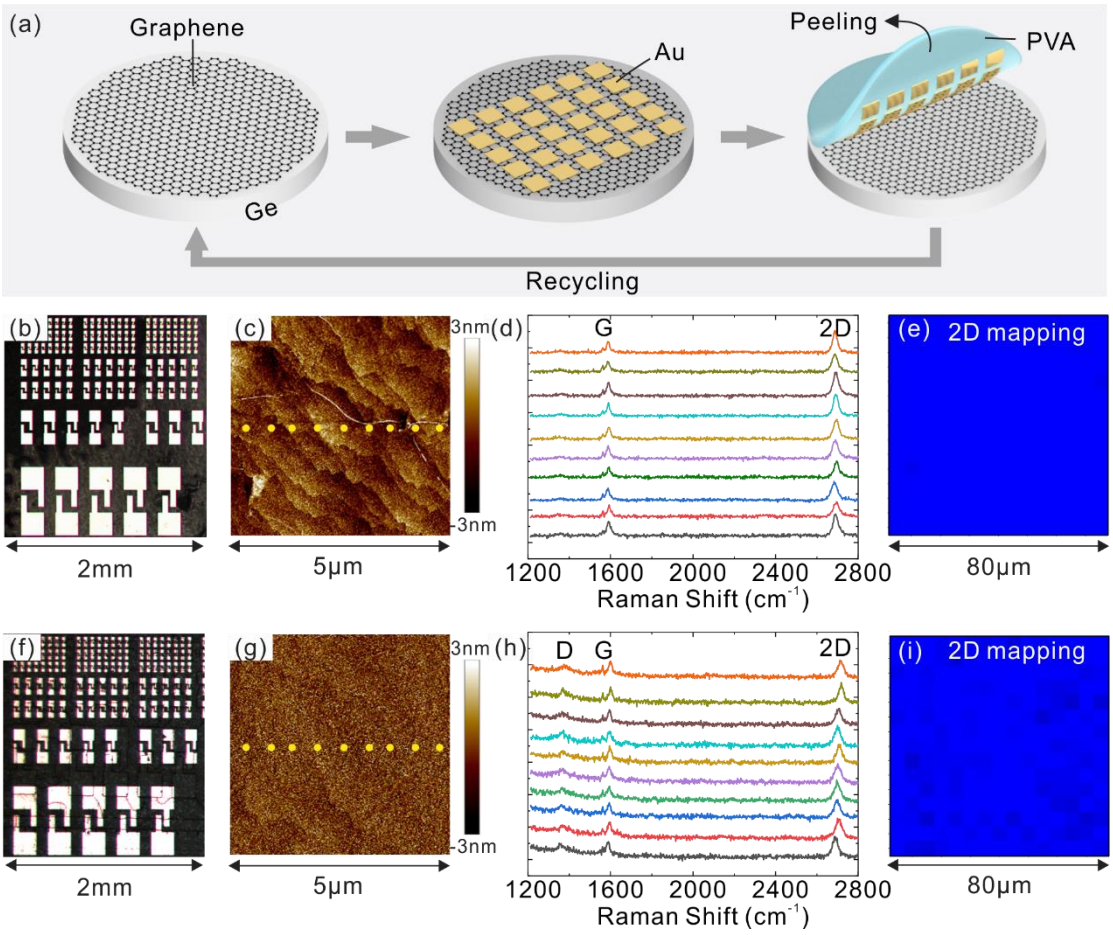
Supplementary Figure 7. (**a-c)** Raman scattering spectra acquired the pristine area and areas with transferred Au patterns of **(a)** SiO_2, **(b)** Gr/SiO_2, and **(c)** and MoS_2/SiO_2.

For SiO_2 substate, the 514nm laser can penetrate the top SiO_2 layer and Raman signal can be detected from Si underneath (**Supplementary Figure 7(a)**). The characteristic peaks corresponding to graphene and MoS_2 can also be observed from the Gr/SiO_2 and MoS_2/SiO_2 substrates, respectively (**Supplementary Figures 7(b-c)**). However, after Au metal contacts are transferred, the Raman signals corresponding to Si, graphene, and MoS_2 disappear, suggesting that the transferred Au metal contacts are able to block the 514 nm laser.



Supplementary Figure 8. (**a)** Schematic illustration of the Raman tests of the graphene films after the metal transfer-release and deposition-release processes, respectively; (**b, c)** Raman scattering spectra of the Gr/Ge surface after **(b)** metal transfer-release process and **(c)** metal deposition-release process.

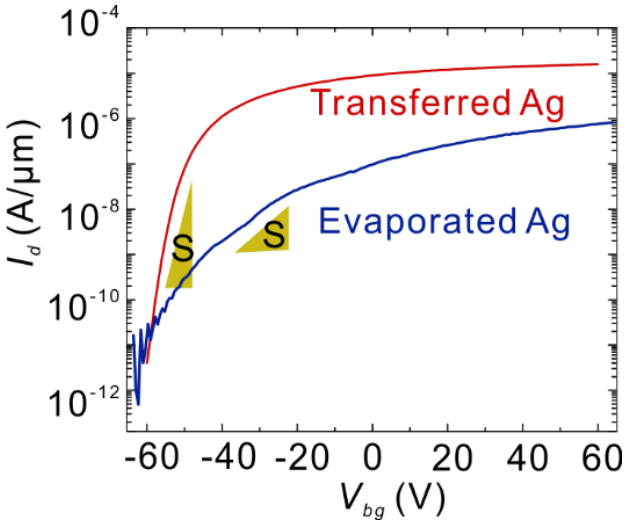
In the metal transfer-release process (**Supplementary Figure 8(a**)), the metal films are transferred onto Gr/Ge. The PVA solution is put onto the substrate again and the PVA film is formed after drying. Finally, the metals are peeled off by PVA to expose the graphene film for Raman scattering analysis. For comparison, the metal deposition-release process which involves aggressive metal deposition and PVA-assisted transfer is conducted. As shown in **Supplementary Figure 8(b**), no obvious defects-related D peaks appear in the Raman spectra after the metal transfer-release process, suggesting that the process is gentle and no defects are created. In contrast, after peeling of the deposited metals by PVA, the defect-related D peaks are observed in the Raman spectra (**Supplementary Figure 8(c**)), indicating that the deposition-release process is aggressive and can create defects in the graphene lattice due to the bombardment by energetic atoms or clusters.



Supplementary Figure 9. **(a)** Schematic illustration of recycling donor Gr/Ge substrate for Au pattern transfer. Characterizations of Au patterns and Gr/Ge substrates after transferring of Au pattern from Gr/Ge substrates once **(b)-(e)** and twice **(f)-(i)**. **(b)** and **(f)** Optical images of the Au patterns transferred on the PVA. **(c)** and **(g)** AFM images of Gr/Ge substrates after the transfer of Au patterns. **(d)** and **(h)** Raman spectra of Gr/Ge substrates after the transfer of Au patterns. Laser positions for Raman spectra collection are denoted by yellow points in **(c)** and **(g)**. **(e)** and **(i)** Raman mappings of Gr/Ge substrates after the transfer of Au patterns.

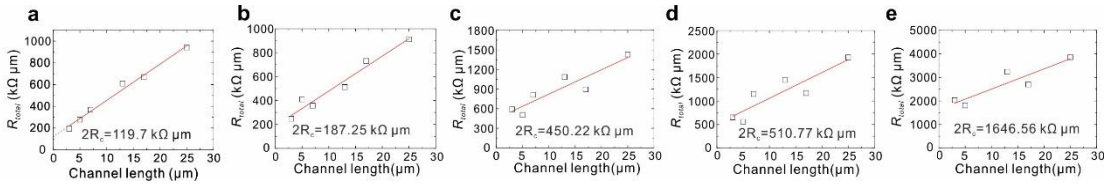
The multiple transfers of Au layers from the same Gr/Ge substrate have been performed, as schematically drawn in **Supplementary Figure 9(a)**. **Supplementary Figure 9(b) and (f)** show the optical images of the Au patterns transferred on the PVA from pristine Gr/Ge substrate and recycling Gr/Ge substrate, respectively. It is found that Au patterns can be well transferred without any visible damage or defect even

from the recycling Gr/Ge substrate. AFM images of Gr/Ge substrates after transferring Au patterns once or twice, as shown in **Supplementary Figure 9 (c)** and **(g)**, respectively. The smooth morphology of the graphene surface is always preserved after transferring Au patterns several times, which suggests the clean exfoliation of Au patterns from Gr/Ge. We also conduct Raman measurement to study the features of graphene/Ge substrate, e.g., crystalline quality, as shown in **Supplementary Figure 9 (d-e)** and **(h-i)**. To reveal the global crystalline quality of graphene, Raman spectra are collected from large regions across 5um*5um, as denoted by yellow points in **Supplementary Figure 9 (c)** and **(g)**. It is observed that the crystalline quality of graphene can also be retained after transferring Au patterns once, and it degrades a little bit after transferring Au patterns twice due to the multiple ion bombardments during Au layer deposition, as evident by the increased D peak appearing at ~1340 cm^{-1}. The comparison of 2D mappings also suggests the gradual degradation of crystalline quality of graphene during the repeatable transfer of Au patterns. Therefore, for sure, the transfer process can be repeated on the same Gr/Ge substrate for several times. But, the real recycling time of Gr/Ge substrate is limited and needs to be explored in the future, and it should correlate to the deposition conditions of Au layer, PVA pealing speed, et al.



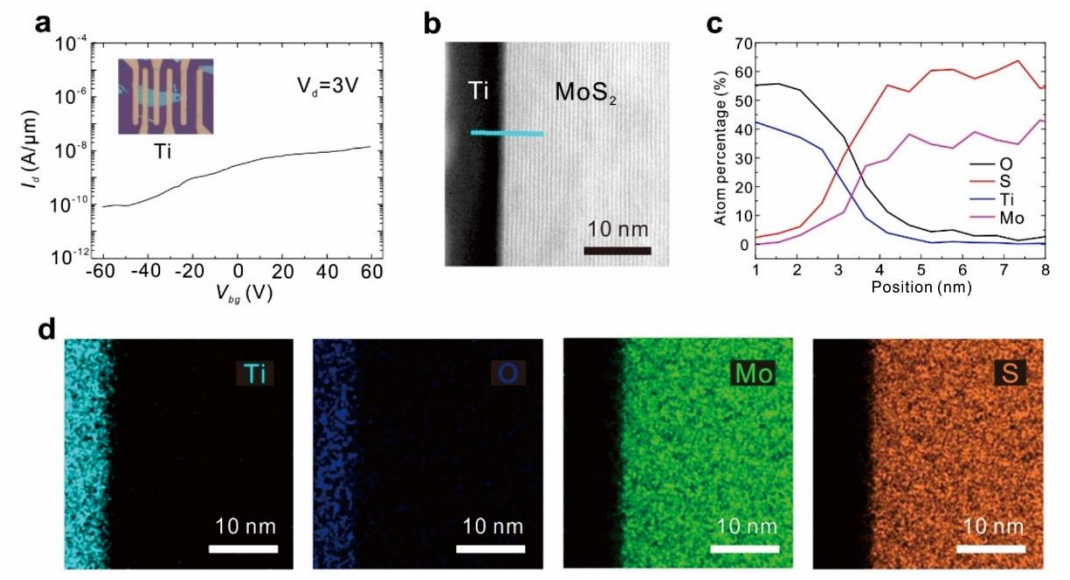
Supplementary Figure 10. The transfer curves of MoS_2 FET using the deposited Ag electrodes and the transferred Ag electrodes

Regarding the comparison of multilayer MoS_2 transistors using deposited Ag electrodes and transferred Ag electrodes, we performed the relevant experiments as shown in **Supplementary Figure 10**. Compared to the deposited Ag electrodes, the interface scattering effect existing at Ag/MoS_2 is significantly suppressed for the transferred Ag electrodes. Therefore, the on-state current for multilayer MoS_2 transistor using the transferred Ag electrodes is much higher than that of the counterpart using the deposited Ag electrode. Moreover, the subthreshold swing (SS) is considerably improved in multilayer MoS_2 transistor using the transferred Ag electrodes, which means better reliability and lower power consumption. The subthreshold swing, SS, can be expressed as $SS=(1+C_d/C_{ox})\ln 10(KT/q)$, where KT/q is the thermal voltage, C_d and C_{ox} are the depletion and the oxide capacitances, respectively. C_d, which reflects the conduction mechanism in the channel, increases as the interfacial defect increases. So, we attribute the improved SS value to the avoidance of defect creation at the Ag/MoS_2 interface during the transfer of Ag electrodes compared to the deposition of Ag electrodes.



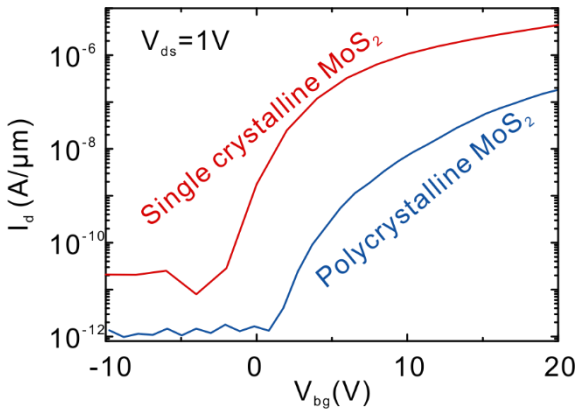
Supplementary Figure 11. (**a-e)** Total resistance normalized by width (R_{total}) as a function of the channel length for MoS_2 transistors with transferred **(a)** Ag, **(b)** Cu, **(c)** Au, **(d)** Ni, and **(e)** Pt contacts.

The total resistance normalized by width (R_{total}) is obtained from the slope of the I_d-V_{ds} curves in Figures 3d-h of the main text. As shown in **Supplementary Figures 11 (a-e)**, R_{total} is plotted as a function of the channel length and the data show a linear relationship. The y-intercept in the linear fit yields the total contact resistance ($2R_c$). Using this method, $2R_c$ values of 119.7 kΩ μm, 187.25 kΩ μm, 450.22 kΩ μm, 510.77 kΩ μm, and 1646.56 kΩ μm are derived for the Ag, Cu, Au, Ni, and Pt contacts on multilayer MoS_2, respectively.



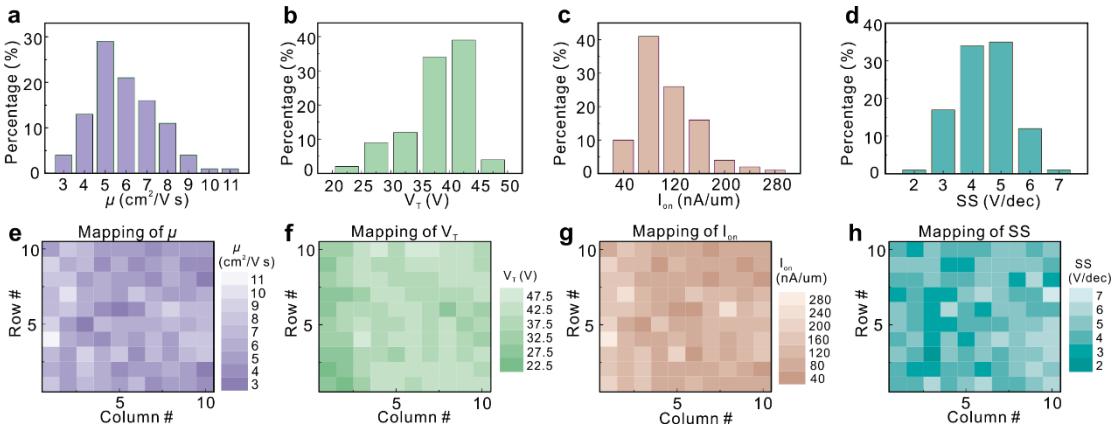
Supplementary Figure 12. (a) I_d-V_{bg} transfer curve of the MoS_2 transistor with Ti contacts obtained by the graphene-assisted metal transfer-printing process; **(b)** Cross-sectional TEM image of the transferred Ti layer on MoS_2; (**c)** Elemental distributions along the blue line in **(b)** determined by EDS; (**d)** Elemental maps of Ti, O, Mo, and S in **(b)**.

The transfer curve of the MoS_2 back-gated FET with Ti contacts obtained by the graphene-assisted metal transfer-printing process is shown in **Supplementary Figure 12 (a)**. The saturation current is about three orders of magnitude less than that of the MoS_2 back-gated FET using Ag electrodes, even though the work function of Ti (4.33 eV) is similar to that of Ag (4.26 eV), thereby suggesting that the resistance of the Ti contact is too large. **Supplementary Figures 12 (b-d)** show a considerable amount of oxygen in the Ti layer after transferring on MoS_2, although the transfer process is conducted in a nitrogen-filled glovebox with a very low O_2 concentration (< 1 ppm). Rapid oxidation of Ti is due to the high chemical activity compared to Ag, Cu, and Ni, as shown in Supplementary Table 1.



Supplementary Figure 13. Transfer characteristics of single crystalline MoS_2 transistor and polycrystalline MoS_2 transistor

Monolayer MoS_2 transistors using single crystalline MoS_2 and polycrystalline MoS_2 are fabricated and made a comparison, as shown in **Supplementary Figure 13**. The size of single crystalline MoS_2 is very limited, so only few transistors can be fabricated, and we are unable to perform the statistical analysis. While wafer-scale polycrystalline MoS_2 is commercially available and it can be used to realize the mass production of MoS_2 transistors. For transistor using single crystalline MoS_2, the on-state current can reach ~10^{-6}A/μm and the SS value is 497 mV/dec. In our study, we intend to achieve batch production of MoS_2 transistors, so wafer-scale polycrystalline MoS_2 is selected. As the crystalline quality of MoS_2 degrades, the on-current of transistor using polycrystalline MoS_2 is reduced to ~10^{-7}A/μm, and the SS value becomes to 4138 mV/dec. It should be noted that, for either single crystalline MoS_2 or polycrystalline MoS_2, the electrical performance of the corresponding transistor can be further improved by reducing the channel length using advanced lithograph tools.



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296 **Supplementary Figure 14.** Histograms of **(a)** field-effect mobility μ, **(b)** threshold
297 voltage V_T, **(c)** on-state current I_{on} **(d)** subthreshold swing SS extracted from the
298 transfer curves of 10 × 10 devices. Mappings of (**e**) μ, (**f**) V_T, (**g**) I_{on} and (**h**) SS
299 collected from 10 × 10 devices.

300

301 The electronic properties of 10 × 10 devices are analyzed, which are derived
302 from the transfer curves shown in Figure 4d in the main text. The field effect carrier
303 mobility μ is determined by $\mu = \frac{L}{WC_{ox}V_{ds}} \cdot \frac{dI_{ds}}{dV_{bg}}$ based on the transfer curve. As
304 shown in **Supplementary Figure 14 (a-d)**, the statistical results of μ, V_T, I_{on}, and SS
305 from 100 transistors show centralized distributions with mean values of 5.9 cm^2/V s,
306 38 V, 109 nA/μm, and 4.4 V/dec, respectively. Corresponding 2D mappings are shown
307 in **Supplementary Figure 14 (e-h)** and illustrate a uniform distribution indicating that
308 the MoS_2 transistors deliver uniform performance across different devices.

309

Supplementary Table 1. Free energies of formation of metal oxides.[2]

Metals	**Metal oxide**	**$\Delta_r G_m$ (kJ/mol, per atom basis)**
Ag	Ag_2O	-5.6
Cu	CuO	-129.7
Ni	NiO	-211.7
Ti	TiO_2	-888.8

Supplementary Table 2. Comparison of the electrical properties of the MoS_2 transistors.

Channel materials	**Gate**	**Array**	**On/off ratio**	**Off state current (A/μm)**	**References**
CVD monolayer MoS_2/SiO_2	back	yes	10^5	10^{-12}	Ref. 3
CVD monolayer MoS_2/SiO_2	back	yes	10^7	10^{-12}	Ref. 4
CVD monolayer MoS_2/SiO_2	dual	yes	10^6	10^{-12}	Ref. 5
CVD monolayer MoS_2/SiO_2	top	yes	10^7-10^8	10^{-13}-10^{-14}	Ref. 6
CVD monolayer MoS_2/SiO_2	back	no	10^7	10^{-13}	Ref. 7
CVD monolayer MoS_2/SiO_2	back	yes	10^6	10^{-12}	Ref. 8
CVD monolayer MoS_2/SiO_2	back	yes	10^5-10^6	10^{-11}	Ref. 9
Si	gate-all-around	yes	10^7	10^{-11}	Ref. 10
CVD monolayer MoS_2/SiO_2	back	yes	~10^7	< 10^{-13}	This work

Supplementary Reference

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