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Supplementary information

How to report and benchmark emerging field-effect transistors

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Supplementary Information for

How to Report and Benchmark Emerging Field-Effect Transistors

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Note S1: Rigorously reporting and benchmarking I_{max}/I_{min}

The I_{max}/I_{min} ratio is the most-used figure of merit for evaluating off-state performance of a transistor and it depends on multiple factors. First, I_{max}/I_{min} is impacted by material properties such as material quality, bandgaps, and doping conditions. Secondly, the specific device structure and geometry, including the channel length and gate capacitance, also affect the achievable I_{max}/I_{min}. Thirdly, the same device operating at different operation regimes might also have different I_{max}/I_{min}. Combined with the absence of a well-defined V_{DD}, these factors make rigorous reporting and benchmarking guidelines strongly desired for I_{max}/I_{min}. Rigorously reporting I_{max}/I_{min} involves clearly identifying the V_{DS} and V_{GS} values at which the I_{max} and I_{min} are extracted. This practice will help fairly benchmark I_{max}/I_{min} between different devices.

Similar to Fig. 3a, Fig. S1a represents benchmarking I_{max}/I_{min} at $V_{DS} = 1$ V, which is a commonly used bias condition when obtaining subthreshold curves. Under $V_{DS} = 1$ V, short-channel devices (e.g., Device A) may operate at the saturation regime, whereas long-channel devices (e.g., Device B) at the linear regime. While using the same $V_{DS} = 1$ V is a convenient and simple method, the I_{max}/I_{min} likely represent different operation regimes for the two example devices. For a more precise comparison, instead of extracting the I_{max} and I_{min} at the same V_{DS} value for the different devices, it is possible to ensure they are extracted in the same regime (linear or saturation) by using the drain-source electric field instead of V_{DS}; e.g., $E_{DS} = 0.1$ V/μm for the linear regime. This improved comparison is demonstrated in Fig. S1b, where the carrier density at which the I_{max} is extracted is also labeled, ensuring that different devices have the same carrier density in their I_{max} extraction.

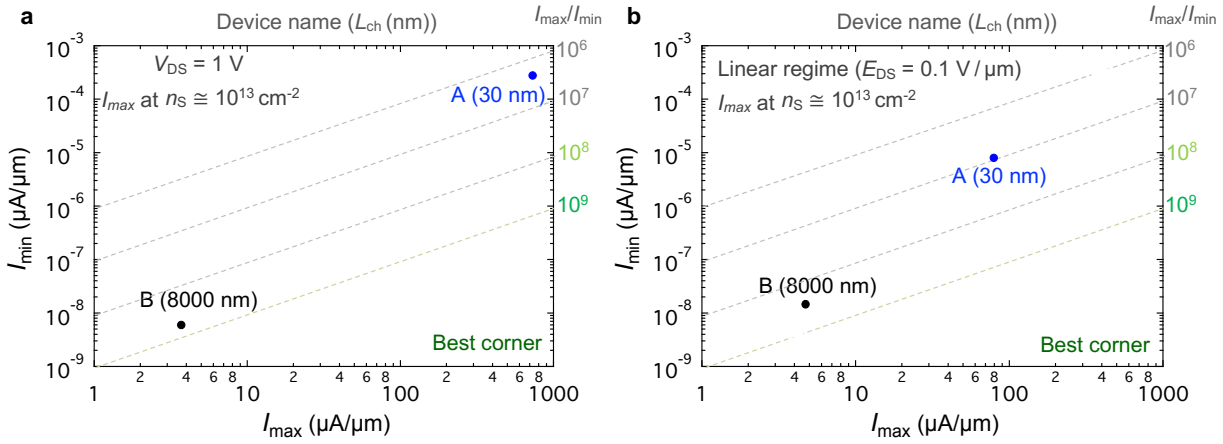

Fig. S1 | Rigorously benchmarking I_{max}/I_{min}. **a**, Benchmarking I_{max}/I_{min} at $V_{DS} = 1$ V, similar to Fig. 3a. Devices A and B are not actual experimental data and are used to demonstrate benchmarking devices with different channel lengths. The carrier density at which the I_{max} is extracted is also labeled. **b**, Benchmarking I_{max}/I_{min} at the same operation regime, which is the linear regime with drain-to-source field $E_{DS} = 0.1$ V/μm used as an example. Note, the diagonal dashed lines indicate certain values of I_{max}/I_{min}.

Additional factors can impact I_{max}/I_{min} ratio. When benchmarking devices with the same channel material but with different channel thicknesses, plotting I_{max}/I_{min} vs. t_{ch} is suggested. It is noteworthy that I_{max}/I_{min} also depends on channel length and the equivalent oxide thickness (EOT) of the gate insulator. When the devices to be benchmarked have the same channel thickness, then benchmarking I_{max}/I_{min} vs. L_{ch}/EOT should be considered. In addition, I_{min} can be limited by the measurement instrumentation, especially in materials with larger band gap such as monolayer TMDs. Additional factors impacting I_{max}/I_{min} include contact resistance (which limits I_{max}), leakage currents (which dominate I_{min}) and parasitic capacitances (which affect electrostatic control of the gate), etc.

Note S2: Different methods to extract threshold voltage V_T and its uncertainties

Different methods to extract V_T

A standard method to extract the V_T is not yet available. Refs. [4–7] have investigated and compared different V_T extraction methods. Specifically, in Ref. [4], the authors investigated eleven approaches to extract the V_T and found that similar V_T values in the linear regime can be extracted. In Refs. [5,6], the authors proposed the Y-function method to eliminate the R_c effect when evaluating mobility values. In their studies, the V_T is extracted from the $I_D/g_m^{0.5}$ curve.

Uncertainty of V_T induced by I-V sweeps

The threshold voltage V_T uncertainties can propagate to the estimation of carrier density. Fig. S2 shows an example of V_T shift due to different sweeps (I_D-V_{GS} vs. I_D-V_{DS}) on the same device illustrated in Fig. 2c.

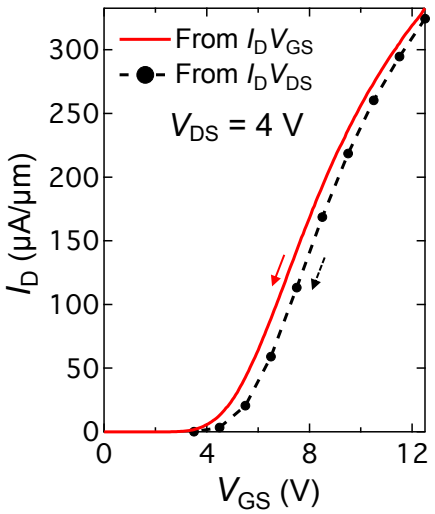

Fig. S2 | Comparison of transfer curves at V_{DS} = 4 V from I_D-V_{GS} sweep (red) and extraction from I_D-V_{DS} sweeps (black) based on data in Figures 2b,d of the main text. The direction of the sweeps is the same (backward). A V_T shift of ~0.6 V is observed comparing the I_D-V_{GS} and I_D-V_{DS} sweeps. We presume this shift arises from hot-carrier stress during the I_D-V_{DS} sweeping at high V_{DS} and V_{GS}. Due to high electric fields, energetic electrons become trapped in the gate oxide as fixed charges[8], increasing the V_T. This phenomenon highlights the dependence of V_T on I_D-V_{DS} sweeping.

Note S3: Extracting R_c from TLM

Extracting R_c from TLM data can lead to significant uncertainties. As a reminder, TLM data is a plot of the total resistance (R_{tot}) from a set of devices having all things consistent with their structure and materials except their channel length. TLM data is plotted as R_{tot} vs L_{ch}, where the $R_{tot} = R_{ch} + 2R_c = R_{sh}L_{ch} + 2R_c$, which means when the channel length is zero (y-axis intercept) $R_{tot} = 2R_c$. A reliable R_c must be derived from TLM data that includes devices in the short-channel limit, where **R_c dominates the total resistance** or at least is comparable to the R_{ch}. Ideally, the sheet resistance and its variation need to be sufficiently small; otherwise, a small variation in R_{sh} could lead to substantial errors in R_c. Three examples of TLM data are presented in Fig. S3a, all claiming an R_c of 500 Ω·μm, based on the intercepts to the R_{tot} axis. However, due to the larger R_{sh}, the uncertainty of R_c in TLM A is significantly larger than TLM B (e.g., a small change in R_{sh} for TLM A would result in a large change in the extracted R_c). In TLM A, the shortest channel device has an R_{tot} of 10 kΩ·μm, which is much larger than the claimed R_c of 500 Ω·μm, whereas in TLM B, the R_{tot} is 2 kΩ·μm and the claimed R_c is 500 Ω·μm. As noted above, with a slight variation in the R_{sh} in TLM A, the R_c might be extracted as a very small (and often untrue) value or even a negative value.

Hence, it is critical to have both of the following in a TLM: 1) devices with channel length small enough to ensure $2R_c$ dominates R_{tot} and 2) a sufficient number of longer channel length devices to ensure a reliable R_{sh} extraction based on a linear fit. Another possible scenario to avoid is illustrated with TLM C, which represents a TLM data set where all of the devices are $2R_c$ dominated thus leading to an inaccurate estimation of R_{sh}. This comparison further highlights the need for proper TLM data; as a summary, a valid TLM data set should have at least four channels and include at least one each of contact and channel resistance-dominated devices.

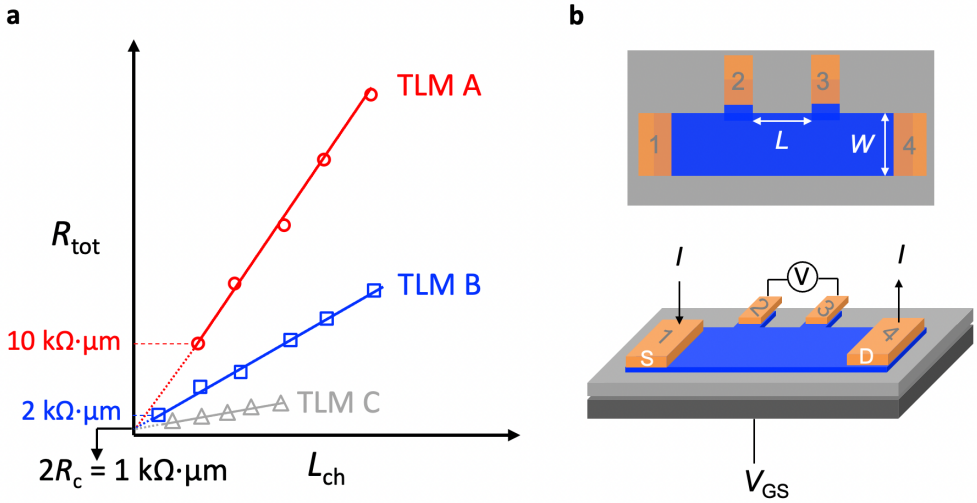

Fig. S3 | a, Demonstration of TLM data sets with all R_{ch}-dominant devices (TLM A, leading to unreliable R_c extraction), all R_c-dominant devices (TLM C, leading to unreliable R_{sh} extraction), and an appropriate balance of devices (TLM B). **b**, Example diagram of four-probe measurements to extract R_{sh}, with a back-gate as a demonstration. The channel resistance R_{ch} between probe 2 and 3 is $R_{14,23} = V_{23}/I_{14}$, where I_{14} is the current flowing from probe 1 to 4 and V_{23} is the voltage between probe 2 and 3. $R_{sh} = R_{14,23}(W/L)$. R_{sh} can be obtained while V_{GS} is swept, yielding R_{sh} vs. V_{GS} or carrier density, which can be used to cross-examine the R_{sh} extracted from TLM.

Since there can be considerable variation in the quality of emerging semiconducting materials, even on the same chip (e.g., variation in crystal quality in MoS_2), this can translate to a sizeable variation in R_{sh} from one device to another. Note, a perfect TLM is based on the assumption that R_{sh} is the same for all devices being tested, so any disruption to this assumption translates to inaccuracy in the extraction of R_c. Hence, it is highly recommended to fabricate several TLM device sets and plot the full distribution of resultant TLM data (multiple data points for each channel length). This provides evidence for how dependable the extraction is; a good example of this is in Ref. [9] and Fig. S5g below.

Another critical aspect of proper TLM data sets is the need for reporting the uncertainties of R_{sh} and R_c in standard error or confidence interval from a least-squares fit of the TLM curve; an example of this can be seen in Fig.2h and Ref. [10]. Lastly, if a record parameter is claimed based on TLM, four-probe measurements[7,11] should ideally be used as a complementary method to cross-check the results. Traditionally, four-probe measurements are used to characterize the resistivity of "bulk" doped films and a gate bias is not involved. However, to estimate the R_{sh} for emergent semiconducting materials, it is necessary to sweep the gate bias so that R_{sh} vs. gate voltage (carrier density, n_S) can be obtained. An example of the four-probe measurement is given in Fig. S3b. It is key to have probe 2 and 3 placed to the side of the channel so that the voltage probes (2 and 3) do not obstruct the current flow from probe 1 to 4. After obtaining R_{sh} vs. n_S, R_c vs. n_S can be derived by subtracting R_{sh} from R_{tot}.

A final caution regarding the use of TLM data is regarding the transfer length (L_T), which is the length of the contact over which the majority of carrier injection occurs between the metal and semiconductor. Traditionally, L_T was also extracted from TLM data as the intercept of the linear fit with the L_{ch} (x-axis). However, extracting L_T in this manner assumes that the sheet resistance of the semiconductor in the metal-contacted region is the same as for the semiconductor in the channel region. For emergent semiconducting materials, particularly low-dimensional materials like CNTs or 2D TMDs, this is not a valid assumption as transport through the materials happens predominantly (if not entirely) on the surface and is strongly dependent on the materials interfacing with the semiconductor. Because L_T has significant implications for the scalability of the contact length in emergent FETs, it must not be improperly extracted and reported from simple TLM data sets. This is commented on further in the next section (Note S4).

Note S4: Additional Parameters

In the main text, we covered the most representative parameters for reporting and benchmarking emergent FETs. Here we describe some additional parameters used in specific studies.

Normalization of I_D for 1D devices: For 1D or close to 1D devices, to compare I_D, it is sometimes necessary to convert the I_D per CNT/nanowire/nanosheet stack to I_D per µm. If the 1D channel materials are aligned CNTs or nanowires (Fig. S4a), the normalization of currents depends on the density of the 1D channel or the number of 1D channels in 1 µm. If the CNTs or nanowire are a dense network, treating the channel similar to a 2D material is more appropriate. For gate-all-around nanosheet devices (Fig. S4b), it is common to report I_D per nanosheet stack. If reporting the I_D per channel footprint, then the current per nanosheet stack should be divided by the nanosheet width (W_{NS}). A more detailed reporting of I_D per channel width would require the calculation total channel width of the nanosheets in the stack, which is close to $W_{NS} \times T_{NS} \times$ number of nanosheets in the stack. The normalized drain currents per channel width is I_D per stack divided by the total channel width of the stack. Ultimately, what matters is both an indication of what is achieved on a per nanomaterial/structure basis (e.g., per CNT or per nanosheet stack) as well as what is achieved on a per aerial footprint width basis (i.e., µA per W_{ch}).

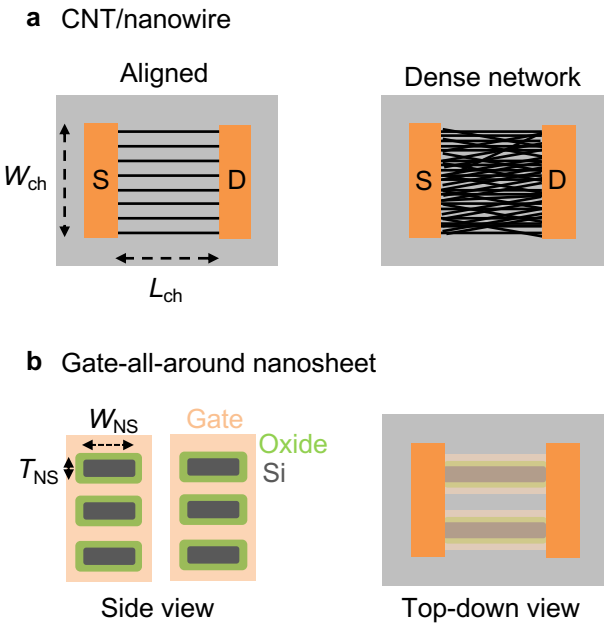

Fig. S4 | Normalization of currents for transistors based on 1D or close to 1D channel materials. **a**, top-down view of transistors based on CNTs or nanowires in the form of aligned channels and a dense network. **b**, side-view and top-down (aerial) view of gate-all-around nanosheet transistors.

Schottky barrier height: For Schottky contacts between metal and semiconductors, the Schottky barrier height determines the efficiency of carrier transport in the contacts. Hence, properly extracting the barrier height is key for comparing different contact engineering approaches. Examples of Schottky barrier extraction can be found in Ref. [3,12–14], with some variances in the equations and approaches used.

Transfer length (L_T): Because charge carriers tend to crowd near the contact edge when transported between the metal contacts and the channel material, only a certain portion of the contacts actively participate in the carrier transport process. The transfer length denotes the distance over which most of the current transfers in the contact. Traditionally, L_T can be estimated as $\sqrt{\frac{\rho_c}{\rho_{sh}}}$ from the transfer length method plot, where the ρ_c is the specific contact resistivity (unit: $\Omega \cdot cm^2$) and ρ_{sh} is the sheet resistance underneath the contact (unit: Ω/square) – this is discussed in some detail in Note S3 above. However, this estimation is not reliable for emergent transistors due to: 1) many of the emergent transistors use ultra-thin, low-dimensional nanomaterials, which can alter the current crowding behavior; 2) lots of research-grade emergent transistors have gated contacts, which complicates the estimation of the sheet resistance underneath the contact; and 3) the difference in the interface between the metal-semiconductor and gate insulator semiconductor leads to further differences in sheet resistance of the semiconductor in these regions. Hence, accurately determining L_T will depend on physically scaled contacts to observe the contact scaling behavior.

Interface trap density (D_{it}): This parameter is essential for studying and evaluating novel gate dielectrics. Different methods for determining D_{it} can be found in Ref. [12].

High-frequency response of the gate insulator capacitance: Although most of the parameters covered in the main text are low-frequency parameters, for devices to be eventually used in high-frequency and high-performance applications, it is necessary to properly evaluate the high-frequency response of the gate insulator capacitance and the current-voltage characteristics[15].

Note S5: Demonstration of device spread and parameter variations

As indicated in the main text, we recommend showing device spread and parameter variations to demonstrate the full picture of the reported devices. In Fig. S5, based on ten TLM structures similar to the one used in Fig. 2, we demonstrate the spread of device characteristics and parameter variations using a cumulative distribution function plot and boxplots.

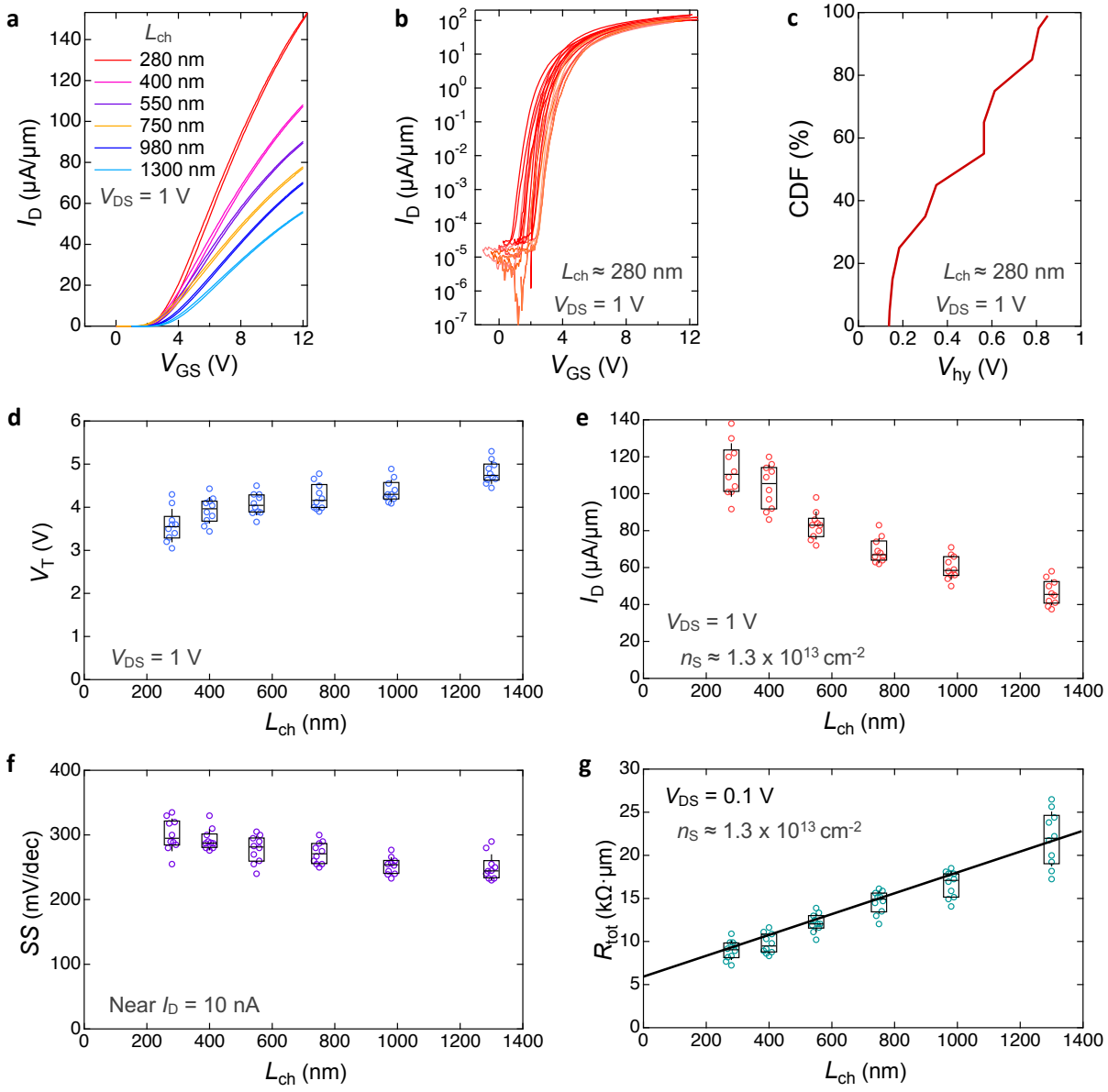

Fig. S5 | Demonstration of device spread and parameter variations based on ten TLM structures. **a**, Example transfer curves (I_D-V_{GS}) for the TLM structure in Fig. 2. **b**, Measured subthreshold curves (I_D-V_{GS}) of ten devices with L_{ch} of 280 nm of 280 nm. **c**, Cumulative distribution function (CDF) of the hysteresis voltage for the ten devices with L_{ch} of 280 nm. Boxplots of (**d**) V_T, (**e**) I_D at V_{DS} = 1 V and n_S = 1.3×10^{13} cm^{-2}, (**f**) the minimal *SS* extracted near I_D = 10 nA, and (**g**) ten TLM plots with the median R_c value of 3 kΩ·μm.

Note S6: Benchmarking devices with different channel thicknesses

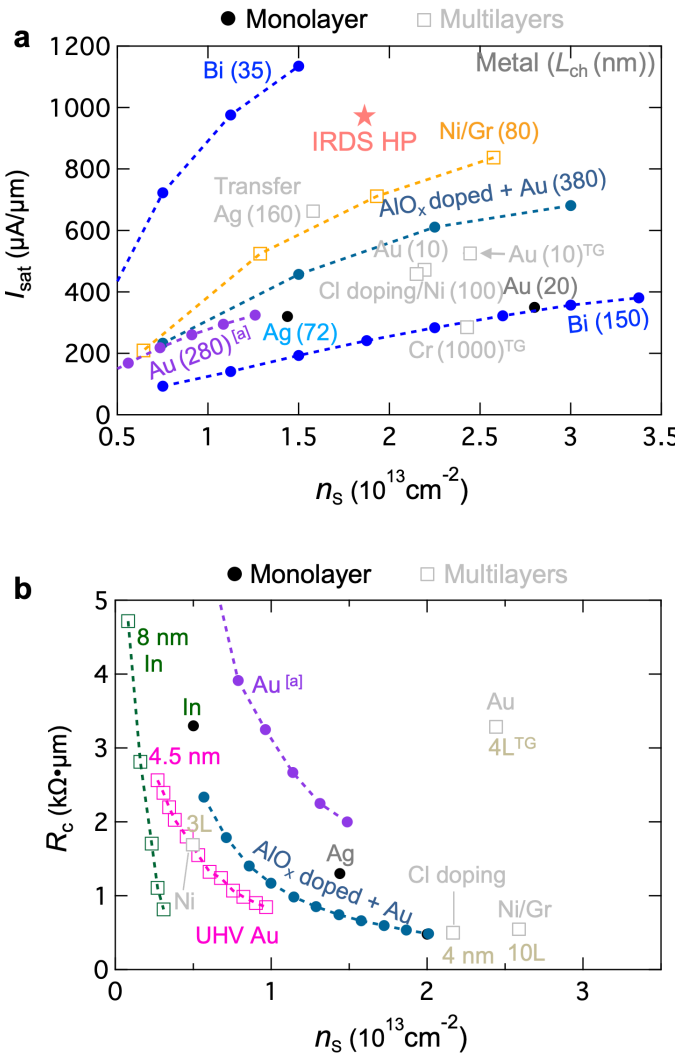

Fig. S6 | Example benchmarking device performance of MoS_2 FETs with different channel thicknesses. **a**, Benchmarking I_{sat} versus n_S, where the channel length in nm is labeled next to the metal contacts used in the devices. **b**, Benchmarking R_c versus n_S in a few representative reports, where the channel thickness is labeled for the multilayer channels. "a" stands for the example device in Fig. 2. A few studies are plotted as dotted lines to keep the plots from cluttering and also highlight the trends. Different colors are assigned to different reported devices. Most of the data are extracted from the following published reports: transferred Ag[16], AlO_x doped+Au[17], Ag[18], In[19], Ni [20], Cl doping[1], Ni/Gr[2], and Bi[3].

Representative reports with relatively large I_{sat} are listed in Table S1, with both monolayer and multilayer MoS_2 channels included.

Table S1| Representative reporting on studies of MoS_2 FETs with I_{sat}

Contacts	Ref.	t_{ch} (nm)	L_{ch} (nm)	n_S (10^{13} cm^{-2})	R_c (kΩ·μm)	V_{DS} (V)	I_{sat} (μA/μm)
Ag	[18]	1L	72	1.44	1.3	1.8	320
Au	[a]	1L	280	1.3	2	4	325
Au	[21]	1L	20	2.8	N/A	2	350
Bi	[3]	1L	150	3.4	0.12	2	380
Ni+Cl doping	[1]	4	100	2.16	0.5	1.6	460
Au	[21]	6	10	2.19	N/A	2	470
Sn	[22]	1L	35	1	0.84	1.5	615
Transferred Ag	[16]	4~20	160	1.58	N/A	3	660
AlO_x+Au	[17]	1L	380	2	0.48	5	700
Ni/Gr	[2]	10L	80	2.58	0.54	2	830
Ni	[23TG]	4.2	1000	2.43	N/A	3	290
Au	[24TG]	1L	10	~7	1.7	2	425
Cr	[25TG]	~4L	400	2.44	3.3	4	526

a: the example MoS_2 FET in Fig. 2a; TG = top gate; 1L = monolayer; 2L = bilayer, etc.
The Table lists I_{sat} in ascending order but not including the last three rows because they are top-gated. All other FETs were back-gated. μ_{FE} is not benchmarked as several of the studies listed have overestimated values. More studies that may not have I_{sat} reported can be accessed at Ref. [26].

References:

1. Yang, L. *et al.* High-Performance MoS_2 Field-Effect Transistors Enabled by Chloride Doping : Record Low Contact Resistance (0.5 k·μm) and Record High Drain Current (460 μA/μm). in *VLSI Technology* (2014).
2. Liu, Y. *et al.* Pushing the Performance Limit of Sub-100 nm Molybdenum Disulfide Transistors. *Nano Lett* **16**, 6337–6342 (2016).
3. Shen, P.-C. *et al.* Ultralow contact resistance between semimetal and monolayer semiconductors. *Nature* **593**, 211–217 (2021).
4. Ortiz-Conde, A. *et al.* A review of recent MOSFET threshold voltage extraction methods. *Microelectron. Reliab.* **42**, 583–596 (2002).
5. Ghibaudo, G. New method for the extraction of MOSFET parameters. *Electron. Lett.* **24**, 543–545 (1988).
6. Chang, H. Y., Zhu, W. & Akinwande, D. On the mobility and contact resistance evaluation for transistors based on MoS_2 or two-dimensional semiconducting atomic crystals. *Appl. Phys. Lett.* **104**, 113504 (2014).
7. Pang, C. *et al.* Mobility Extraction in 2D Transition Metal Dichalcogenide Devices—Avoiding Contact Resistance Implicated Overestimation. *Small* **17**, 2100940 (2021).
8. Streetman, B. G. & Banerjee, S. K. *Solid State Electronic Devices, 6th Edition*. (Pearson, 2006).
9. Kumar, A. *et al.* Sub-200 Ω·μm Alloyed Contacts to Synthetic Monolayer MoS_2. in *IEEE International Electron Devices Meeting (IEDM)* 154–157 (2021).
10. Smithe, K. K. H., English, C. D., Suryavanshi, S. V & Pop, E. Intrinsic electrical transport and performance projections of synthetic monolayer MoS_2 devices. *2D Mater.* **4**, (2016).
11. Guros, N. B. *et al.* Reproducible Performance Improvements to Monolayer MoS_2 Transistors through Exposed Material Forming Gas Annealing. *ACS Appl. Mater. Interfaces* **11**, 16683–16692 (2019).
12. Schroder, D. K. *Semiconductor Material and Device Characterization, 3rd Edition*. (Wiley-IEEE Press, 2015).
13. Das, S., Chen, H. Y., Penumatcha, A. V & Appenzeller, J. High performance multilayer MoS_2 transistors with scandium contacts. *Nano Lett* **13**, 100–105 (2013).
14. Cheng, Z. *et al.* Immunity to Contact Scaling in MoS_2 Transistors Using in Situ Edge Contacts. *Nano Lett.* **19**, 5077–5085 (2019).
15. Bethge, O. *et al.* Process temperature dependent high frequency capacitance-voltage response of ZrO2/GeO2/germanium capacitors. *Appl. Phys. Lett.* **96**, 052902 (2010).
16. Liu, Y. *et al.* Approaching the Schottky-Mott limit in van der Waals metal-semiconductor junctions. *Nature* (2018) doi:10.1038/s41586-018-0129-8.
17. McClellan, C. J., Yalon, E., Smithe, K. K. H., Suryavanshi, S. V. & Pop, E. High Current Density in Monolayer MoS_2 Doped by AlOx. *ACS Nano* **15**, 1587–1596 (2021).
18. Smithe, K. K. H., English, C. D., Suryavanshi, S. V. & Pop, E. High-Field Transport and Velocity Saturation in Synthetic Monolayer MoS_2. *Nano Lett.* **18**, 4516–4522 (2018).
19. Wang, Y. *et al.* Van der Waals contacts between three-dimensional metals and two-dimensional semiconductors. *Nature* **568**, 70–74 (2019).
20. Smets, Q. *et al.* Ultra-scaled MOCVD MoS_2 MOSFETs with 42nm contact pitch and 250μA/μm drain current. in *Technical Digest - International Electron Devices Meeting, IEDM* (2019). doi:10.1109/IEDM19573.2019.8993650.
21. Patel, K. A., Grady, R. W., Smithe, K. K. H., Pop, E. & Sordan, R. Ultra-scaled MoS_2 transistors and circuits fabricated without nanolithography. *2D Mater.* **7**, 015018 (2020).
22. Chou, A. S. *et al.* High On-State Current in Chemical Vapor Deposited Monolayer MoS_2 nFETs with Sn Ohmic Contacts. *IEEE Electron Device Lett.* **42**, 272–275 (2021).
23. Li, X. *et al.* Effect of Dielectric Interface on the Performance of MoS_2 Transistors. *ACS Appl Mater Interfaces* **9**, 44602–44608 (2017).
24. English, C. D., Smithe, K. K. H., Xu, R. L. & Pop, E. Approaching ballistic transport in monolayer

MoS_2 transistors with self-aligned 10 nm top gates. *Tech. Dig. - Int. Electron Devices Meet (IEDM)* 5.6.1-5.6.4 (2017) doi:10.1109/IEDM.2016.7838355.
25. Zou, X. *et al.* Interface engineering for high-performance top-gated MoS_2 field-effect transistors. *Adv. Mater.* **26**, 6255–6261 (2014).
26. McClellan, C. J. *et al.* 2D Device Trends. http://2d.stanford.edu.