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Supplementary information

Integrated acoustic resonators in commercial fin field-effect transistor technology

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Integrated Acoustic Resonators in Commercial Fin Field-Effect Transistor Technology
Supplemental Information

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1 FinFET Sensing: Electromechanical Conversion from Stress to Drain Current

To understand the conversion from stress to drain current in the sense transistors, modulation of three separate FET properties is examined: channel mobility due to piezoresistivity, oxide capacitance, and silicon bandgap.

1.1 Mobility

The piezoresistive effect is typically modeled as a linear change in resistivity (ρ) as a function of applied stress (σ) and the longitudinal and transverse piezoresistive coefficients (π):

$$\rho = \rho_0[1 + \pi_L\sigma_L + \pi_T\sigma_T]. \tag{1}$$

Low-field mobility (μ) is related to the resistivity as follows, where q is the elementary charge and N is the doping concentration per unit volume.

$$\mu = 1/q\rho N \tag{2}$$

A stress-dependent mobility can be defined in terms of the initial mobility μ_0,

$$\mu(\sigma) = \frac{\mu_0}{1 + \pi_L\sigma_L + \pi_T\sigma_T} \tag{3}$$

and the initial value of mobility subtracted out to obtain the net change

$$\Delta\mu(\sigma) = \mu_0\left(\frac{1 - (1 + \pi_L\sigma_L + \pi_T\sigma_T)}{1 + \pi_L\sigma_L + \pi_T\sigma_T}\right) = \mu_0\frac{-\pi_L\sigma_L - \pi_T\sigma_T}{1 + \pi_L\sigma_L + \pi_T\sigma_T} \tag{4}$$

1.2 Oxide Capacitance

Oxide capacitance changes due to the physical thickness change of the oxide (t_{ox}) under strain. This strain ($\Delta t_{ox}/t_{ox0}$) is given by the applied stress divided by the Young's modulus, E, of the dielectric, assuming the film is stressed in the elastic regime. Such a relation results in the following expressions:

$$C'_{ox}(\sigma) = \frac{\epsilon_{ox}}{t_{ox0} + \Delta t_{ox}} = \frac{\epsilon_{ox}}{t_{ox0}(1 + \sigma/E_{ox})} \tag{5}$$

$$\Delta C'_{ox} = \frac{\epsilon_{ox}}{t_{ox0}}\left(\frac{1}{1 + \sigma/E_{ox}} - 1\right) = C'_{ox0}\left(\frac{-\sigma/E_{ox}}{1 + \sigma/E_{ox}}\right) \tag{6}$$

1.3 Bandgap Modulation

Strain dependence of the bandgap of silicon (E_g) is given by [1]:

$$E_g(\xi) = E_{g0} + E_{1g}\xi \tag{7}$$

where E_{1g} represents the sensitivity of the bandgap to total strain ξ, where

$$\xi = \sum_{j=1}^{3} \sigma_{jj}/E_{jj}. \tag{8}$$

Using this relation, the theoretical dependence of threshold voltage on strain can be derived using a typical expression for extrapolated threshold voltage that is referenced to the approximate onset of strong inversion [2]:

$$V_T = V_{FB} + \phi_0 + \gamma\sqrt{V_{SB} + \phi_0} \tag{9}$$

where V_{SB} is the source to body voltage, V_{FB} is the flat-band voltage governed by the metal-semiconductor work function ϕ_{ms} and effective oxide charge per unit area Q_0', by

$$V_{FB} = \phi_{ms} - Q_0'/C_{ox}', \tag{10}$$

ϕ_0 is a value a few ($2 < n < 5$ typical) thermal voltages ϕ_t above the onset of strong inversion

$$\phi_0 = 2\phi_f + n\phi_t, \tag{11}$$

and

$$\gamma = \frac{\sqrt{2q\epsilon_s N_A}}{C_{ox}'}, \tag{12}$$

where ϵ_s is the semiconductor permittivity N_A is the semiconductor acceptor doping per unit volume (assuming p-type substrate),

$$\phi_{ms} = \phi_m - \chi_s - E_g/2 - \phi_f, \tag{13}$$

$$\chi_s = E_{vac} - E_c, \tag{14}$$

and

$$\phi_f = kT * ln\Big(\frac{N_A}{n_i}\Big), \tag{15}$$

with n_i being the intrinsic carrier concentration in the semiconductor ($\approx 10^{10}$ in silicon at room temperature). Combining all of this together,

$$\begin{aligned} V_T(\xi) = \phi_m - \chi_s(\xi) - E_g(\xi)/2 + \phi_f(\xi) - Q_0'(\xi)/C_{ox}'(\xi) \\ + nkT + \frac{\sqrt{2q\epsilon_s N_A(\xi)}}{C_{ox}'(\xi)}\sqrt{V_{SB} + 2\phi_f(\xi) + nkT} \end{aligned} \tag{16}$$

The dependence of C_{ox}' on strain has already been discussed. The other terms, however, require further examination. Starting with the expression for n_i,

$$n_i = \sqrt{N_c N_v} * exp\Big(\frac{-E_g}{2kT}\Big) \tag{17}$$

where $N_{c/v}$ are related to the effective mass of carriers in the semiconductor conduction and valance band as follows:

$$N_{c/v} = 2 * \sqrt[3/2]{\frac{2\pi m_{n/p}^*}{kTh^2}} \tag{18}$$

Neglecting the change in $\sqrt{N_c N_v}$ since it will have less impact than the change in the exponential term,

$$n_i(\xi) \approx \sqrt{N_c N_v} * exp\Big(\frac{-(E_g + \Delta E_g)}{2kT}\Big) = \sqrt{N_c N_v} * exp\Big(\frac{-E_g}{2kT}\Big) exp\Big(\frac{-\Delta E_g}{2kT}\Big)$$
$$= n_{i0} * exp\Big(\frac{-\Delta E_g}{2kT}\Big) \quad (19)$$

Carrier concentration exhibits a simple dependence on strain as the stretching/compression of the lattice merely changes the number of charges within a fixed volume. To a first order approximation,

$$N_A(\xi) = \frac{N_{A0}}{1+\xi} \quad (20)$$

These expressions, along with bandgap dependence on strain, are now inserted into the expression for ϕ_f to obtain

$$\phi_f(\xi) = kT * ln\Big(\frac{N_{A0}}{n_{i0}} * \frac{exp(\Delta E_g/2kT)}{1+\xi}\Big) = \phi_{f0} + kT * ln\Big(\frac{exp(\Delta E_g/2kT)}{1+\xi}\Big) \quad (21)$$

where

$$\Delta\phi_f = kT * ln\Big(\frac{exp(\Delta E_g/2kT)}{1+\xi}\Big) = \Delta E_g/2 + kT * ln\Big(\frac{1}{1+\xi}\Big) \quad (22)$$

Examining the change in threshold voltage as a function of gate dielectric stress and strain in the silicon substrate, the only term that does not have a well defined relation is Q_0'. This is because the term is the projection of all parasitic charges in the gate stack onto the semiconductor surface. Thus, while this term is itself an effective sheet charge, it in reality encompasses a mixture of sheet and volume charges which respond differently to strain, the ratio of which is not well defined. This term is thus left alone in the expression below, being defined as an initial $(Q_0 0')$ and change in $(\Delta Q_0')$ value. Substituting the derived relations into Eq. 16 and subtracting out the initial threshold voltage value gives the following expression for ΔV_T:

$$\Delta V_T = -\Delta\chi_s + kT * ln\Big(\frac{1}{1+\xi}\Big) + \Bigg(\frac{\sqrt{2q\epsilon_s \frac{N_{A0}}{1+\xi}}}{C'_{ox}(1+\sigma/E_{ox})} * \sqrt{2\Big(\phi_{f0} + \Delta E_g/2 + kT * ln\Big(\frac{1}{1+\xi}\Big)\Big) + V_{SB} + nkT}$$
$$- \frac{\sqrt{2q\epsilon_s N_{A0}}}{C'_{ox0}}\sqrt{V_{SB} + 2\phi_{f0} + nkT}\Bigg) - \Big(\frac{\Delta Q_0' - Q_{00}'\sigma/E_{ox}}{C'_{ox}(1+\sigma/E_{ox})}\Big)$$
$$(23)$$

1.4 Square Law Model

The source-referenced simplified strong-inversion model with $\alpha = 1$ gives the traditional square-law model [2]:

$$I_d = \mu C_{ox}\frac{W}{L}\Big((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\Big) \quad (24)$$

Modified to include the effects of stress on μ, C'_{ox}, and V_T, this becomes the following:

$$I_d(\sigma) = (\mu_0 C'_{ox0} + \mu_0\Delta C'_{ox} + C'_{ox0}\Delta\mu + \Delta\mu\Delta C'_{ox}) * \frac{W}{L}\Big((V_{GS} - V_{T0})V_{DS} - \frac{V_{DS}^2}{2}\Big)$$
$$- \Delta V_T V_{DS}\frac{W}{L}(\mu_0 C'_{ox0} + \mu_0\Delta C'_{ox} + C'_{ox0}\Delta\mu + \Delta\mu\Delta C'_{ox}) \quad (25)$$

where

$$\Delta I_d(\sigma) = (\mu_0\Delta C'_{ox} + C'_{ox0}\Delta\mu + \Delta\mu\Delta C'_{ox}) * \frac{W}{L}\Big((V_{GS} - V_{T0})V_{DS} - \frac{V_{DS}^2}{2}\Big)$$
$$- \Delta V_T V_{DS}\frac{W}{L}(\mu_0 C'_{ox0} + \mu_0\Delta C'_{ox} + C'_{ox0}\Delta\mu + \Delta\mu\Delta C'_{ox}) \quad (26)$$

Likewise, in saturation

$$I_{d0} = \mu C_{ox}\frac{W}{2L}\Big((V_{GS}-V_T)^2\big(1+\lambda[V_{DS}-(V_{GS}-V_{T0})]\big)\Big) \tag{27}$$

and

$$\begin{aligned}\Delta I_d = {}&(\mu_0\Delta C'_{ox}+C'_{ox0}\Delta\mu+\Delta\mu\Delta C'_{ox})*\frac{W}{2L}\Big((V_{GS}-V_T)^2(1+\lambda(V_{DS}-V_{GS}+V_T))\Big)\\ &-\frac{W}{2L}(\mu_0 C_{ox0}+\mu_0\Delta C_{ox}+C_{ox0}\Delta\mu+\Delta\mu\Delta C_{ox})\Bigg[\\ &\qquad\Delta V_T\Big[\lambda(V_{GS}-V_{T0})^2-2(V_{GS}-V_{T0})*\Big(1+\lambda\big[V_{DS}-(V_{GS}-V_{T0})\big]\Big)\Big]\\ &\qquad+\Delta V_T^2\Big[\Big(1+\lambda\big[V_{DS}-(V_{GS}-V_{T0})\big]\Big)-2\lambda(V_{GS}-V_{T0})\Big]\\ &\qquad+\Delta V_T^3[\lambda]\Bigg]\end{aligned} \tag{28}$$

Observing Eq. **??** combined with the expressions for change in mobility and capacitance (Eqns. 4 and 6), it can be seen that the initial values for mobility and capacitance can both be factored out of the non-ΔV_T term, resulting in a change in drain current as follows (for the linear regime):

$$\begin{aligned}\Delta I_d = {}&I_{d0}\Bigg(\Big(\frac{-\sigma/E_{ox}}{1+\sigma/E_{ox}}\Big)+\Big(\frac{-\pi_L\sigma_L-\pi_T\sigma_T}{1+\pi_L\sigma_L+\pi_T\sigma_T}\Big)+\Big(\frac{-\sigma/E_{ox}}{1+\sigma/E_{ox}}\Big)\Big(\frac{-\pi_L\sigma_L-\pi_T\sigma_T}{1+\pi_L\sigma_L+\pi_T\sigma_T}\Big)\Bigg)\\ &-\Delta V_T V_{DS}\frac{W}{L}\mu_0 C_{ox0}\Bigg(1+\Big(\frac{-\sigma/E_{ox}}{1+\sigma/E_{ox}}\Big)+\Big(\frac{-\pi_L\sigma_L-\pi_T\sigma_T}{1+\pi_L\sigma_L+\pi_T\sigma_T}\Big)+\Big(\frac{-\sigma/E_{ox}}{1+\sigma/E_{ox}}\Big)\Big(\frac{-\pi_L\sigma_L-\pi_T\sigma_T}{1+\pi_L\sigma_L+\pi_T\sigma_T}\Big)\Bigg)\end{aligned} \tag{29}$$

with a similar expression likewise derivable for saturation.

2 Mobility and Velocity Saturation Effects

In sub-micron devices with high lateral fields in the channel region, carrier drift velocity does not exhibit a linear dependence on electric field (constant mobility), but rather saturates as V_{DS} increases [3]. The first notable deviation in velocity comes from phonon scattering, whereby carriers in motion lose energy to the lattice around them. This can be modeled via an effective temperature for the carriers, with drift velocity decreasing as the temperature differential increases [4]:

$$\frac{T_e}{T} = \frac{1}{2}\Bigg[1+\sqrt{1+\frac{3\pi}{8}\Big(\frac{\mu_0 E}{c_s}\Big)^2}\Bigg] \tag{30}$$

$$v_d = \mu_0 E\sqrt{\frac{T}{T_e}} \tag{31}$$

Once the field becomes sufficiently large, carriers may obtain enough energy (E_p) to emit optical phonons. When this kinetic energy is transferred to optical phonons, the carriers must subsequently accelerate again to regain kinetic energy [5]. The maximum rate at which they may travel is given by setting the kinetic energy equal to optical phonon energy and solving for velocity:

$$v_s = \sqrt{\frac{2E_p}{m^*}} \tag{32}$$

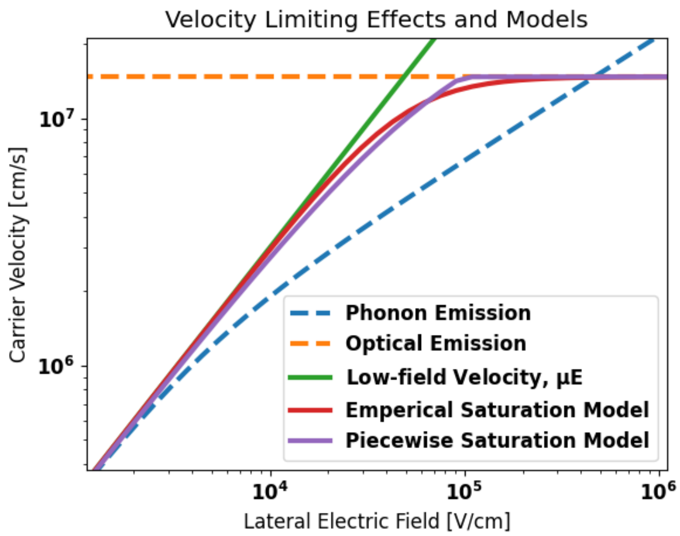

Figure 1: Representative curves for various mobility models. μ=300 cm^2/V*s, $c_s \approx$ 8400 m/s, E_p=63 meV, m^*=0.98, κ=2. Further discussion of the role of optical and acoustic phonon scattering can be found in [6].

To simplify modeling of velocity saturation in compact models, an empirical formula is typically used to encapsulate these effects into a simple equation:

$$v_d = \frac{\mu_0 E}{\sqrt[\kappa]{1 + (\mu_0 E / v_s)^\kappa}} \tag{33}$$

For simplicity in deriving an analytical equation for transistor operation with the presence of velocity saturation, a piece-wise approximation may also be utilized [2]:

$$v_d = \begin{cases} \frac{\mu |E_x|}{1 + |E_x|/E_{sat}} & , \quad |E_x| < E_{sat} \\ v_{sat} & , \quad |E_x| > E_{sat} \end{cases} \tag{34}$$

which, solved at $v_d = v_{sat}$, gives

$$E_{sat} = \frac{2 v_{sat}}{\mu} \tag{35}$$

A comparison of these drift velocity models is shown in Fig. 1, with the understanding that the absolute values of these effects are influenced by doping, device orientation, strain engineering, temperature, and more. For silicon, the two most important phenomena limiting low-field mobility are acoustic-phonon interactions and ionized impurities, with overall mobility calculated as the harmonic mean (Matthiessen rule) of all individual contributions [3].

$$\mu_{ph} = \frac{\sqrt{8\pi} q \hbar^4 C_l}{3 E_{ds}^2 m_c^{*5/2} (kT)^{3/2}} \tag{36}$$

$$\mu_i = \frac{64 \sqrt{\pi} \epsilon_s^2 (2kT)^{3/2}}{N_I q^3 m^{*1/2}} \left[ln \left[1 + \left(\frac{12 \pi \epsilon_s kT}{q^2 N_I^{1/3}} \right)^2 \right] \right]^{-1} \tag{37}$$

Of note is the fact that both mobility and optical phonon emission depend on effective mass, meaning the change in transistor current due to an effect that alters effective mass (such as acoustic deformation of the crystal lattice) will not be subject to velocity saturation like its DC component. Thus, the approach taken in this work is to use a compound model, with unsaturated long-channel expressions used to derive the relative AC change in transistor current and a saturation model, developed hereafter, to obtain the steady-state drain current used for the unstrained initial condition.

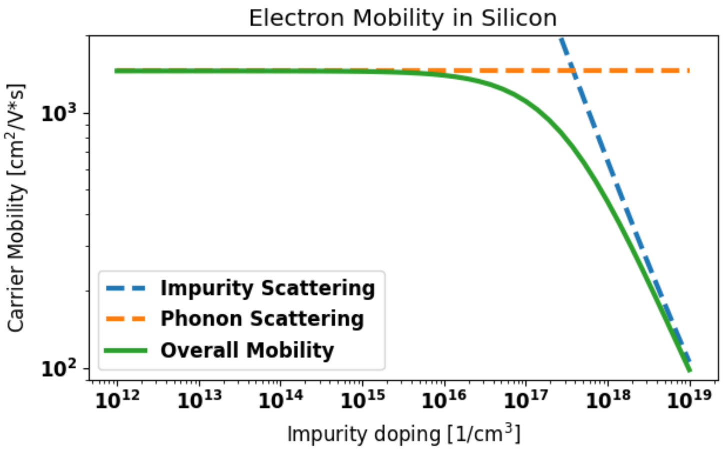

Figure 2: Combination of phonon-limited mobility and impurity-limited mobility via Mattiessen rule results in a familiar shape for mobility of electrons in Si. Exact relations are presented in Equations 36 and 37. T=300 K, m^*=0.98, C_l=165 GPa, ρ=2,329 kg/m^3, ϵ_s=11.9ϵ_0, E_{ds}=-2.7 eV

3 Velocity Saturated Square Law Model

Utilizing the previously mentioned piece-wise model for carrier drift velocity leads to a modified version of the long channel model:

$$I_d = \begin{cases} \mu C_{ox} \dfrac{W}{L} \dfrac{1}{1 + \dfrac{V_{DS}}{E_{sat} L}} \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right) & , \quad V_{DS} < V_{DSsat} \\ \\ C_{ox} W v_{sat} \dfrac{(V_{GS} - V_T)^2}{(V_{GS} - V_T) + E_{sat}(L - \Delta L)} & , \quad V_{DS} > V_{DSsat} \end{cases} \tag{38}$$

where

$$V_{DSsat} = \frac{(V_{GS} - V_T) E_{sat} L}{(V_{GS} - V_T) + E_{sat} L}. \tag{39}$$

In the long channel limit, V_{DSsat} tends towards $V_{GS} - V_T$ and Equation 35 can be used to substitute in for v_{sat}. Furthermore, linearizing the channel length modulation via Taylor expansion

$$\frac{1}{1 - \Delta L/L} \approx 1 + \Delta L/L \tag{40}$$

and taking

$$\Delta L/L = \lambda (V_{DS} - V_{DSsat}) \tag{41}$$

gives the original long channel expression, shown in Equation 27.

The end result of this is that the DC saturation current no longer scales quadraticly with $V_{GS} - V_T$ but rather linearly reduces the overall current. While the simultaneous change in mobility and saturation velocity with stress prevents AC current waveforms from clipping, this does reduces the magnitude of the mobility and oxide capacitance modulation terms that are linearly proportional to steady-state drain current.

4 Berkeley Short-channel IGFET Model - Common Metal Gate (BSIM-CMG)

The standard model for commercial devices, the BSIM-CMG model [7], captures many additional effects that exist in highly scaled and non-planar FETs through a mixture of physical and semi-empirical modeling based on hundreds of input parameters. The underlying BSIM-CMG equation for I_{DS} is given as:

$$I_{DS} = IDS0MULT * \mu_0(T) * C_{ox} * \frac{W_{eff} * NFIN_{total}}{L_{eff}} * i_{ds0} * \frac{M_{oc}M_{ob}M_{nud}}{D_{mob}D_rD_{vsat}} \tag{42}$$

where $IDS0MULT$ is a scaling factor (default value of 1), $NFIN_{total}$ is the number of fins in parallel, W_{eff} and L_{eff} are the effective channel width and length, C_{ox} is the gate oxide capacitance, and $\mu_0(T)$ is the temperature-dependent bulk low-field mobility. These values can be directly mapped to the simplified analytical model fit to the data, with $NFIN_{total}$ multiplied into the width. The last term in Equation 42 consists of current multipliers for various effects including M_{ob} for the body effect (equal to 1 except in the case of decoupled bulk multigate transistors), M_{nud} for non-uniform doping (empirically derived from measurement data), and M_{oc}, which accounts for channel length modulation (present in our model) as well as drain induced barrier lowering (less than 0.02 V/V in these devices). Divisors include D_{mob} for vertical field mobility degradation, D_r for source/drain resistance, and D_{vsat} for velocity saturation. Of these, the simplified analytic model handles only the last, with vertical field degradation being a likely candidate for the decreased performance seen at high gate biases in experimental devices.

5 Model Fit Report

```
[[Model]]
    Model(Id_DC_lmfit)
[[Fit Statistics]]
    # fitting method   = basinhopping
    # function evals   = 1862
    # data points      = 81
    # variables        = 6
    chi-square         = 1.4881e-08
    reduced chi-square = 1.9842e-10
    Akaike info crit   = -1803.82554
    Bayesian info crit = -1789.45884
##  Warning: uncertainties could not be estimated:
    this fitting method does not natively calculate uncertainties
    and numdifftools is not installed for lmfit to do this. Use
    `pip install numdifftools` for lmfit to estimate uncertainties
    with this fitting method.
[[Variables]]
    u0:     0.00500636 (init = 0.03)
    eot:    1.1953e-09 (init = 1e-09)
    Vt0:    0.23980455 (init = 0.3)
    vsat:   271628.267 (init = 200000)
    clm:    0.23573658 (init = 0.3)
    Weff0:  3.9177e-06 (init = 3.2e-06)

[[Model]]
    Model(delId_vsat_lmfit)
[[Fit Statistics]]
    # fitting method   = leastsq
    # function evals   = 79
    # data points      = 81
    # variables        = 3
    chi-square         = 8.9548e-13
    reduced chi-square = 1.1481e-14
    Akaike info crit   = -2597.00481
    Bayesian info crit = -2589.82146
[[Variables]]
    stressx:  951297.581 +/- 3062959.59 (321.98%) (init = 1000000)
    stressy:  10000.3346 +/- 3040116.12 (30400.14%) (init = 1000000)
    stressz:  10000.0053 +/- 304759.605 (3047.59%) (init = 1000000)
[[Correlations]] (unreported correlations are < 0.100)
    C(stressx, stressy) = -0.998
    C(stressy, stressz) =  0.989
    C(stressx, stressz) = -0.979
```

6 Supplemental Figures

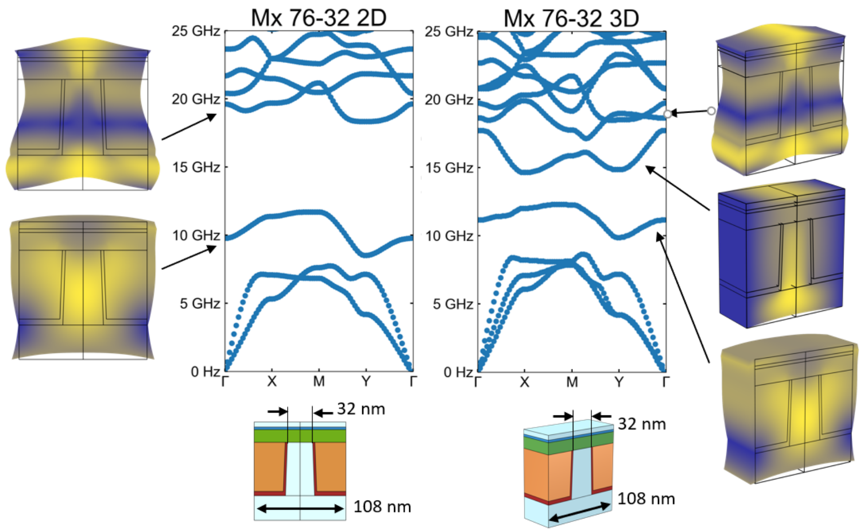

Figure 3: Results of 3D (left) vs 2D (right) simulations of the 76×32 PnC band structure, highlighting how the 2D simulation fails to capture modes with a transverse component. This increases the possible modes that energy may scatter into, reducing the complete bandgap provided by the PnC. Structure simulated with Floquet periodic boundaries with out-of-plane momentum (for the 3D cell) set to 0.

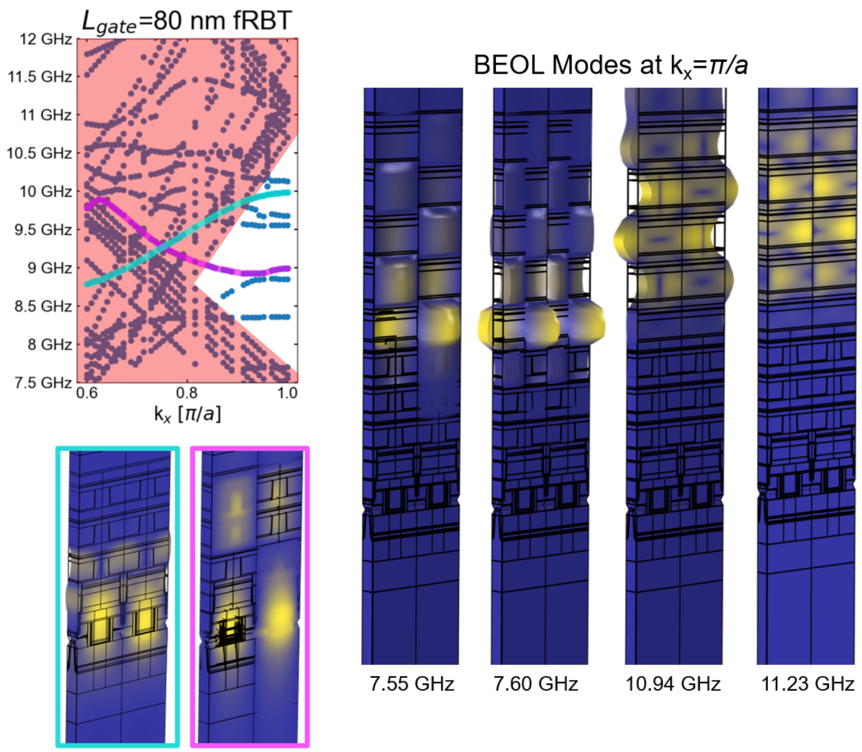

Figure 4: 80 nm gate length dispersion relation, highlighting the FEOL waveguided modes as well as some of the propagating modes that exist in the sound cones of the plate layers. For the 80 nm fRBT these cones reach π/a around 7.5 and 11 GHz and then fold back on themselves due to the uniform nature of the plates [8]. For longer gate length devices, a will be larger and the Brillouin zone will shrink, causing these cones to intersect at lower frequencies ($\omega = vk$).

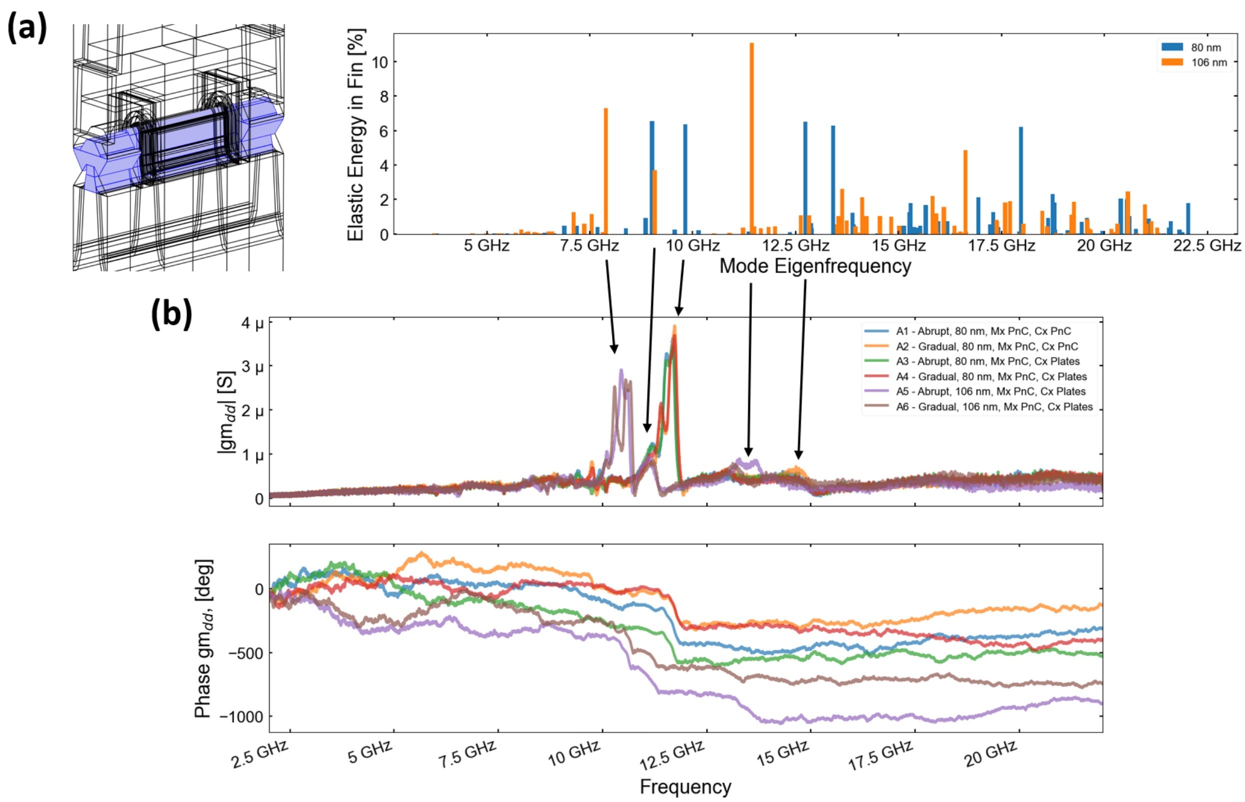

Figure 5: **(a)** Highlighted fin over which the percentage of mode elastic energy is calculated, shown in graph at right for 80 and 106 nm unit cell. **(b)** Experimentally measured differential transconductance from 2 to 22 GHz for Mx PnC confined devices. Shifting the simulated frequency axis by the approximately 2 GHz offset experimentally seen in the target mode results in good alignment between anticipated and measured FEOL mode spectra. Lack of modes visible in measurement at higher frequencies is likely due to lack of confinement, as these exist within the sound cone of the BEOL (and eventually Si substrate) layers.

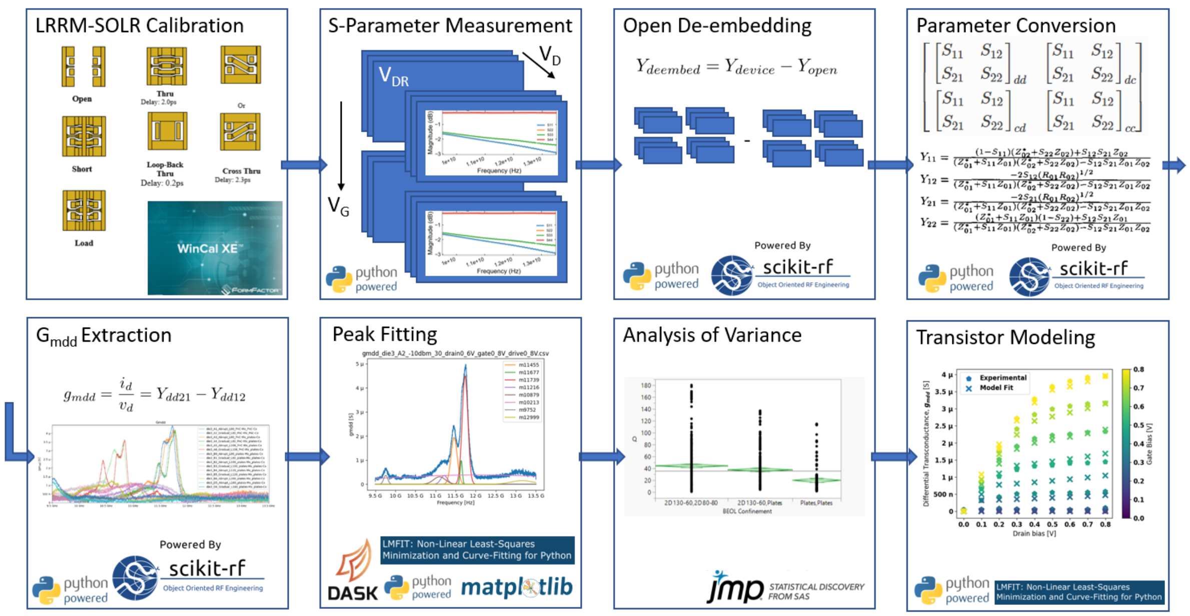

Figure 6: Overview of the data pipeline utilized for analysis of the fRBT devices. Measurements corrected to probe tip with an LRRM-SOLR calibration are de-embedded down to the fRBT unit cell using an on-chip open. These corrected parameters are then converted to mixed-mode to allow for differential analysis and g_{mdd} extraction. For analyzing design splits, peak fitting of the measurements is performed followed by ANOVA. For transistor modeling, peak g_{mdd} with the measurement floor subtracted is extracted from experimental data and fit to the discussed model.

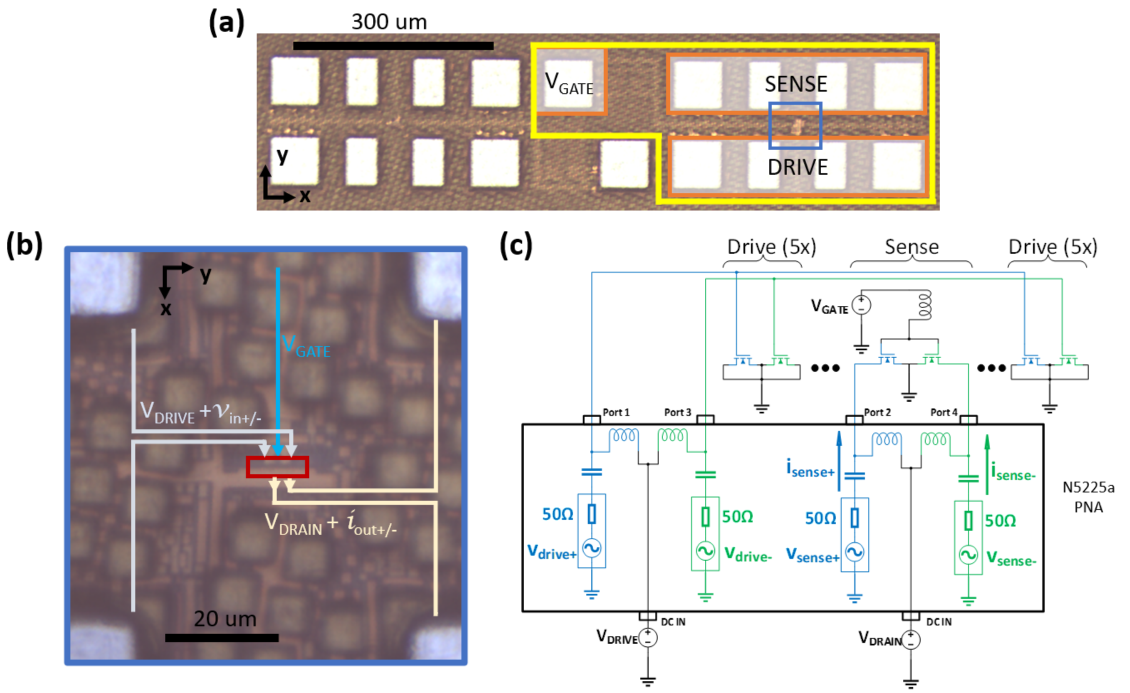

Figure 7: **(a)** Die micrograph showing two adjacent resonators, with GSSG pads for the rf drive and sense and a DC pad for gate biasing. **(b)** Close-up view from center of device in **(a)**, showing the approximate resonator location, dimensions, and signal routing underneath the BEOL metal layers. **(c)** Device measurement setup, with differential RF input applied via ports one and three of a Keysight N5225a Performance Network Analyzer (PNA). Differential output current measured via ports two and four. DC gate bias is applied directly from a Keithley 2400 Source Measure Unit (SMU) via needle probe, while the drive and drain biases are applied via SMU through the PNA using the built-in bias-tee.

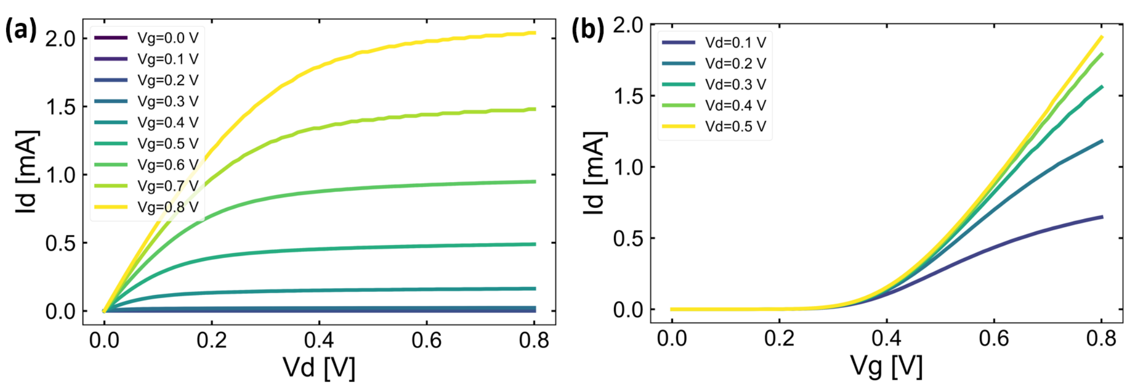

Figure 8: Experimental **(a)** family of curves and **(b)** $I_D - V_G$ DC bias currents for A1 resonator with 80 nm gate length. Curves are representative of all devices, with absolute value of current scaling with channel length. Drain currents reported are high due to the large width of the sense transistors, which comprise of 40 fins in parallel.

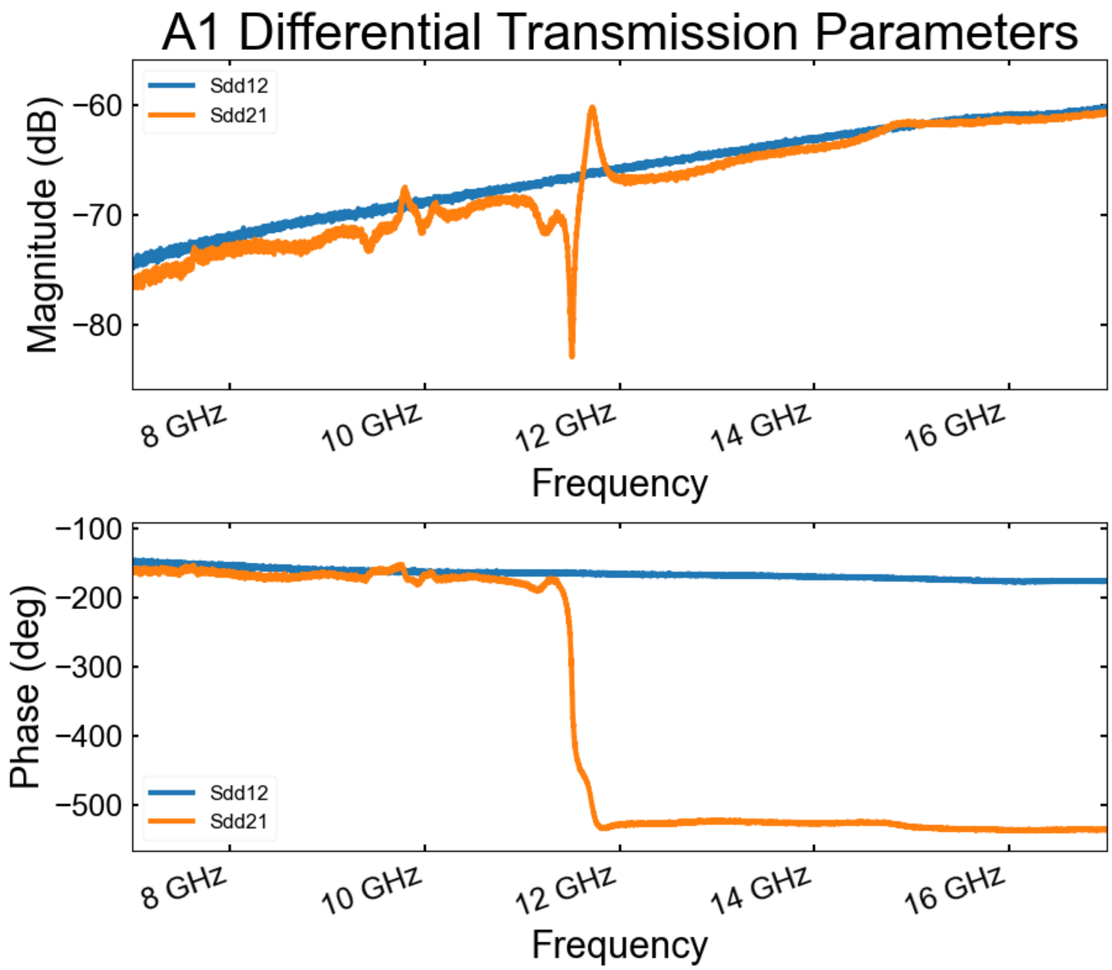

Figure 9: Experimental S_{dd} transmission parameters, showing nonreciprocal behaviour with resonance only in S_{dd21}. This confirms the modes are actively sensed, highlighting the impact of active transduction in overcoming large feedthrough capacitance in integrated devices.

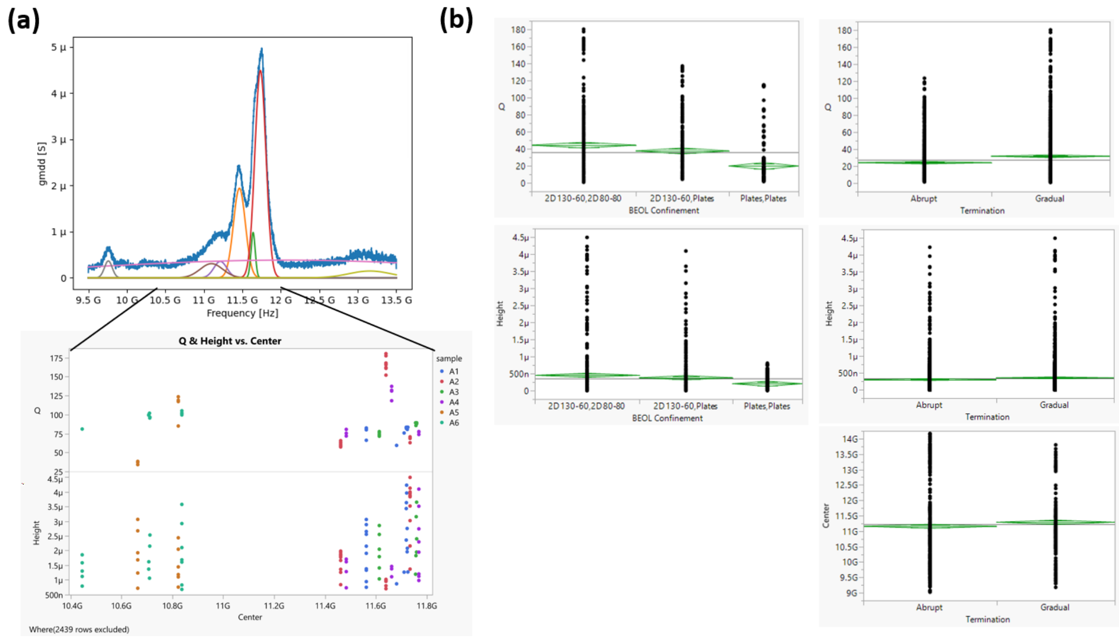

Figure 10: **(a)**: Output of peak fit algorithm for one of the 392 individual measurements evaluated. Peak fits with error above 0.025 were filtered (120 out of 2554 peaks) and then design splits were evaluated via ANOVA between appropriate samples. Lower plot shows Q and amplitude of fit resonance peaks, filtered by a minimum Q of 25 and height of 750 nS, with each dot indicating a peak of the correspondingly colored device under a single bias condition. Transconductance variations at the same frequency show the dependence of the resonance on electrical biases. Also evident is the change in center frequency due to gate length, and splitting from two to three distinct modes with gradual termination, as first shown in Fig. **??**. Impacts of BEOL confinement and lateral termination, are shown in **(b)**, with complete results given in Table 1. Diamonds centered on mean and extend to 95% confidence interval. In addition to increasing average peak height and Q across a range of drive and drain biases, it is also evident that an Mx-PnC greatly increases the maximum peak height, from under 1 μS to 4.5 μS for the highest-performing resonator.

Table 1: ANOVA Results for Peak Fits

95% Confidence Intervals Significant results in bold.		n	Frequency [Hz]		Height [nS]		Q		Samples
			Mean	Std. Error	Mean	Std. Error	Mean	Std. Error	
PnC Confinement	Mx, Cx	413	11.27 G	52.8 M	**451.1**	**30.6**	**44.32**	**1.68**	A1-A4, B0-B1 (L_{gate}=80 nm)
	Mx Only	368	11.22 G	55.9 M	**379.4**	**32.5**	**37.55**	**1.78**	
	Plates	276	11.26 G	64.6 M	**203.6**	**37.5**	**19.88**	**2.05**	
Termination	Abrupt	1289	**11.16 G**	**33.4 M**	**301.6**	**13.9**	**24.21**	**0.795**	All
	Gradual	1145	**11.29 G**	**35.4 M**	**352.4**	**14.7**	**31.71**	**0.843**	
L_{gate}	80 nm	30	**11.66 G**	**23.0 M**	1,866	153	84.8	4.40	A3-A6 Q>25, Height>500 nS
	106 nm	30	**10.71 G**	**23.0 M**	1,651	153	87.1	4.40	

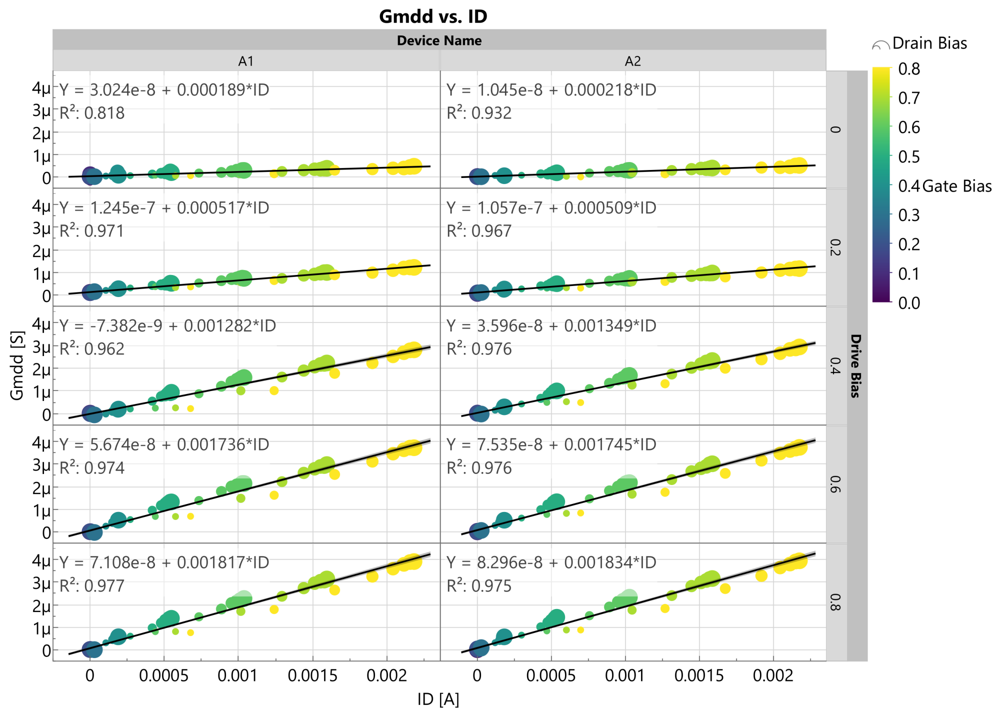

Figure 11: Trend in differential transconductance of largest mode (≈11.75 GHz) for A1 and A2 resonators (80 nm gate length, Mx and Cx phononic crystal confinement). g_{mdd} (Y-axis) is plotted against DC bias current of the sense transistor (X-axis), tiled by device (X tiles) and drive bias (Y tiles). Gate bias is shown by marker color (blue to yellow), with gate biases of 0.3 V and below overlapping near zero drain current (subthreshold). Drain bias is represented with marker size, moving from small to large as bias increases. The large cluster of points with equal gate biases and similar drain currents indicate saturation mode operation for those bias conditions with channel length modulation. Peak g_{mdd} increases as a function of drive bias and is largely dependent on drain current of sense transistor, although efficiency drops as gate voltage increases. Very low drain biases also tend to be less efficient than saturation mode biasing for a given device current.

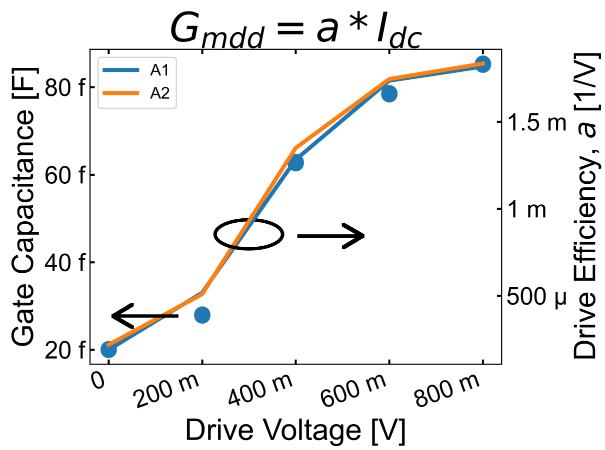

Figure 12: Observed drive efficiency of resonators from the linear fits shown in Fig. 11 plotted alongside extracted capacitance from drive transducers vs drive bias on the X-axis indicating that transduction efficiency is dominated by the large change in capacitance in these devices over the small allowable voltage range.

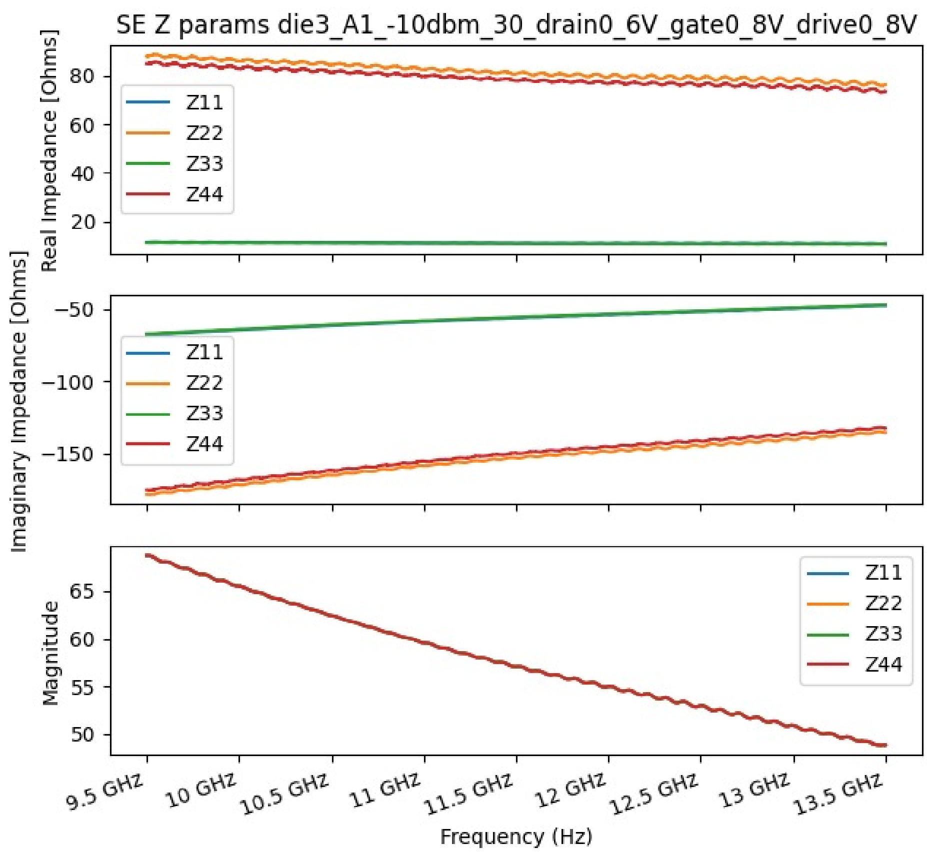

Figure 13: Experimentally measured resonator impedance at input (ports 1 and 3) and output (ports 2 and 4), used to calculate the gate capacitance at each drive bias shown above.

References

[1] Bardeen, J. & Shockley, W. Deformation Potentials and Mobilities in Non-Polar Crystals. *Physical Review* **80**, 72–80 (1950). URL `https://link.aps.org/doi/10.1103/PhysRev.80.72`.

[2] Tsividis, Y. & McAndrew, C. *Operation and Modeling of the MOS Transistor* (Oxford University Press, New York, 2010), 3 edition edn.

[3] Sze, S. M. & Ng, K. K. *Physics of Semiconductor Devices* (John Wiley & Sons, 2006). Google-Books-ID: o4unkmHBHb8C.

[4] Moll, J. L. *Physics of Semiconductors* (McGraw-Hill, 1964).

[5] Mitin, V., Mitin, V. V., Kochelap, V. & Stroscio, M. A. *Quantum Heterostructures: Microelectronics and Optoelectronics* (Cambridge University Press, 1999). Google-Books-ID: Wzo4IdxS48oC.

[6] Conwell, E. Lattice mobility of hot carriers. *Journal of Physics and Chemistry of Solids* **8**, 234–239 (1959). URL `https://www.sciencedirect.com/science/article/pii/0022369759903245`.

[7] BSIM Group. URL `http://bsim.berkeley.edu/`.

[8] Joannopoulos, J. D., Johnson, S., Winn, J. & Meade, R. *Photonic crystals : molding the flow of light* (2008), 2nd edn.