

An elastic and reconfigurable synaptic transistor based on a stretchable bilayer semiconductor

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Supplementary Information

An elastic and reconfigurable synaptic transistor based on a stretchable bilayer semiconductor

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Supplementary Notes

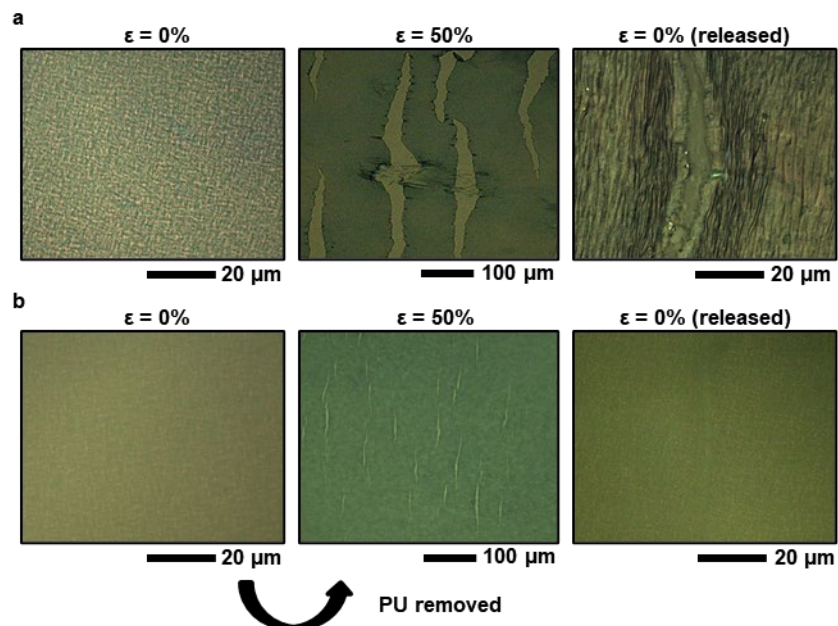
1. Calculation of mobility and threshold voltage

The field-effect mobilities (μ_{FE}) were obtained from the output current versus voltage in the saturation region. We fitted the plot of $\sqrt{I_{ds}}$ versus V_{gs} and extracted the mobilities based on following equation:

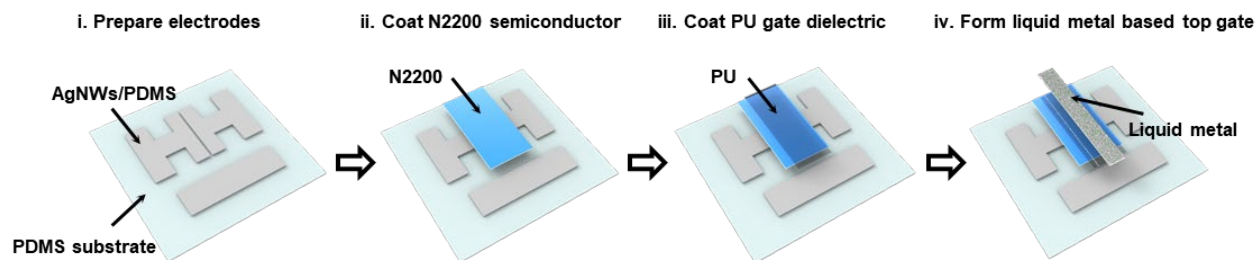
$$I_{ds} = \left(\frac{WC_i}{2L}\right) \mu_{FE} (V_{gs} - V_{th})^2 \quad (S1)$$

where L, W, and C_i are the channel length, the width, and the gate capacitance per unit area, respectively. The x-intercept of the extrapolation of the fitted curve defines the threshold voltage (V_{th}).

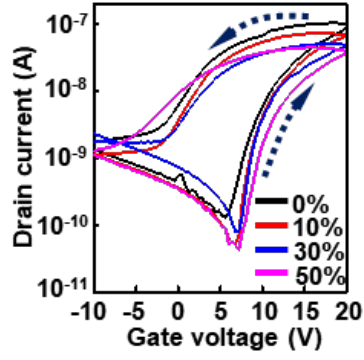
Supplementary Figures



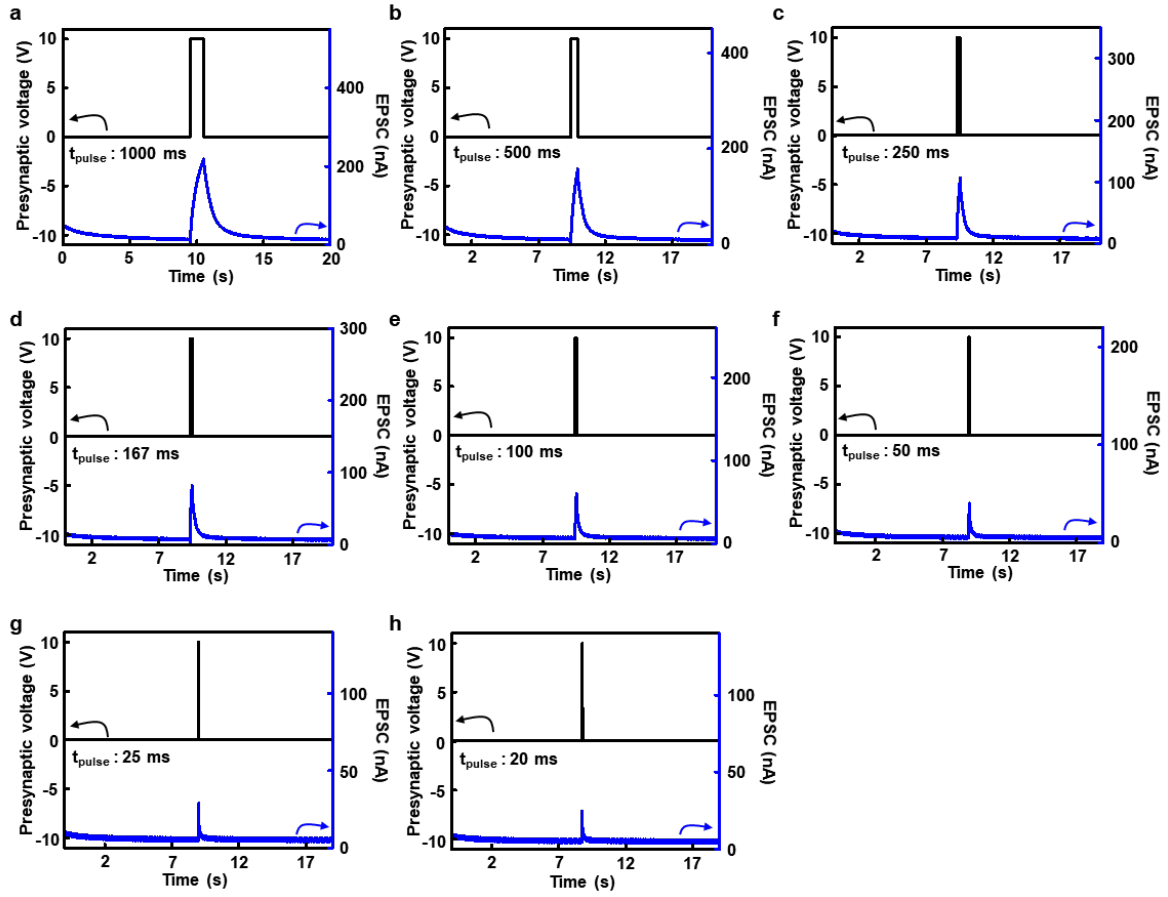
Supplementary Figure 1. Optical microscope images of the N2200 films under strain. a, Bare N2200 thin film on PDMS without PU encapsulation after stretching by 50% and then relaxed. Many microcracks present when stretched by 50%. **b,** N2200 thin film on PDMS with PU encapsulation after stretching by 50% and then relaxed. Only a few microcracks with much smaller crack size compared with the bare N2200 film exist.



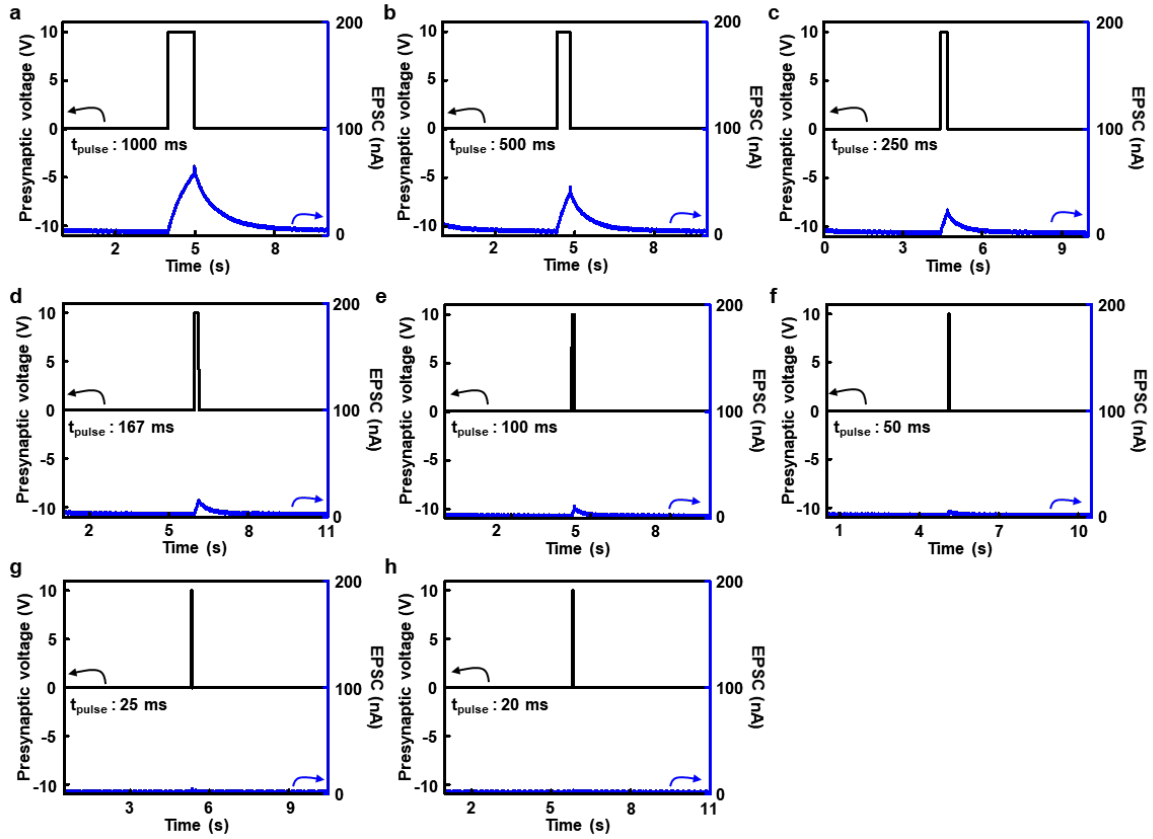
Supplementary Figure 2. Schematic illustration of the detailed fabrication procedure and steps for synaptic transistor based on the thin stretchable N2200 thin film.



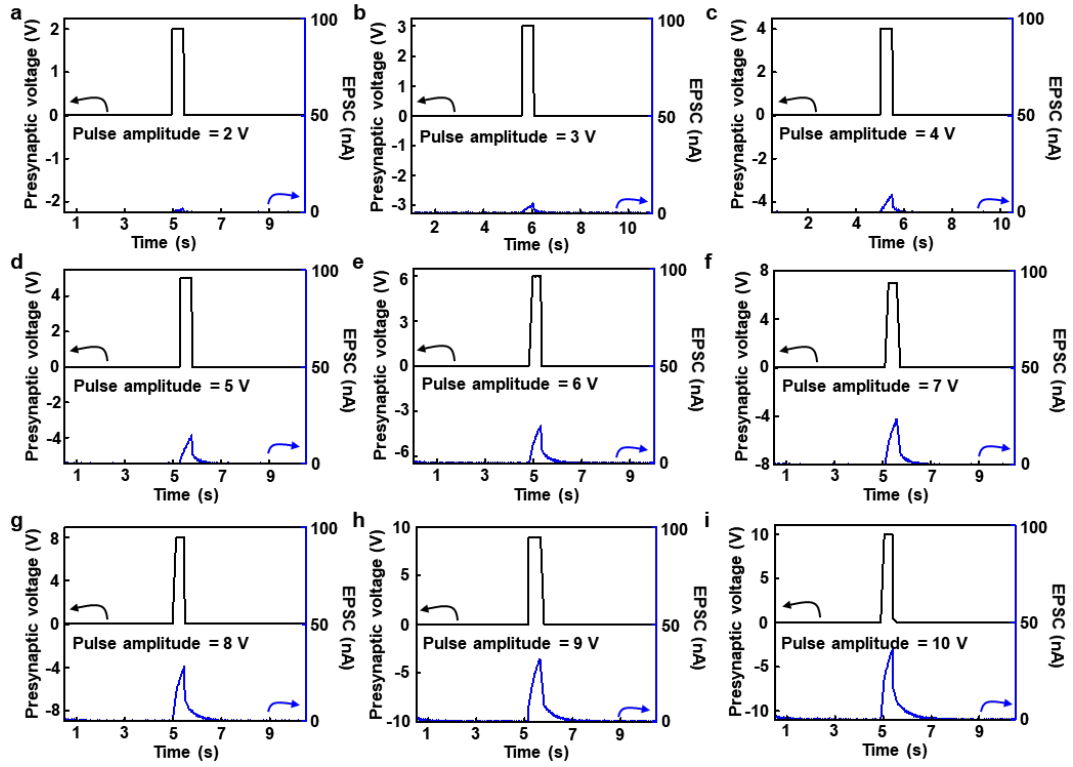
Supplementary Figure 3. The transfer curves of the transistor under mechanical strains of 0, 10, 30, and 50% perpendicular to the channel length direction.



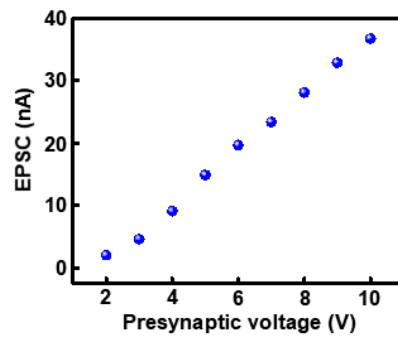
Supplementary Figure 4. The EPSC peaks as a function of the pulse duration for the device without mechanical strain. a-h, pulse duration of 1000, 500, 250, 167, 100, 50, 25, and 20 ms, respectively.



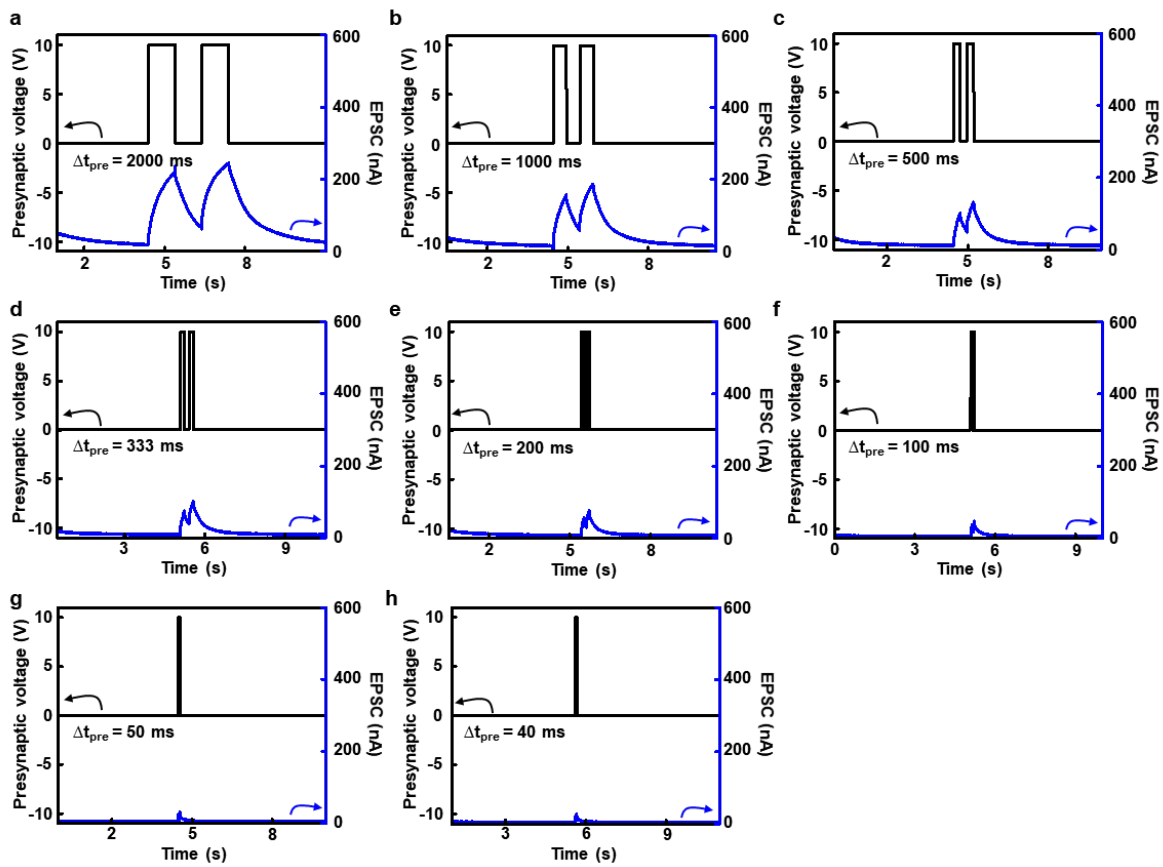
Supplementary Figure 5. The EPSC peaks as a function of the pulse duration for the device with 50% strain. a-h, pulse duration of 1000, 500, 250, 167, 100, 50, 25, and 20 ms, respectively.



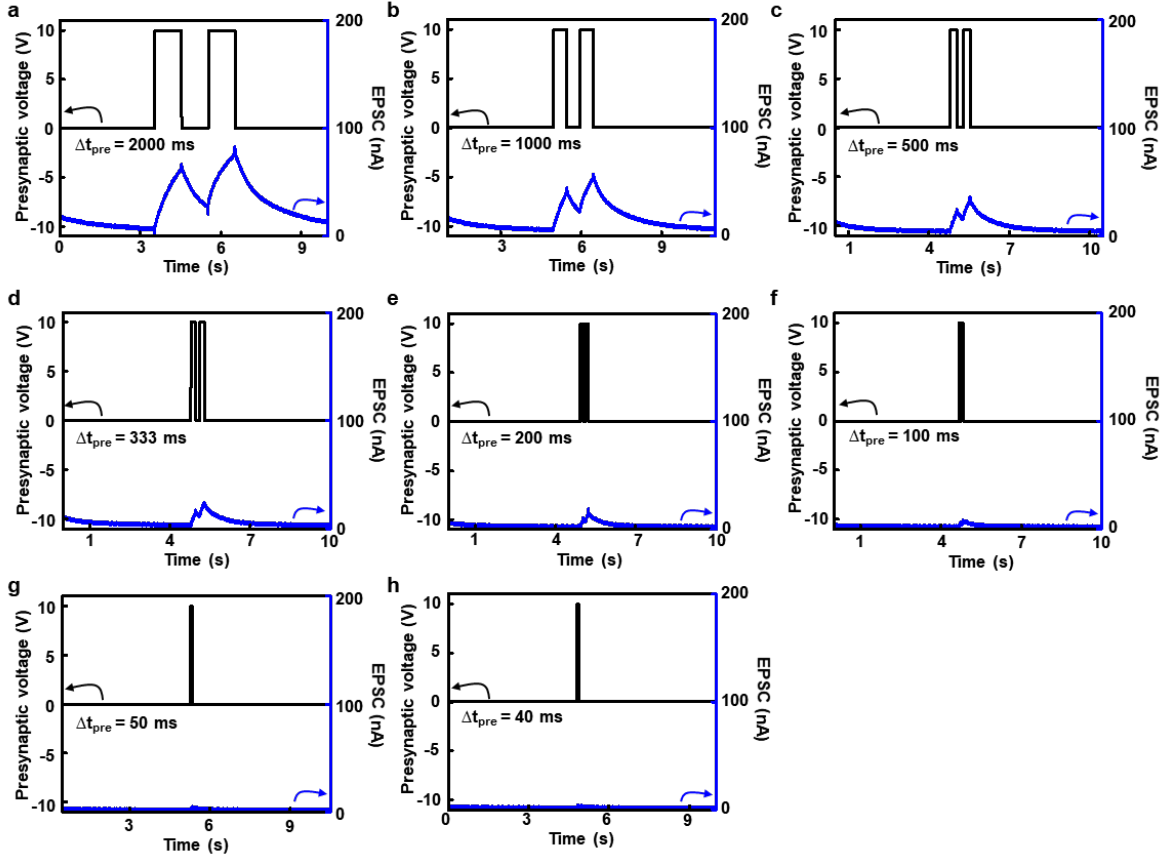
Supplementary Figure 6. The EPSC peaks as a function of presynaptic pulse amplitude. a-h, pulse amplitude of 2, 3, 4, 5, 6, 7, 8, 9, and 10 V, respectively.



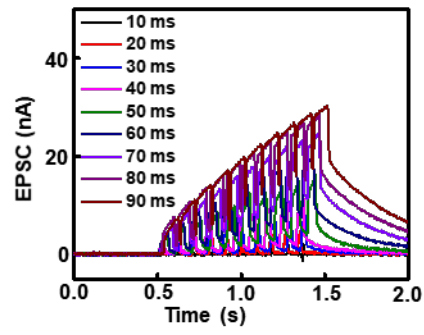
Supplementary Figure 7. Summarized EPSC peaks as a function of presynaptic pulse amplitude, ranging from 2 to 10 V.



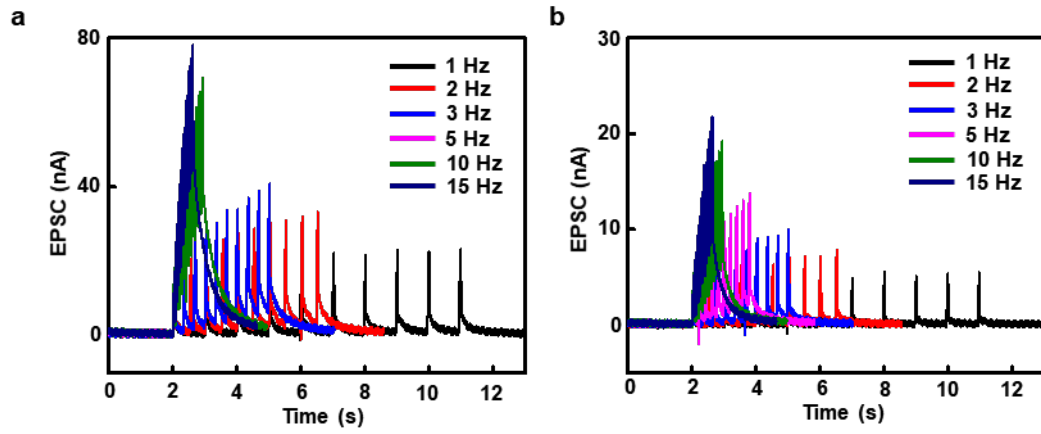
Supplementary Figure 8. EPSC results for different Δt_{pre} for the synaptic transistor without strain. a-h, Δt_{pre} of 2000, 1000, 500, 333, 200, 100, 50, and 40 ms, respectively.



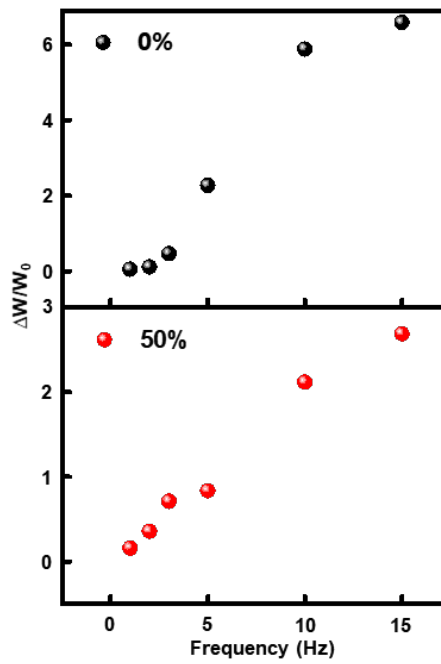
Supplementary Figure 9. EPSC results for different Δt_{pre} for the synaptic transistor with 50% strain. a-h, Δt_{pre} of 2000, 1000, 500, 333, 200, 100, 50, and 40 ms, respectively.



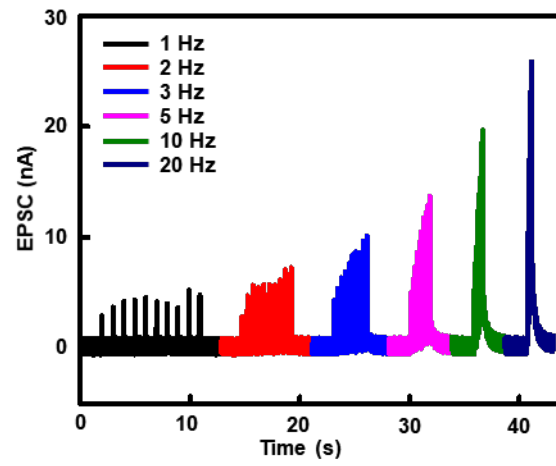
Supplementary Figure 10. Summarized memory characteristics results for the synaptic transistor under 50% with different pulse widths from 10 to 90 ms.



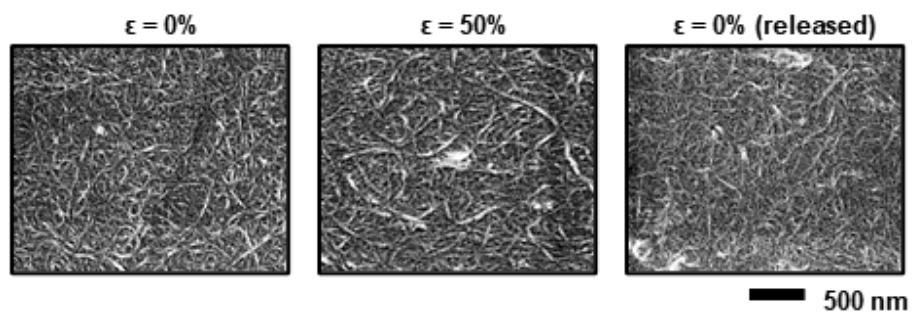
Supplementary Figure 11. The memory characteristics of 10 successive presynaptic pulses (+10 V, 50 ms) with variable frequencies from 1 to 15 Hz. a, 0% strain. b, 50% strain.



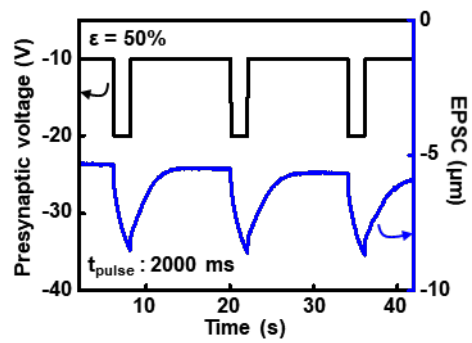
Supplementary Figure 12. The trend of $\Delta W/W_0$ from 10 successive presynaptic pulses with different pulse frequencies from 1 to 15 Hz without any strain and with 50% strain.



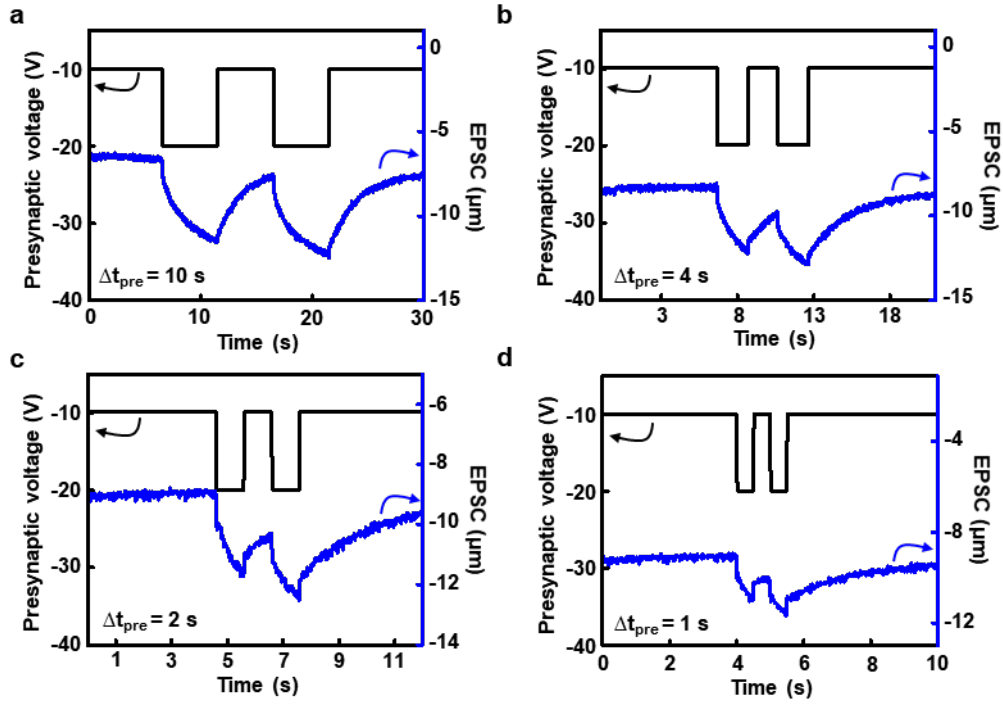
Supplementary Figure 13. Summarized high-pass filter characteristics for the synaptic transistor with 50% strain from 10 successive presynaptic pulses with different pulse frequencies from 1 to 20 Hz.



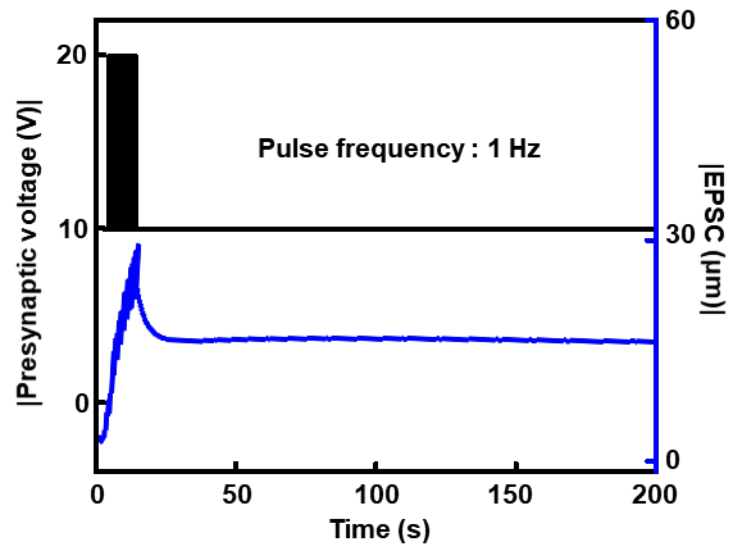
Supplementary Figure 14. The SEM images of s-CNT network under mechanical strain.



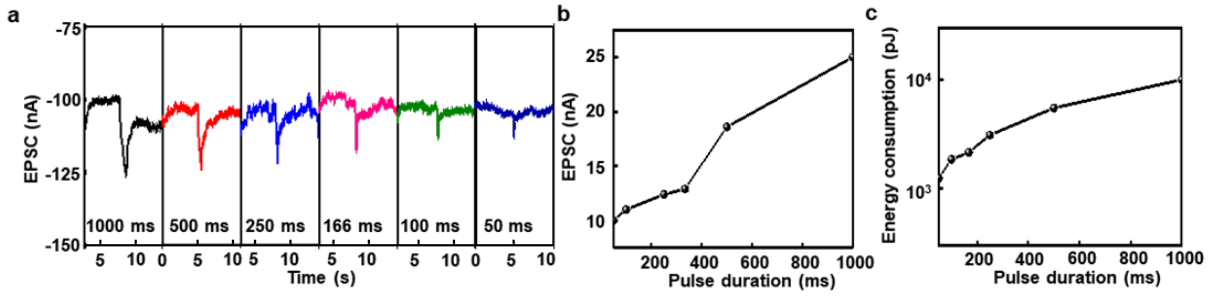
Supplementary Figure 15. The single pulse-induced EPSC results for the synaptic transistor with 50% strain.



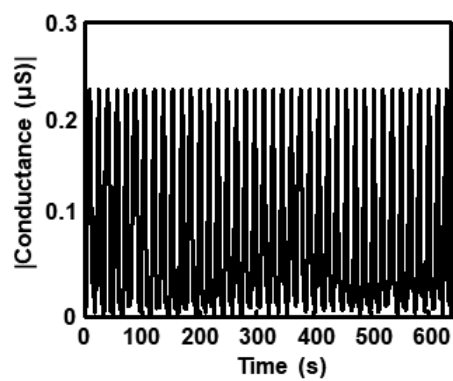
Supplementary Figure 16. The detailed EPSC results with different pulse interval (Δt_{pre}) for the synaptic transistor under 50% strain. **a-d**, pulse interval of 10, 4, 2, and 1 s, respectively.



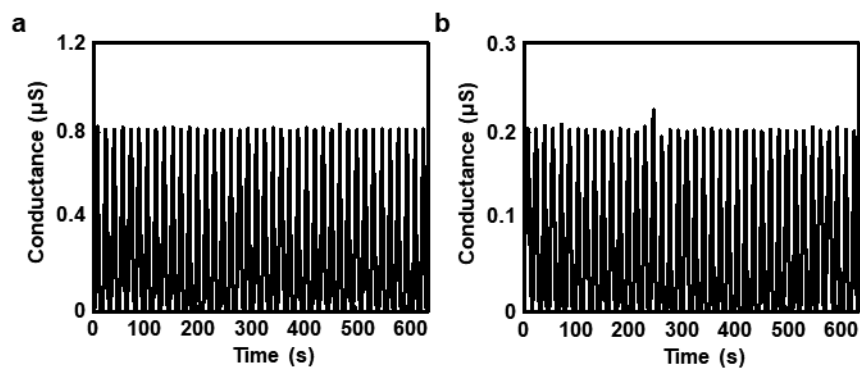
Supplementary Figure 17. The LTM characteristics during a longer time.



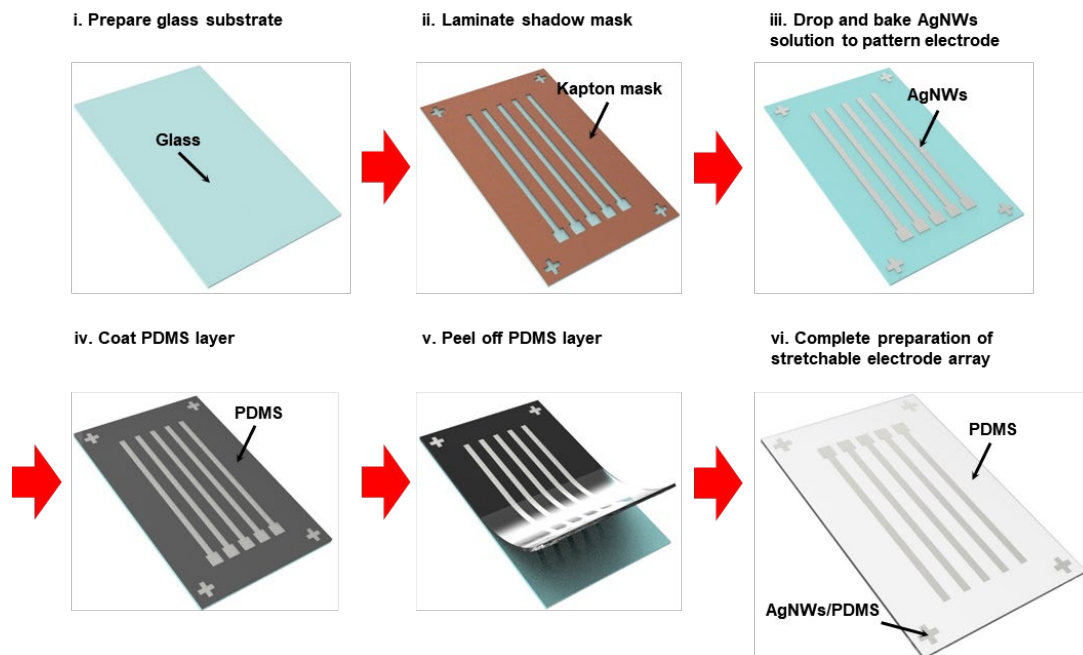
Supplementary Figure 18. The EPSC results and the energy consumption of the device. a, The single pulse-induced EPSC results. **b,** The peak current of the EPSC in **a**. **c,** The energy consumption with respect to the pulse duration in **a**.



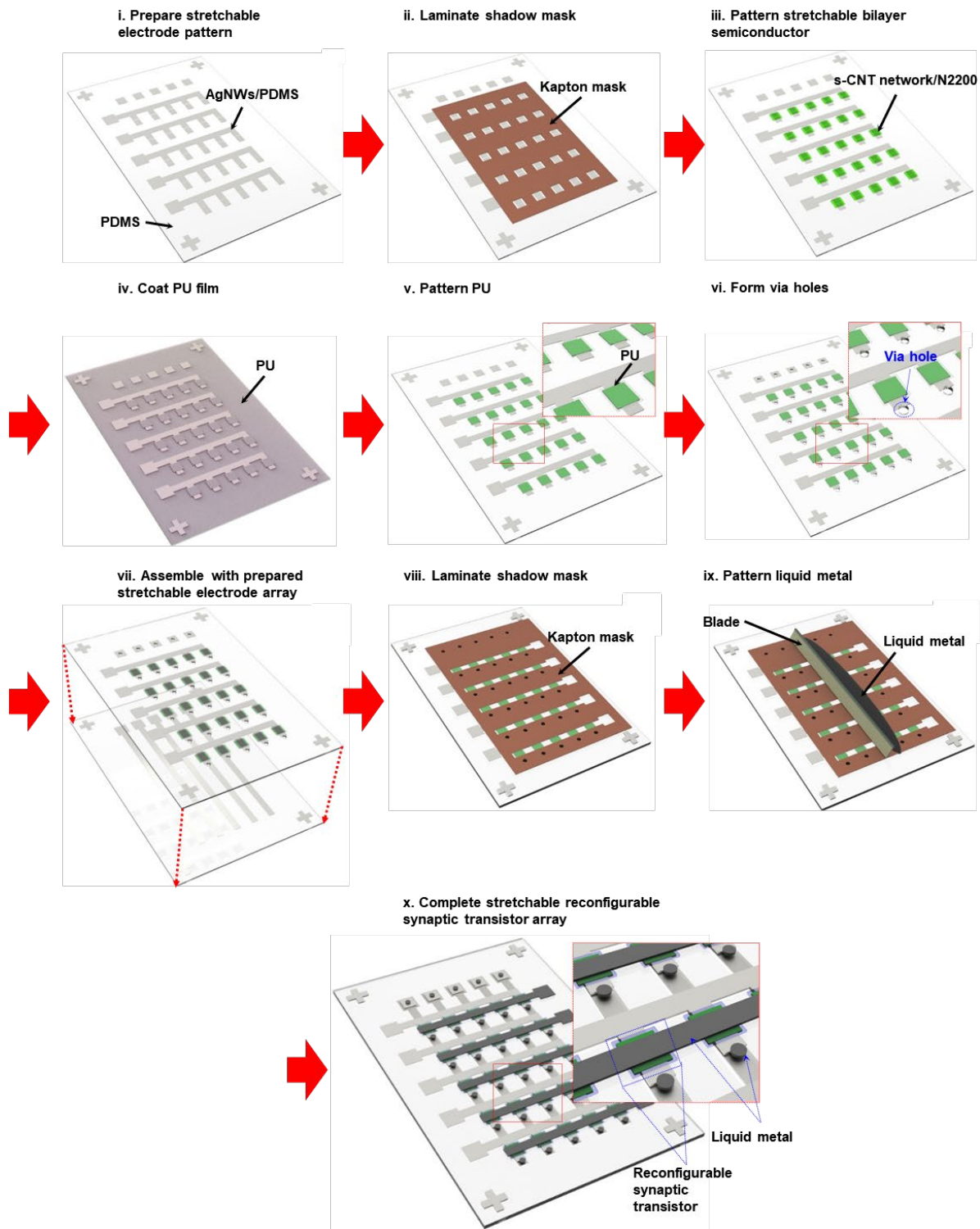
Supplementary Figure 19. The measured linear potentiation and depression during 40 cycles in p-type operation (excitatory synapse, $V_{ds} < 0$).



Supplementary Figure 20. The measured linear potentiation and depression during 40 cycles in n-type operation (excitatory synapse, $V_{ds} > 0$). a, 0% strain. b, 50% strain.



Supplementary Figure 21. The fabrication procedure of the stretchable AgNWs/PDMS electrode array.



Supplementary Figure 22. The fabrication procedure of the stretchable reconfigurable synaptic transistor array.