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Article

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Wafer-scale alignment and integration of micro-light-emitting diodes using engineered van der Waals forces

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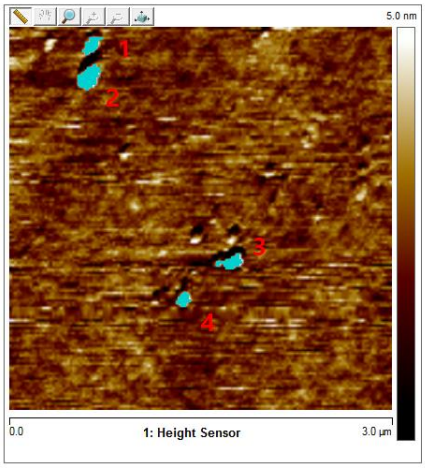
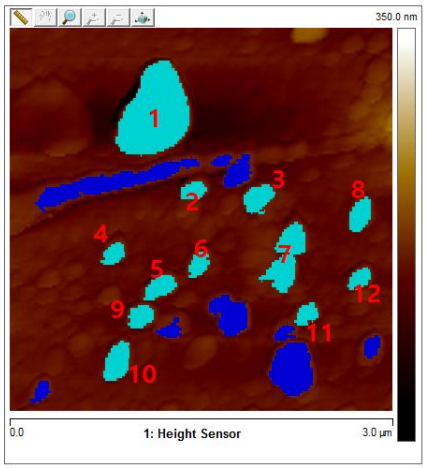
a



b



c

	y_{max} (nm)	r (nm)
1	5.43	64.0
2	9.20	88.0
3	9.35	67.0
4	4.90	55.0

d

	y_{max} (nm)	r (nm)
1	151	306
2	37.7	86.5
3	53.9	113
4	28.7	86.5
5	45.4	103
6	30.4	88.5
7	48.3	177
8	31.9	108
9	32.3	97.0
10	48.0	125
11	33.8	87.0
12	40.7	86.0

Figure S1. Particle analysis of AlN and Au faces Particle analysis results of AlN **a,** and Au **b,** faces. The extracted values of y_{max} and r are shown in AlN **c,** and Au **d,** faces. Each particle detected by the software was numbered. In d, only the particle of No. 1 with y_{max}=151 nm was considered to calculate the vdW force because large difference of y_{max} compared to other particles.

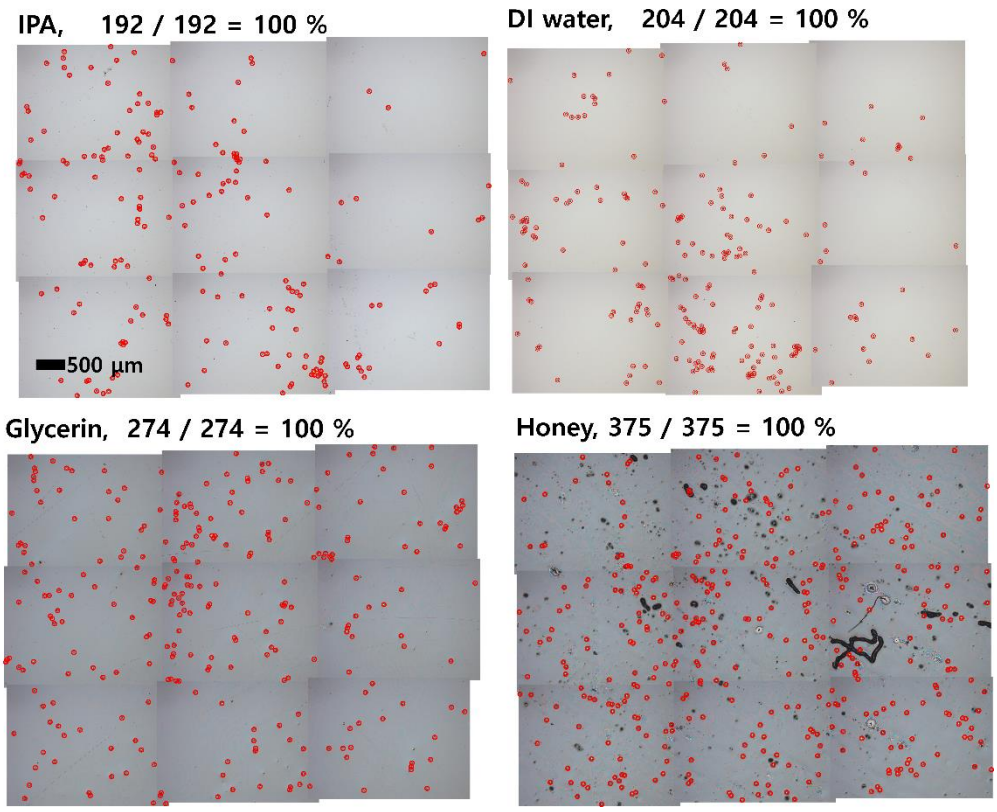


Figure S2. Single-face alignment results under different solvents Single-face alignment results under different solvents of IPA, DI water, glycerin, and honey (# of AlN↓ chips / # of all chips = 100 % for different solvents). The viscosity of IPA, DI water, glycerin and honey are 2, 1, 1500, and larger than 7,000 mPa·s. Also, IPA and DI water solvent shows large different surface tension of 21.7 and 71.9 dyn/cm, respectively.

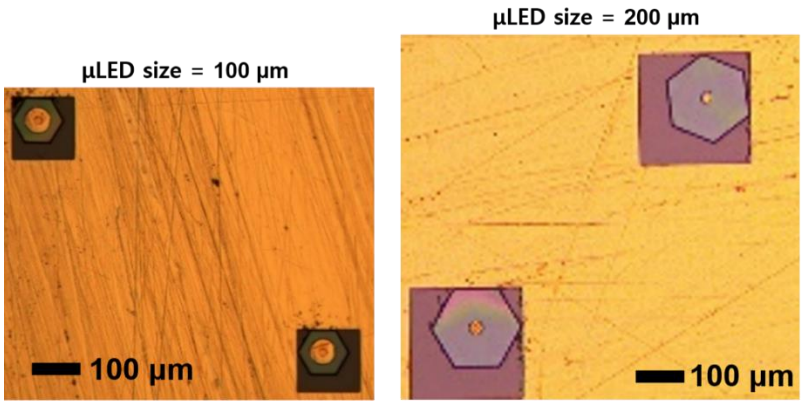


Figure S3. Transfer of mini LED in the mold Various size and shape of mini LED chips ranging from 100 to 200 µm

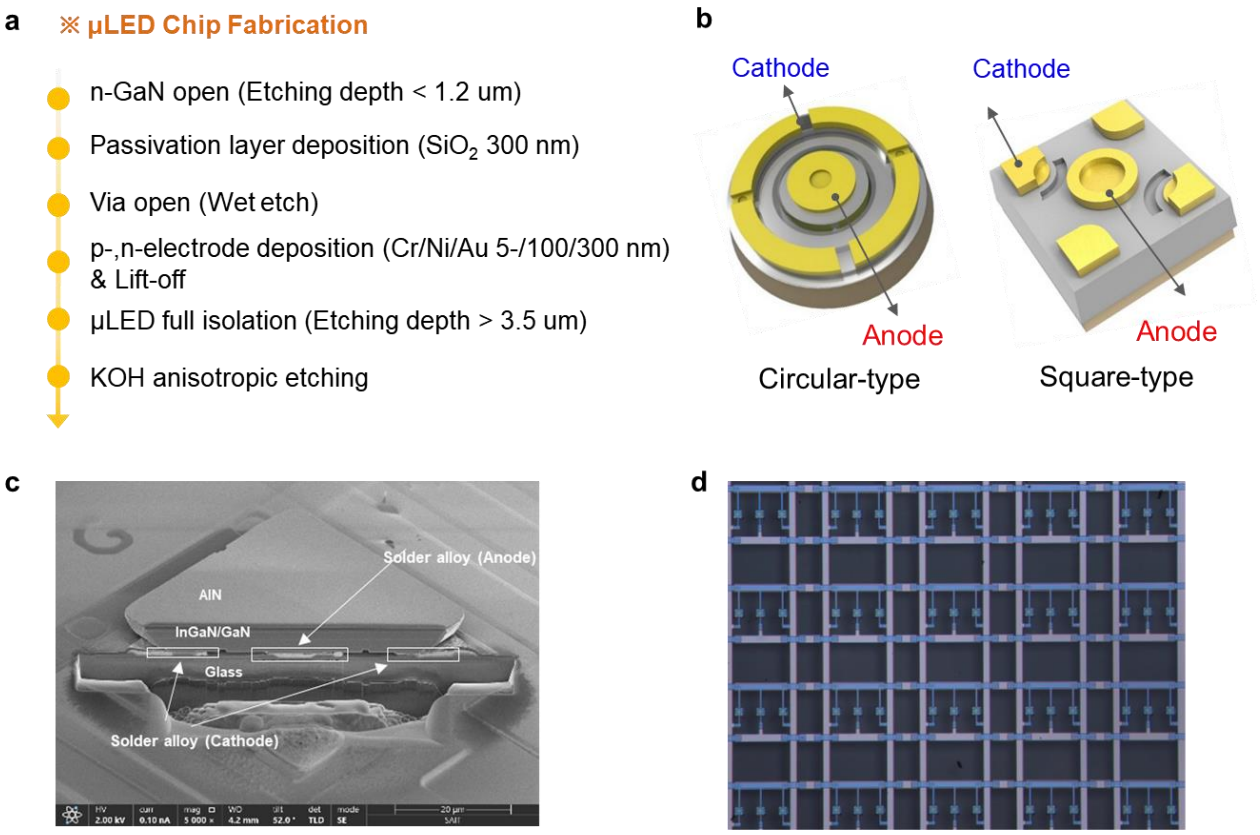


Figure S4. Fabrication and integration of µLED chip a, Summary of the µLED chip fabrication process with four photomasks. **b**, Schematic 3D illustration of the fabricated circular- and square-type µLED chips. **c**, A FIB-SEM image of the µLED chip (40 µm size) after integration. **d**, An optical image of the integrated panel. Each pixel consists of three µLED chips that can be addressed independently.

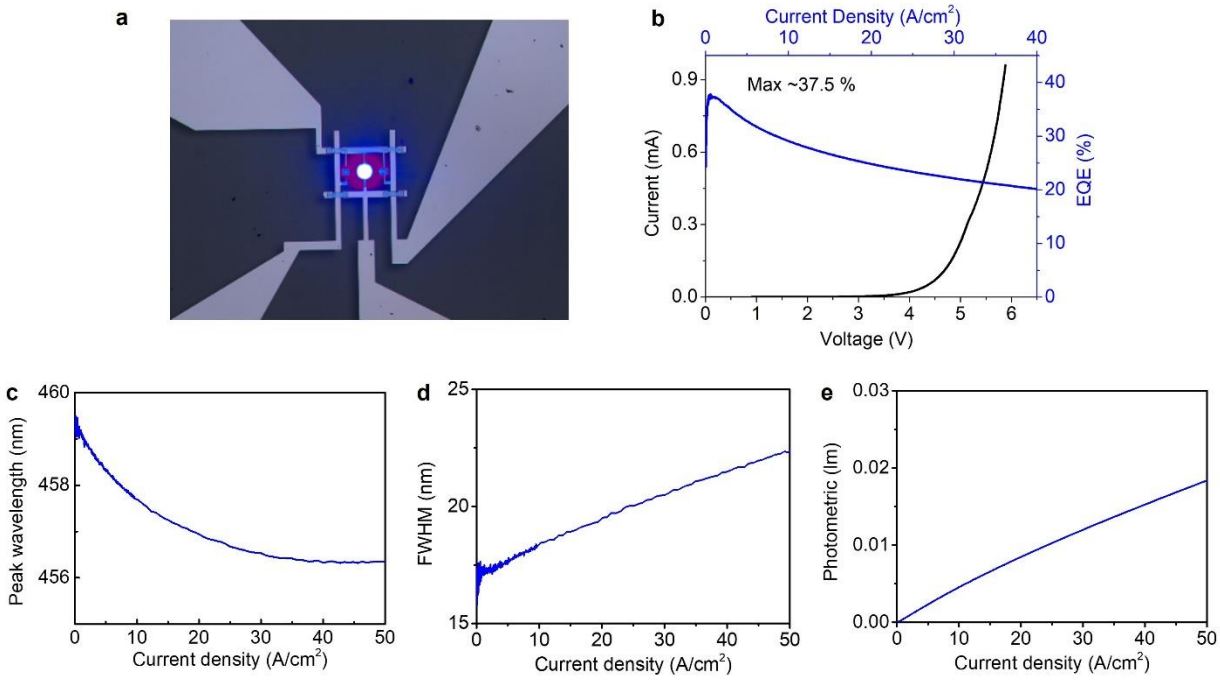


Figure S5. Optical properties of a single µLED chip a, An optical emission image of the individual µLED chip under an applied voltage. A TEG design with separate contact pads is prepared on the passive-matrix panel to characterize µLED chip after integration. **b,** Representative current-voltage and current density-EQE curves. **c,** the peak wavelength shift, **d,** full width at half maximum (FWHM) shift, and **e,** luminous flux as a function of applied current density up to 50 A/cm^2.

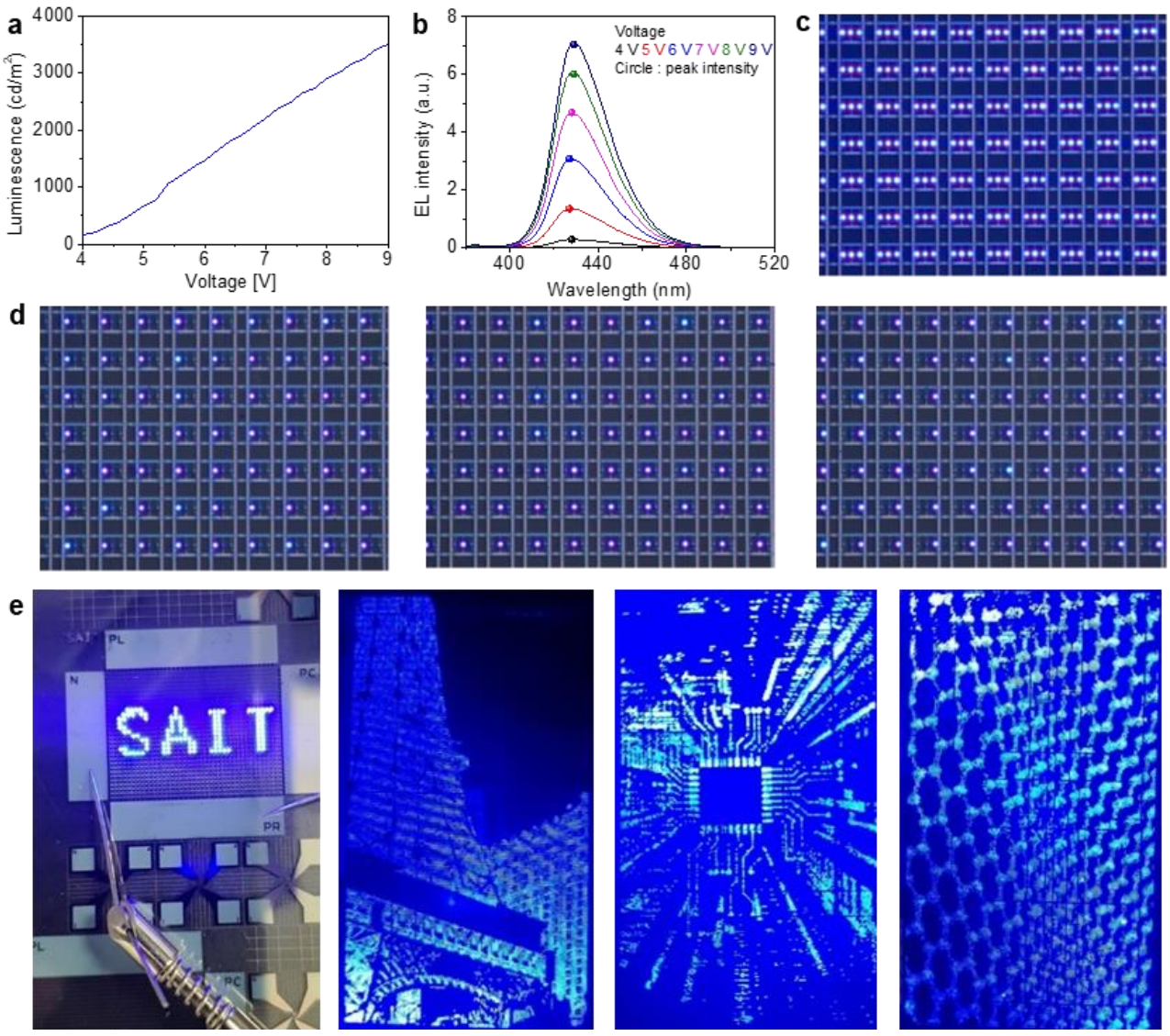


Figure S6. Properties and driving of the integrated panel a, Luminescence, and **b,** Emission spectrum as a function of the applied voltage. **c, d** Emission images of all pixel turned-on and separately addressed columns of the panel. **e**, Emission images of the integrated μLED display panels with computer-generated layouts; luminance difference was realized by controlling the number of emitted μLED chips in a pixel.

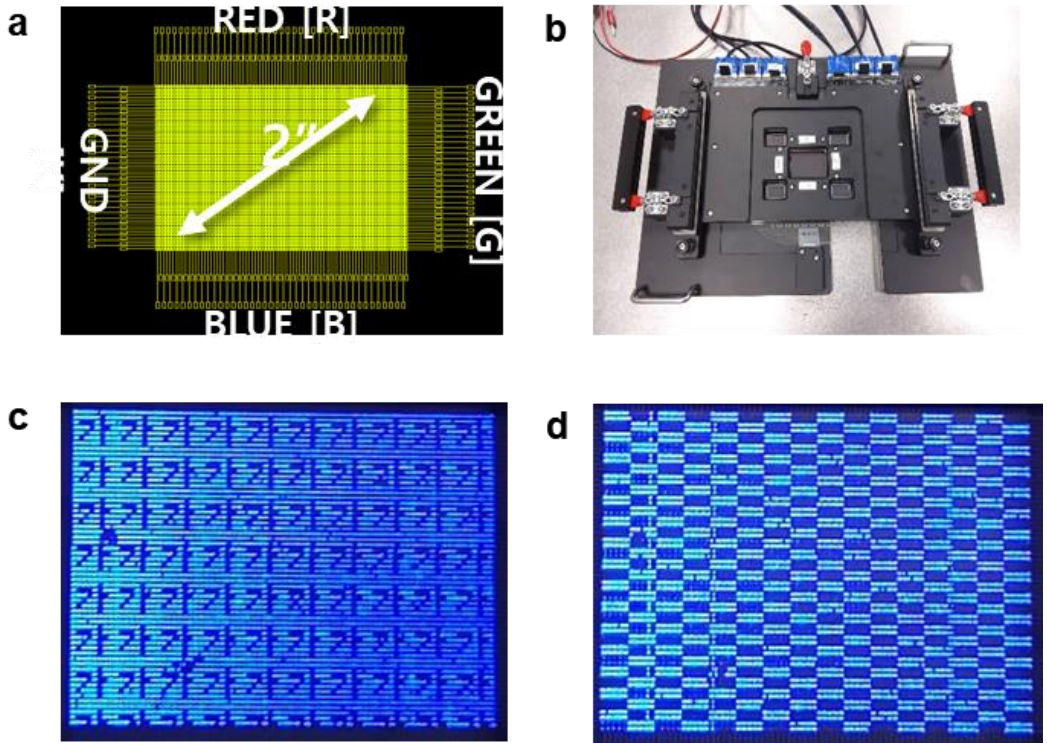


Figure S7. Passive matrix display a, Layout of the passive matrix panel (2″ Diagonal) with a pixel comprising three μLED chips, which is named red (R), green (G), and blue (B) for convenience. **b,** A customized panel driving module with pogo pin type contactors. **c, d,** Emission images of the passive matrix panel driven by the customized panel driving module

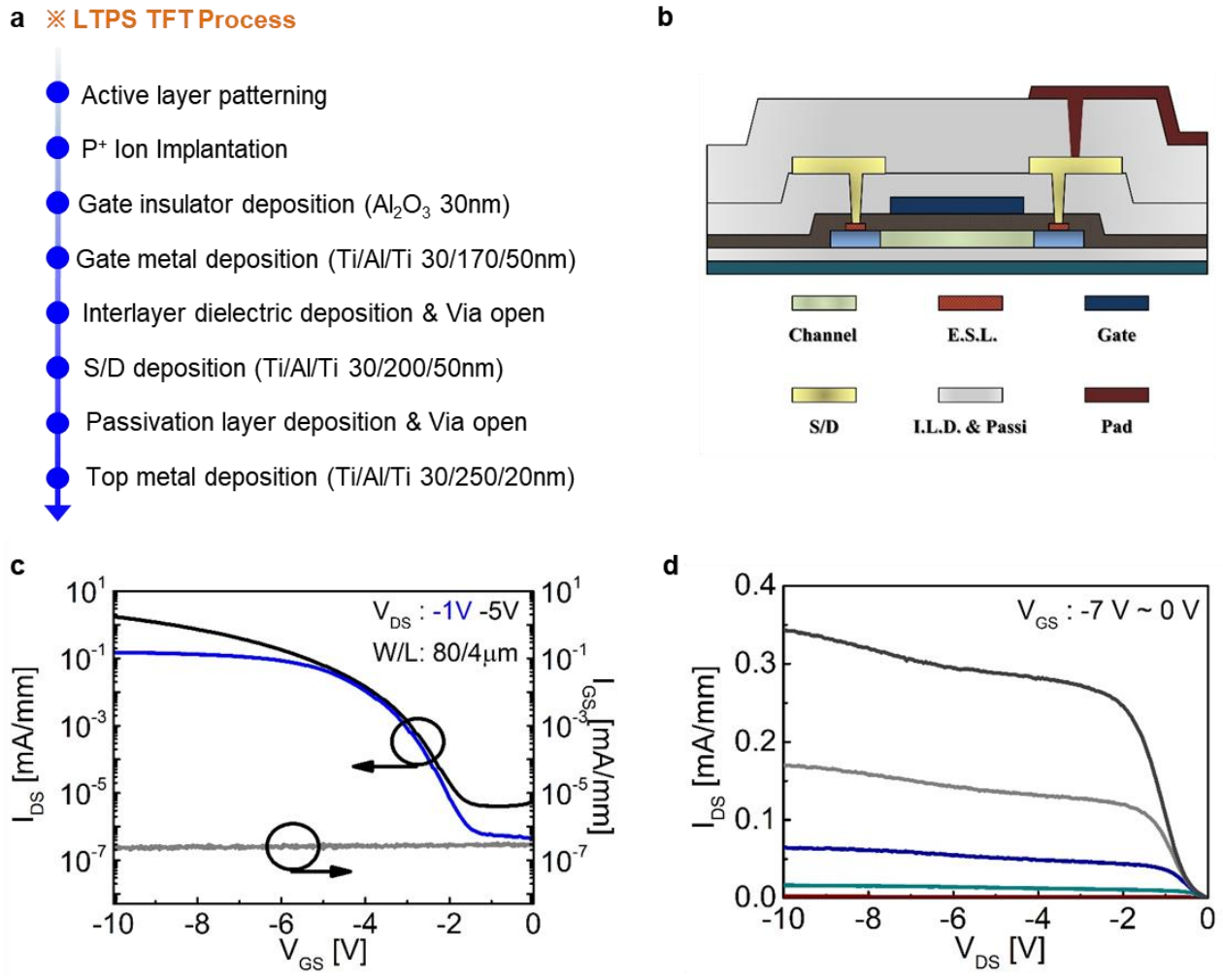


Figure S8. LTPS thin-film transistor process and properties a, Summary of LTPS TFT process with nine photomasks. **b**, Schematic illustration of the fabricated p-Si TFT. **c, d,** Representative transfer and output curves of the TFT.

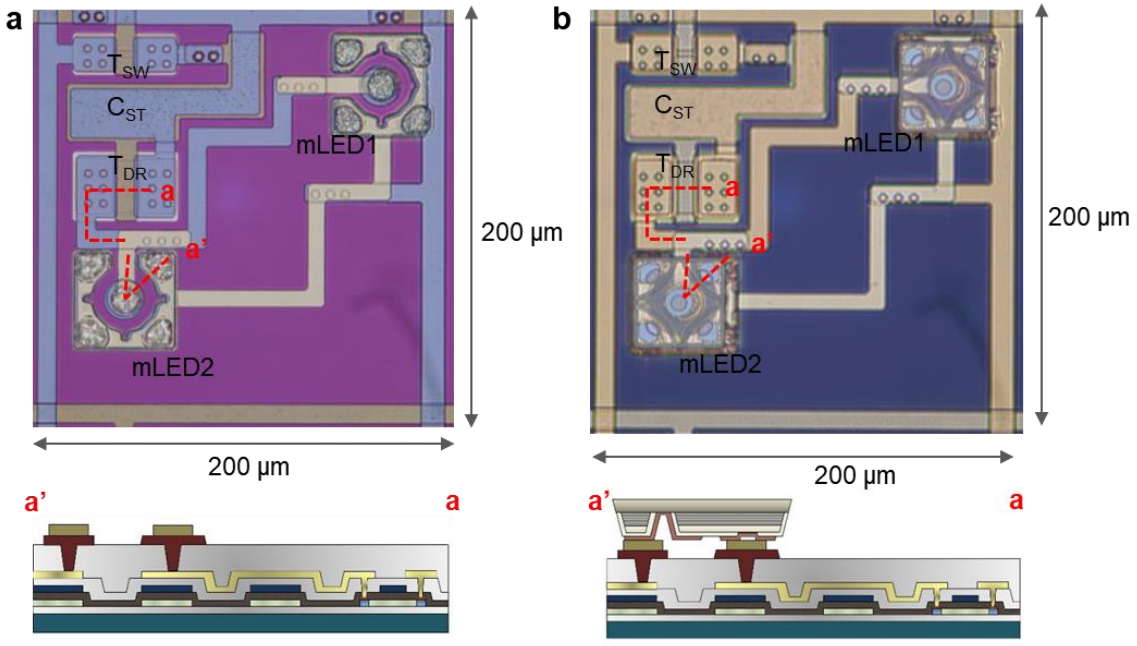


Figure S9. A single pixel image before and after μLED chip integration An optical image of a single pixel from the active-matrix panel **a,** before and **b,** after μLED chip bonding process. A conventional pixel design (2T-1C) was adopted, including a switching TFT (T_{SW}), driving TFT (T_{DR}), and storage capacitor (C_{ST}). Two μLED chips (mLED1, 2) were incorporated considering redundancy