

An integrated CMOS–silicon photonics transmitter with a 112 gigabaud transmission and picojoule per bit energy efficiency

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Supplementary Materials

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The manuscript is intended to further explain the background and motivation of this research work and provide further technical details of the design that we report in the main article.

1 Energy efficiency of photonics devices when embedded within the optical transmitter

For over a decade, the energy efficiency of the optical transmitter has been interpreted differently by people from different backgrounds. Focussing on the photonics device only, depending on the operating conditions, two categories of equations were normally used to estimate the energy efficiency of photonics devices.

For devices operating as a lumped capacitor, the energy per bit can be calculated with the following equations^{1,2}

$$E_{bit} = \frac{1}{4} CV_{pp}^2 \quad (1)$$

$$E_{bit, PAM-N} = \frac{CV_{pp}^2 \sum_{i=1}^N (N-i)(i/(N-1))^2}{N^2 \log_2(N)} \quad (2)$$

$$E_{bit, 16QAM} = \frac{5}{72} CV_{pp}^2 \quad (3)$$

where C is the capacitance of the device and V_{pp} is peak-to-peak drive voltage. Based on the equation (1), the energy per bit for complex modulation formats has also been derived, including equation(2)^{3,4} for PAM-N(N is PAM order) and equation(3)⁵ for 16-QAM. Typical examples of photonics device that are treated as lumped capacitors include Electro-Absorption Modulators (EAMs)³, silicon-based Ring Resonator Modulators (RRMs)⁴ and plasmonic modulators⁵, all of which reported device capacitance down to tens of fF or even less indicating that the energy efficiency those photonics devices could be down to the fJ/bit level.

For devices operating with the travelling wave configuration, the energy per bit can be calculated with equation(4)^{6,7}

$$E_{bit} = \frac{2 \times (V_{RMS}^2 / R)}{B} \quad (4)$$

where B is the bitrate, V_{RMS} is the root-mean-square voltage generated from the driver amplifier, R is the impedance value of the termination resistor. Many works^{6,8-10} use equation (4) to guide their phase shifter optimisation and often come with fJ/bit level energy efficiency with drive voltage swings down to hundreds of mV.

In summary, equation (1)-(4) suggest that reducing the device capacitance and increasing the load impedance of the photonics device as well as optimising the voltage swing requirement could directly benefit the energy efficiency of an optical transmitter. However, when the photonics device is embedded within a practical optical transmitter, the real energy efficiency is determined by many factors, which are far beyond the scope of equations (1)-(4). To further explain this, consider the following: As shown in Fig 1, the front-end circuit of an optical transmitter could be simplified as a driver, with internal output impedance R_0 , integrated with an effective load. For the cases with lumped elements, the effective load could be simplified as the device capacitance (C_l). The driving behaviour could therefore be simplified as an RC charge/discharge operation, in which the charge/discharge current (i) delivered by the driver follows the rule that is defined by the equation(5)

$$i = C \frac{dv}{dt} \quad (5)$$

Obviously, the amplitude of the current (i) is inversely proportional to the charging/discharging period(τ). When targeting the same level of voltage swing (V_{pp}), a higher voltage slew rate($\tau_1 < \tau_2$) requires more current($i_1 > i_2$) to charge/discharge the same capacitive load. Within the output stage of the driver amplifier, a higher current demands a larger transistor size and hence generates more parasitic capacitance, which in turn demands more current. Therefore, although the energy delivered to the same capacitive load could be the same, the energy

59 dissipating within the charge/discharge procedure could be dramatically different, which is out
60 of the scope of equations (1)-(3).

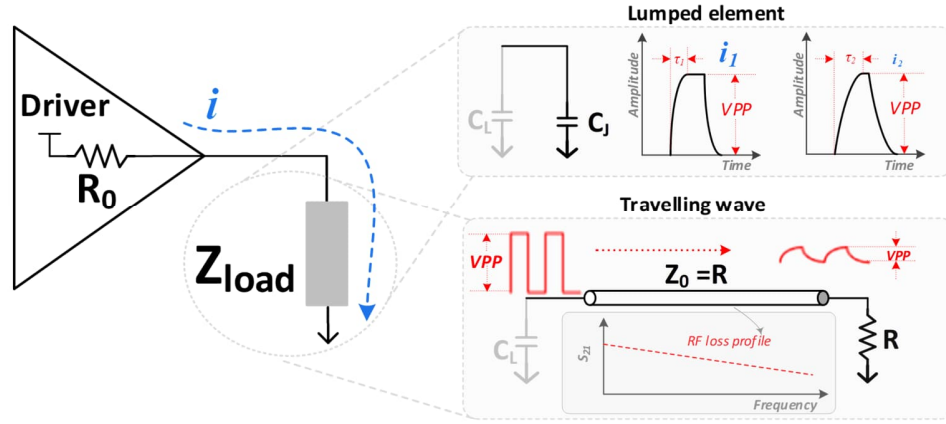


Figure 1 Simplified model of the front-end circuit of the optical transmitter

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63 A similar scenario arises with travelling wave configurations, in which the driver amplifier
64 sees the travelling wave phase shifter and far-end termination resistors as a low impedance load.
65 If the electrodes that form the travelling wave phase shifter are lossless, the energy efficiency
66 associated with the far-end termination R could be described by equation (4). However, the real
67 scenario is that a considerable amount of energy associated with these high-frequency
68 components is actually dissipated within the electrodes rather than contributing to optical phase
69 change over the entire phase shifter length. As a result, depending on the RF loss profile of the
70 phase shifter, the V_{pp} (and V_{RMS}) at the far-end could be significantly attenuated as compared to
71 the starting point of the phase shifter.

72 Furthermore, when the photonics device is integrated with the electrical device, a parasitic
73 capacitance (C_L) is associated with the integration, including the capacitance underneath the
74 I/O pad, the capacitance within the solder bump, the Cu pillar or bonding wire, which is another
75 dominant side-effect that must be considered. For instance, a typical I/O PAD within a standard
76 CMOS process could come with a capacitance of 80fF¹¹, which is already equivalent to a 40-
77 ohm impedance load when operating at 50GHz. Consequently, when operating at a high baud
78 rate (such as 100G Baud), the voltage swing (V_{pp}) generated from the driver amplifier could
79 be significantly attenuated before it really contributes to optical modulation. From the energy
80 dissipation perspective, the primary task of the driver circuit is to deliver enough electrical
81 energy to cope with all these low impedance loads and ensure that the majority of the electrical
82 energy really contributes to optical modulation over the desired frequency band.

83 Recent work⁸ has concluded that low capacitance or small $V\pi$ (half wave voltage)
84 modulators can be “driverless modulators”. If the driver is only considered as a voltage
85 amplifier, perhaps it is reasonable to classify those modulators as driverless designs as they
86 come with sub 1V half-wave voltage and do not need additional voltage amplification;
87 However, if we consider the energy delivery from an electrical circuit and the energy
88 dissipation within the optical modulator, the term “driverless” is a pseudo proposition as energy
89 transition from the electrical circuit to the optical device always exists.

90 Finally, perhaps it would be more meaningful to examine some practical design examples
91 to illustrate the limitation of the traditional concept in studying the energy efficiency of
92 photonics devices. In 2019, researchers from ETH Zurich reported excellent results on energy
93 efficiency figures for their plasmonic modulator⁵, which was calculated based on the equation
94 (1) and (3). The reported energy efficiency figures were 0.07 fJ/bit at 50 Gbps, 0.3 fJ/bit at 200
95 Gbps, and 2 fJ/bit at 400 Gbps. One year later, the same group of researchers monolithically
96 integrated their plasmonic modulator with electrical devices (SiGe) and reported an integrated
97 optical transmitter operating up to 120G Baud (OOK mode)¹². However, the MZM driver that
98 directly drives the modulator consumed 0.9W, indicating the energy efficiency (driver only) is
99 7.5pJ/bit, which is at least **3750** times worse than the cases when the plasmonic modulator was

evaluated as a standalone module. Obviously, without knowing the modulation depth (such as extinction ratio) or exact bit-error-rate, it is not rigorous to compare the above two results. However, more than three orders of degradation of the energy efficiency figure already indicates that equations (1)-(4) are not sufficient for estimating the real energy efficiency of a practical integrated optical transmitter.

2 Energy efficiency of an integrated photonics transmitter

If the energy efficiency of photonics devices in isolation is not adequate to estimate the real power consumption, it is, therefore, necessary to analyse the electrical amplifier and photonics devices as an integrated system. Over the years, numerous models¹³⁻¹⁶ were derived to estimate the energy efficiency of an integrated optical transmitter at different speeds together with analysis of the trade-off between electrical power and optical link budget. However, these kinds of model are only valid with certain types of circuit topology when operating within a limited speed range, whereas practical circuits could be dramatically different when the optical transmitter is running at different speeds with complex modulation formats.

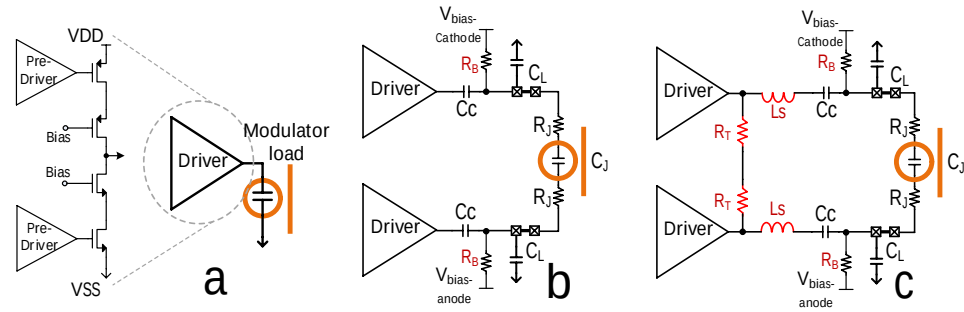


Figure 2 Illustration of the front-end circuit when the driver is integrated with Ring Resonator Modulators. (a) Circuit diagram when the driver sees the RRM as a capacitive load. (b) Circuit diagram when two drivers coupled to the cathode and anode of PN junction. (c) Circuit diagram when incorporating inductive peaking and shunt resistors¹¹.

For example, based on the Ring Resonator Modulator (RRM), the analytical model from reference¹⁵ has predicted a linear relationship between the driver's energy efficiency and the data rate of the integrated optical transmitter when operating under different drive voltages. This model is correct only if the load seen by the driver is dominated by the capacitive load, which is the scenario shown in many moderate-speed cases. For example, in 2011, previous work¹⁷ has presented outstanding energy efficiency results for 10G baud (OOK) transmission with 7dB ER giving energy efficiency optimised at 0.135pJ/bit. Similar work can be found in¹⁸ and¹⁹, both of which demonstrated excellent energy efficiency figures when operating at 20G-25G baud. Nonetheless, the front-end circuit topologies within these references can be simplified to the circuits that are illustrated in Figure 2(a) and (b), in which the drivers see the RRM as a capacitive load. Although some additional elements from device packaging (C_L) and DC biasing (C_C and R_B) also influence the transmission performance, the overall circuit can be regarded as an RC charging/discharging function.

However, when the RRM-based optical transmitter operates at 56G baud¹¹ (112Gbps PAM-4), as shown in Figure 2(c), a peaking inductor (L_S) has been adopted to enhance the bandwidth. To ensure a flat frequency response (i.e. an RLC resonant circuit is operating in the over-damped condition), an additional shunt resistor (R_T) has to be incorporated. The side effect is that the shunt resistor (R_T) behaves as an additional low-impedance resistive load to the driver and consumes a considerable amount of power. This kind of circuit obviously sits beyond the scope of the model that has been reported in previous work¹⁵. The fact is that within the work¹¹, the output stage of the driver amplifier on its own has consumed 160mW, which gives 1.43pJ/bit energy efficiency figure when operated at 56G baud (112Gbps PAM-4). Bear in mind that our manuscript has demonstrated 112G baud (112Gbps OOK and 224Gbps PAM-4) with sub pJ/bit energy efficiency, we may conclude that when operating at an extremely high baud rate (>100G Baud), in certain circumstances the practical energy efficiency of an RRM

based optical transmitter may be even worse than the typical MZM solution, since the RRM needs additional power to stabilise its wavelength.

It is not trivial for any integrated optical transceiver to operate at 100G baud+, regardless of the device material, including silicon, III-V, thin-film LiNbO₃, plasmonic or polymer. Among all the challenges faced by the designer, perhaps the least difficult is the EO bandwidth (Baud rate) of the photonics device, whereas the dominant challenges are the resources that are demanded to achieve such a high baud rate, including the fabrication costs for high-volume production and the electrical energy consumed to perform data transmission. For over a decade, driven by the relentless growth in data demand, huge efforts²⁰ have been devoted to enhancing the overall throughput of optical transceivers, and the issue of electrical power consumption has become unavoidable.

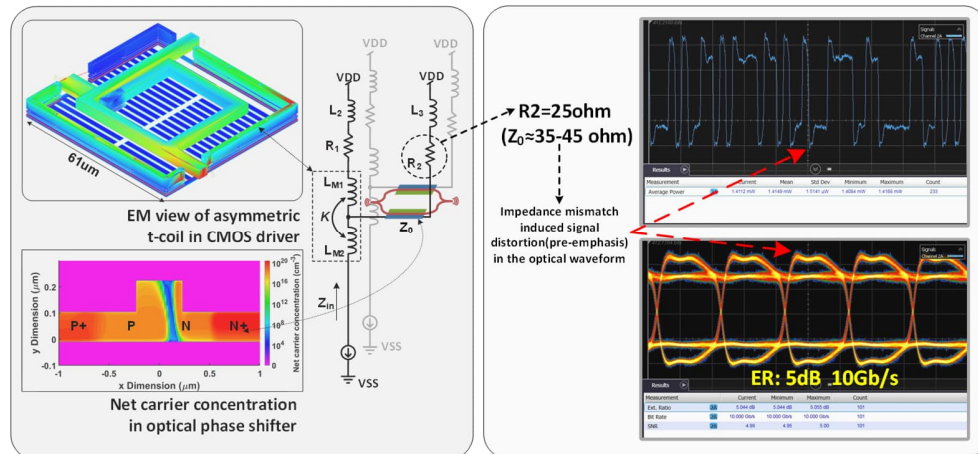


Figure 3 Illustration of the impedance mismatch induced waveform distortion (pre-emphasis) within our previous work²¹

Facing the above challenge, we have revisited our previous optical transmitter work²¹, which was designed for high-speed operation. To enhance the overall bandwidth of that integrated silicon transmitter, we adopted several techniques, including T-coil peaking²², the far-end impedance mismatch approach²³ and the use of a customised doping profile for the PN junction²⁴. The outcome was that our previous work demonstrated it was possible to operate up to 100G baud OOK in an all-silicon modulator-driver integrated transmitter without using any DSP techniques.

The interesting thing is when examining that device at a lower speed, as shown in Figure 3, the far-end impedance mismatch approach introduced obvious waveform distortion (pre-emphasis). Although the impedance-mismatch-induced waveform reflection does benefit overall bandwidth, it obviously degrades the achievable Signal-to-Noise Ratio (SNR). From the energy efficiency perspective, a certain amount of energy was wasted within the waveform reflection. This issue becomes more serious when operating with complex modulation formats (such as PAM-4) or when the driver operates at its lowest power consumption, both of which impose even tighter requirements for signal integrity and SNR.

Abandoning the impedance mismatch approach could easily solve the above issues but would come with the penalty of a lower EO bandwidth. To compensate this bandwidth drop, once again, the dimensions of all the inductive peaking functions, the impedance of the near-end terminations, and the doping profiles associated with the phase shifter have to be re-designed. It often requires several iterations of design optimisation to achieve the most balanced solution (maximum bandwidth, lowest optical loss, and lower power consumption). However, these passive electrical devices (near-end and far-end terminations, inductive peaking function) are closely linked with the phase shifter and are compatible with standard back-end processes. Therefore, rather than optimising each individual parameter, it would be reasonable to consider the phase shifter, inductive network, far-end termination (R_2) and near-end termination (R_1) as an “integrated optoelectronic device”. That is, the input to this integrated device is a pair of

“switching currents (I_{in+}/I_{in-})”, whereas the output is the “modulated light”. Then the system can be optimised for optimal power utilisation within the optical modulation process.

3 Voltage mode and current mode driver amplifier

Driver amplifier circuit design is complex, and every detail is beyond the scope of this paper. Therefore, we show here the typical circuit topology of the voltage mode and current mode driver amplifier designs and then distinguish the design philosophy that we have proposed in this manuscript.

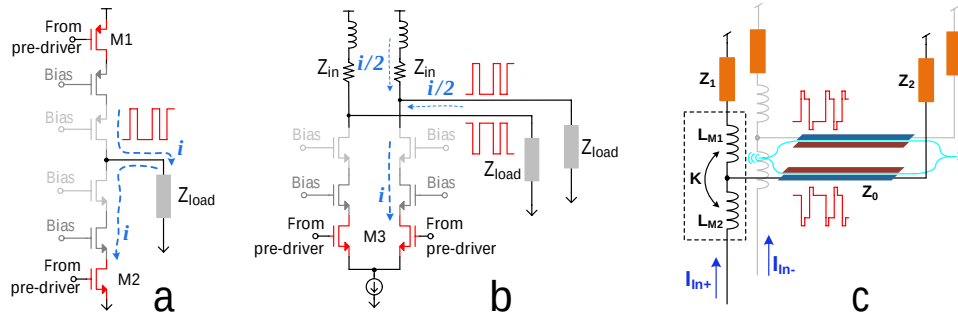


Figure 4 Simplified circuit topology of (a) a voltage mode driver (b) a current mode driver and the (c) the “integrated optoelectronic device” proposed in this work.

The voltage mode driver^{25,26}, as shown in Figure 4(a), is implemented by switching the transistors M1 and M2 simultaneously so that the charge/discharge current (i) is delivered to the load, hence generating a voltage swing ($i \times Z_{load}$). The challenge with the voltage mode approach is the relatively low speed (due to the low-speed PMOS(M1)) and the output impedance control. In contrast, high speed and output impedance control are more easily achieved within the current mode approach²⁷⁻²⁹. As shown in Figure 4(b), the current mode driver is realised by switching a pair of NMOS transistors(M3) so that the switching current is delivered to the near-end load (Z_{in}) and the far-end load (Z_{load}). If the impedance of Z_{in} is equal to Z_{load} , the effective voltage swing is $(i/2) \times Z_{load}$, which is half of the voltage swing within that voltage mode approach. The choice of voltage mode or current mode driver within a practical optical transmitter depends on many factors, including the operating speed, packaging approach and the type of photonics devices. Previous work³⁰ further compared the power efficiency figure when a different type of driver was integrated with different photonics devices. Overall, regardless of the details of the driver circuit, all drivers could be treated as broadband power amplifiers that deliver a certain amount of energy to photonics devices over the desired frequency band. Typically, when the load is the optical modulator, the efficiency is evaluated as the peak-to-peak voltage swing (V_{pp}), as the modulation efficiency figure is denoted as the $V\pi \cdot L$ (V_{cm}).

This work is not focusing on the optimisation of the driver circuit. Instead, we are trying to maximise the energy that is delivered from the electrical amplifier and utilised within an integrated optical transmitter for modulation. As shown in Figure 4(c), we treat the phase shifter, inductive network, far-end termination (R_2) and near-end termination (R_1) as an “integrated optoelectronic device”. Therefore, the desired electrical energy is embodied as the “switching current” rather than “voltage swing” in the traditional sense.

4 Characterization of the separated “standalone” driver amplifier.

Although we have mentioned several times in the main article that the electrical input was designed as a “switching current” supply and the near-end termination together with the inductive network is designed in the context with the phase shifter and far-end termination, the performance of the separated “standalone” driver amplifier is of interest to the reader. Therefore, the CMOS chip was characterised with a 4-port network analyser Keysight-N5227B, with the testing configuration and testing results shown in Figure 5.

Over the entire frequency band, up to 5 dB ripple is observed due to the fact of adopting additional inductive peaking, which may indicate this is a “badly” designed voltage amplifier if we evaluate it in isolation and in the traditional way. Closely analysing the results shown in Figure 5, the first peaking happens in the 25-30GHz frequency range, which is consistent with the peaking observed in the EO integrated 2.47mm long device (main-article Figure 3(d)); whereas the second peaking happens around 60-65GHz, which is consistent within the peaking observed in the EO integrated 1.27mm long device (main-article Figure 3(b)). Once again, we emphasise that our approach was not to design and build a standalone driver as a voltage amplifier and drive a standard 50 ohm load.

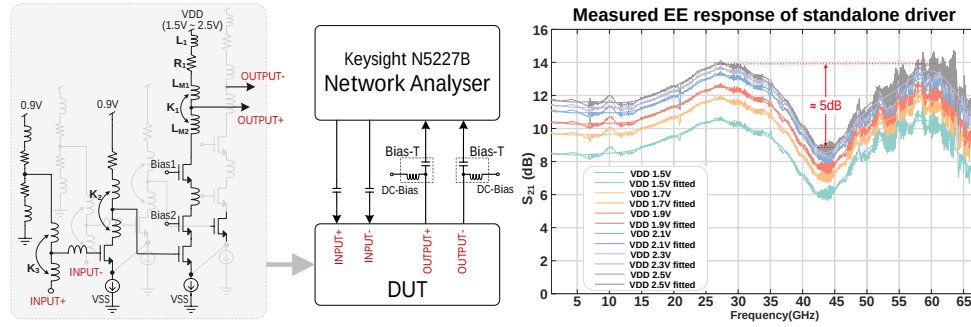


Figure 5 Characterisation of the “standalone” driver amplifier.

5 Shield CPW travelling-wave electrodes

The travelling wave electrode is a typical solution for optical modulators, which can help to reduce the driving voltage while maintaining the EO bandwidth³¹. When implementing CPW travelling-wave electrodes with PN-junction based modulators, one of the common issues is the asymmetric distribution of the capacitance associated with the CPW electrodes. As shown in Figure 6 (a) and (b), the PN junction only exists between the left ground track and the middle signal track. Therefore, the unwanted slot-line mode (odd mode) could be easily triggered within CPW electrodes, degrading the achievable bandwidth of the modulator. Previous work^{31 32} has built an analytical model for this phenomenon and suggests solutions to mitigate the unwanted slot-line mode, including the use of a bonding wire formed shield³² and a top-metal track formed shield³¹(Figure 6(c)).

Closely examining these previous works, we realised that the model presented in work³¹ was only based on the discrete components, in which the PN junction was simplified as a resistor(R) in series with a capacitor(C) and the shielded electrodes were simplified as an inductor(L). It does illustrate the unwanted slot-line mode and an approach to suppress it, but it may not be able to analyse the whole electromagnetic (EM) effect associated with the travelling wave modulator. Therefore, as shown in Figure 6 (d)-(e), we have purposely modelled the whole optical modulator(with/without shield) within the EM analysis platform Keysight-ADS-FEM, in which the resistivity of each section (P++, P, N, N++) within the PN junction was extracted based on the doping profile reported in our previous work²¹. An intrinsic silicon region is purposely built within the P and N regions to form the junction capacitance. Depending on the reverse-bias voltage that is applied to the PN junction, the width of this intrinsic silicon region could be varied to match the capacitance per unit length of the phase shifter. The electrode and via material are defined as standard Aluminum with typical dimensions reported in the silicon photonics platform CORNERSTONE³³. The whole EM simulation runs on a dedicated server, which could use more than 1TB of memory and requires more than two days of processing time.

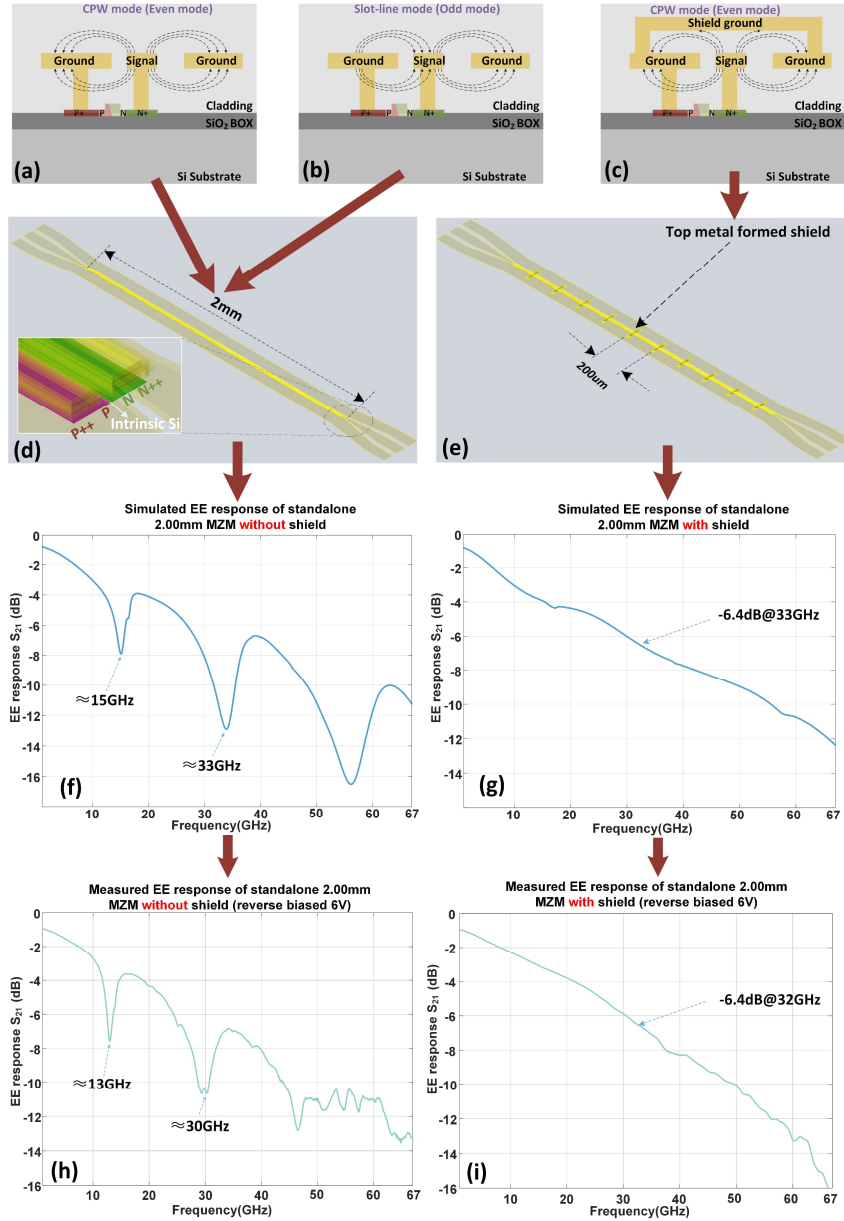


Figure 6 Mitigation of the slot-line mode within the travelling wave modulator (a) CPW mode with traditional PN junction based travelling wave modulator. (b) Slot-line mode with traditional PN junction based travelling wave modulator. (c) CPW mode with top-metal shield. (d/e) 3-D view of the analytical model in ADS. (f) Simulated EE response of a standalone 2.00mm long MZM without shield. (g) Simulated EE response of a standalone 2.00mm long MZM with shield. (h) Measured EE response of a standalone 2.00mm long MZM without shield (reverse biased at 6V). (i) Measured EE response of a standalone 2.00mm long MZM with shield (reverse biased at 6V)

The simulated electrical RF S_{21} (EE response) results are shown in Figures 6 (f) and (g). As expected, without the shield, three noticeable band-stop effects happen within the frequency range 10-20GHz, 30-40GHz and 50-60GHz, which is due to the occurrence of the slot-line mode. In contrast, with the shielded structure, an almost constant roll-off factor indicates that the slot-line mode has been eliminated within the whole analysed band.

To further justify the simulation results, we have conducted electrical S-parameter testing on the standard 2mm long silicon MZM by using a Keysight-N5227B network analyser. As shown in Figure6(h)the measured EE S_{21} results of the device without shield show three band-

stop regions, which are similar to the band-stop regions that were obtained within the simulation results. In contrast, all the band-stop regions disappear when the bonding wire is applied as a top shield as shown in Figure 6(i). Differences observed between the simulation and measurement results, especially with the band-stop regions is believed to be due to process variations within the photonics device fabrication, especially at the doping and annealing stage. Furthermore, it is necessary to point out that within the shielded case, both simulated and measured results illustrated a -6.4dB bandwidth at about 32GHz. According to the analytical model reported in ³⁴, the -6.4dB bandwidth of an EE response could be translated to the 3dB bandwidth of an EO response for optical modulation. As expected, the testing results in the main article (Figure 3 (c)) also demonstrated this.

In summary, as we have pointed out above, adopting the top-metal shield approach to eliminate the slot-line mode within the travelling wave modulator has been reported in many previous work³⁵. Perhaps the most valuable contribution of this part is the EM modelling approach that we have adopted, which could be further utilized to optimize the electrode design for the optical modulator, especially when the modulator is designed together with an inductive network and on-chip terminations.

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