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Supplementary information

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Scaled vertical-nanowire heterojunction tunnelling transistors with extreme quantum confinement

In the format provided by the authors and unedited

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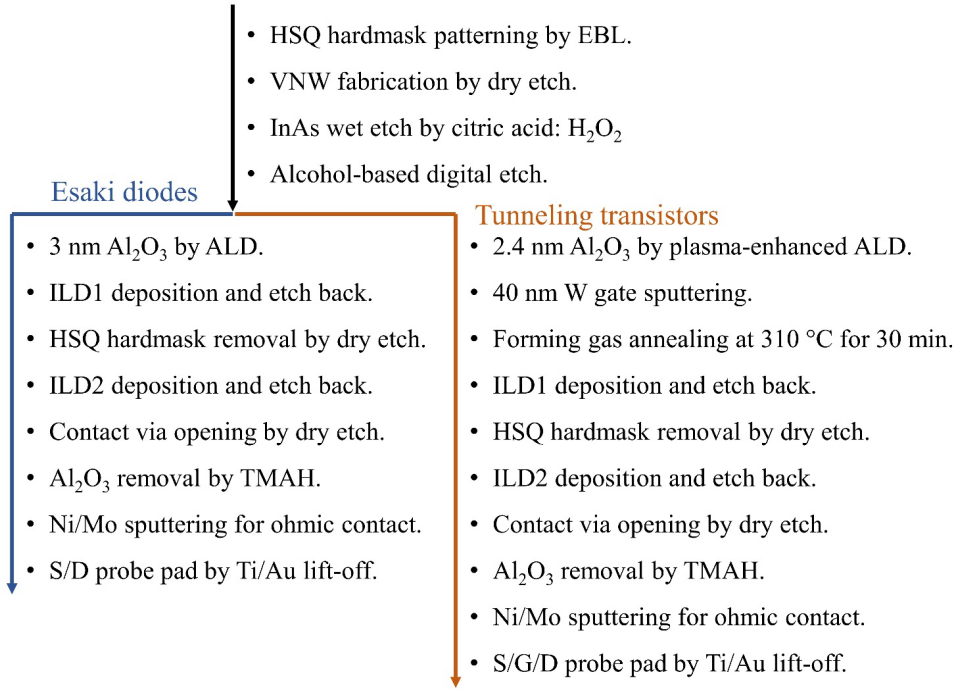
Supplementary Text: discussion of the complementary HJ tunneling transistor technology

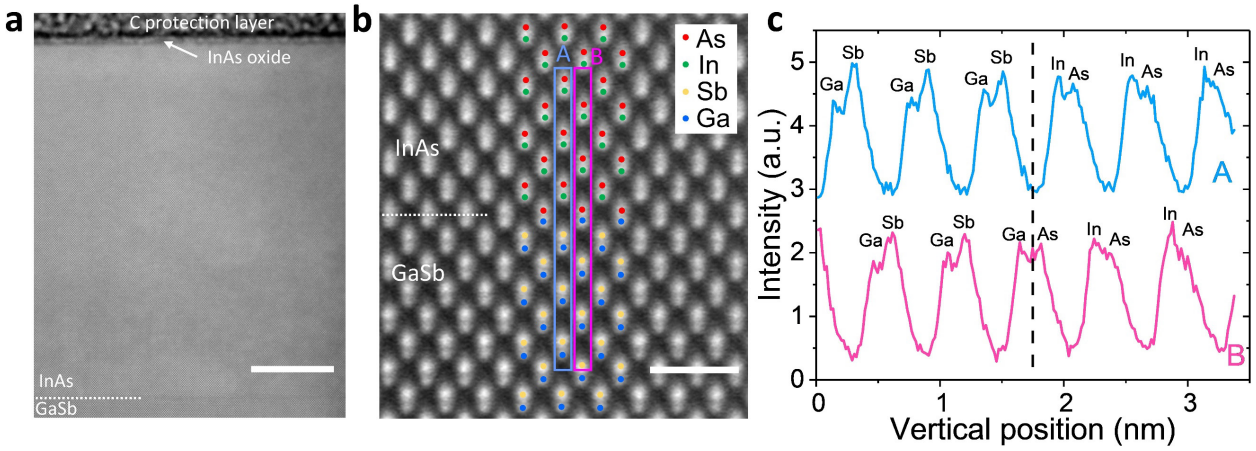
The success of microelectronics in the past 60 years is largely credited to CMOS technology, in which both p- and n-type MOSFETs with balanced performance are used in logic circuits to deliver extremely low static power. Therefore, for future logic applications, complementary HJ tunneling transistor technology must be demonstrated.

Compared to n-type HJ tunneling transistors, realizing high-performance p-type devices is even more challenging, due to fundamental material properties and device processing issues. In a GaSb/InAs(Sb) p-type HJ tunneling transistor, n-InAs, i-GaSb, and p-GaSb are designed as source, channel, and drain, respectively[S1]. The small density of states (DOS) in the InAs conduction band creates a trade-off between high tunneling probability and steep switching slope[16]. Fortunately, by careful design of the source doping concentration, a decent on-state performance and a subthermionic subthreshold swing have been predicted[16]. Besides, the GaSb/oxide interface is notorious for high interface trap density that could deteriorate the switching slope [S1]. Although there is no solid solution yet to the GaSb interface trap problem, there are several possible directions to explore, such as by using an in-situ hydrogen plasma surface clean[S2], and/or by using an in-situ atomic-layer etching plus atomic-layer deposition technology[44].

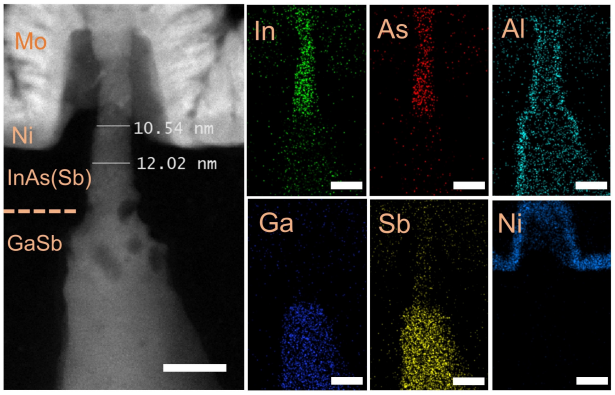
Therefore, despite foreseen and even unforeseen challenges, realization of balanced-performance HJ tunneling transistor technology appears indeed viable. It offers a very promising path for continuous CMOS scaling.



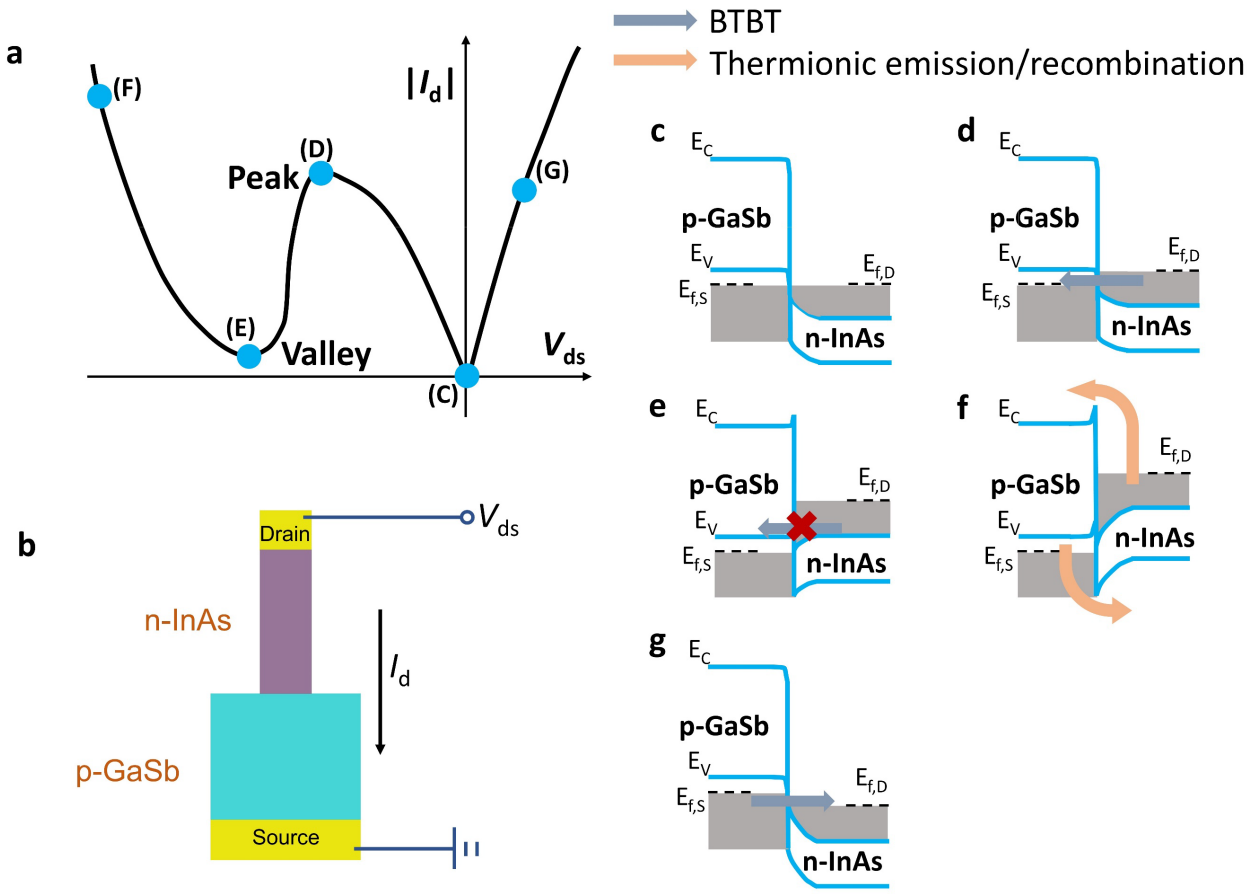
Supplementary Scheme 1| Fabrication process flow. VNW Esaki diodes and tunneling transistors share the same fabrication flow (indicated by the black arrow) up to the digital etch step. From then on, the process flow differs as indicated by the blue arrow for Esaki diodes and the red arrow for transistors.



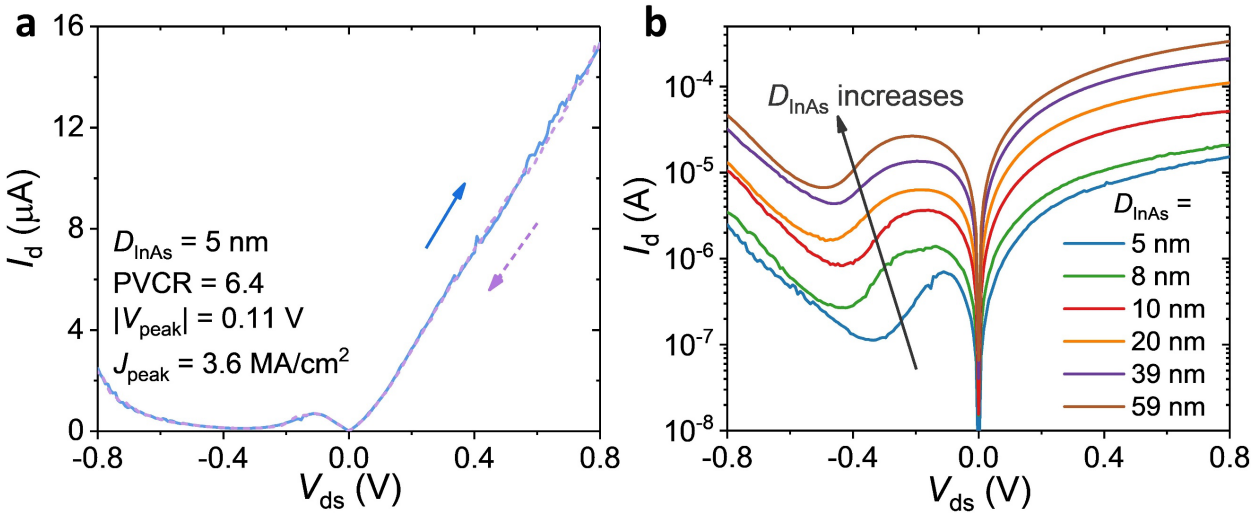
Supplementary Fig. 1| Characterization of atomically-sharp tunneling junction. a, STEM image of Esaki diode heterostructure shown in Fig. 1a with no visible defects. The tunneling junction is labeled. Scale bar: 20 nm. **b**, High-resolution STEM image of tunneling junction. Individual In, Ga, As, and Sb atoms are labeled as well as the location of the GaSb/InAs interface. Scale bar: 1 nm. **c**, Extracted line scan along lines A and B from **b**, respectively, as indicated by the boxes. The atoms are assigned based on the fact that the brightness is proportional to the square of the atomic number[S3]. A GaAs-like heterointerface is demonstrated.



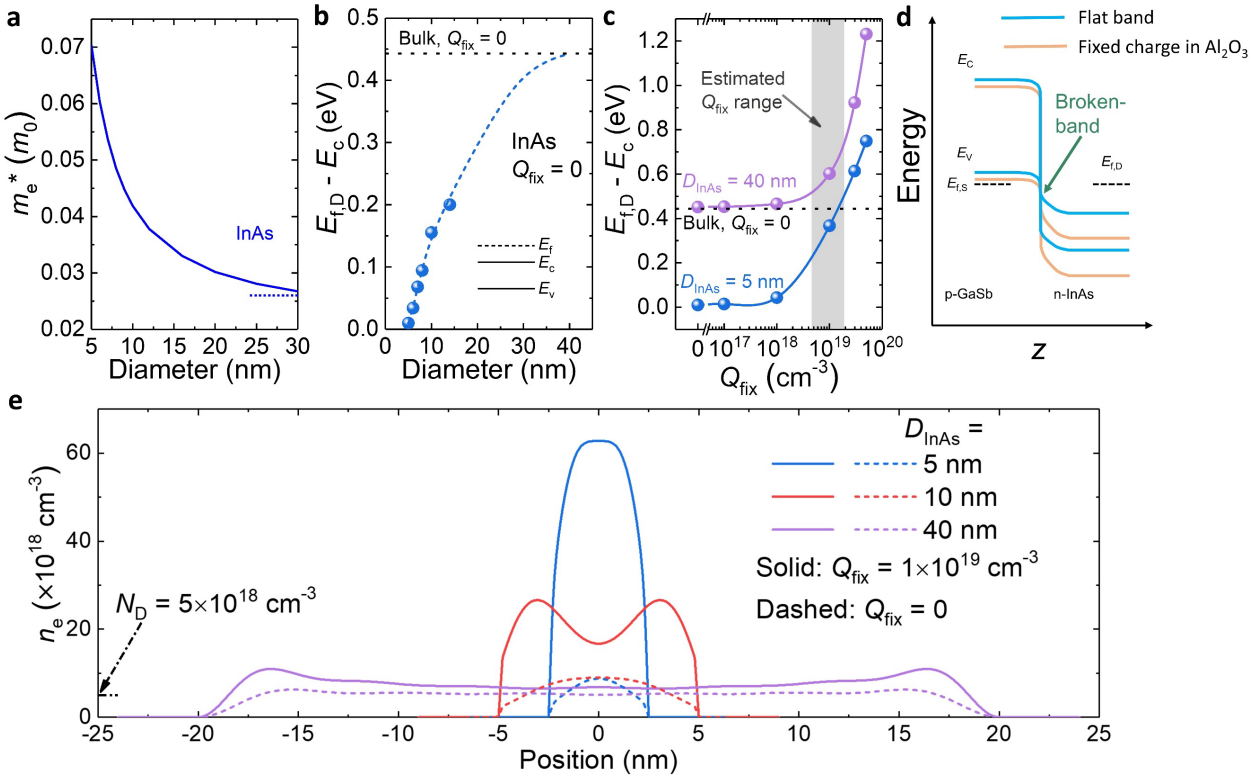
Supplementary Fig. 2| VNW device TEM characterization. HAADF-STEM image of a finished VNW Esaki diode with D_{InAs} = 12 nm at the tunneling junction. EDS element mappings of In, As, Al, Ga, Sb, and Ni are also shown. The presence of Al on the whole VNW cross-section indicates the VNW was not cut through during FIB, but was protected by a thin layer of Al_2O_3. Scale bars: 20 nm.



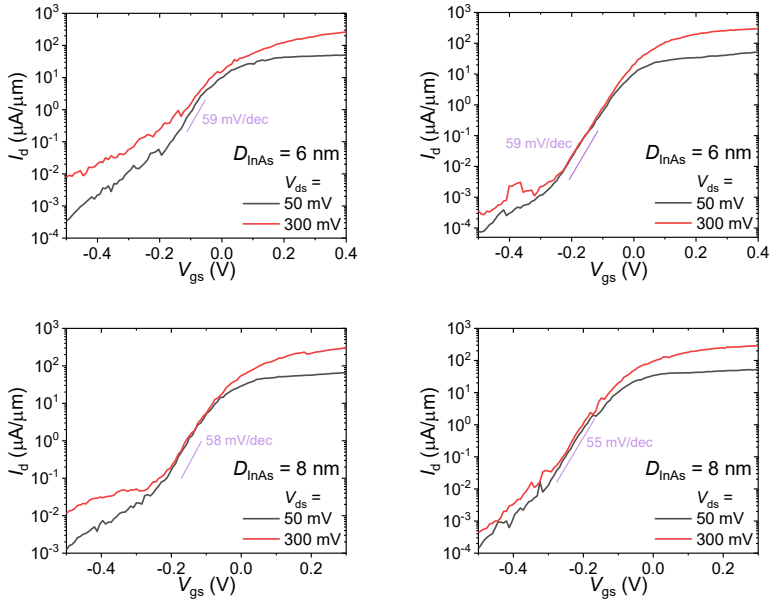
Supplementary Fig. 3| Working principle of broken-band GaSb/InAs Esaki diode. a, Schematic *I-V* curve of a GaSb/InAs Esaki diode with peak and valley labeled. **b**, Schematic Esaki diode structure, as well as the definition of voltage and current. **c-g**, Schematic energy band diagrams at different bias, including thermal equilibrium (**c**), peak position (**d**), valley position (**e**), thermal current (**f**), and positive V_{ds} regimes with dominant BTBT (**g**). When a negative V_{ds} is applied, as the absolute bias value increases, peak current (I_{peak}) due to BTBT of electrons from InAs to GaSb is reached (**d**), followed by an NDR region with a valley current (I_{valley}) (**e**). Finally, the current increases again due to thermionic emission (**f**). When a positive V_{ds} is applied, the BTBT current of electrons from GaSb to InAs keeps increasing as the bias increases (**g**). This is the working regime for tunneling transistors.



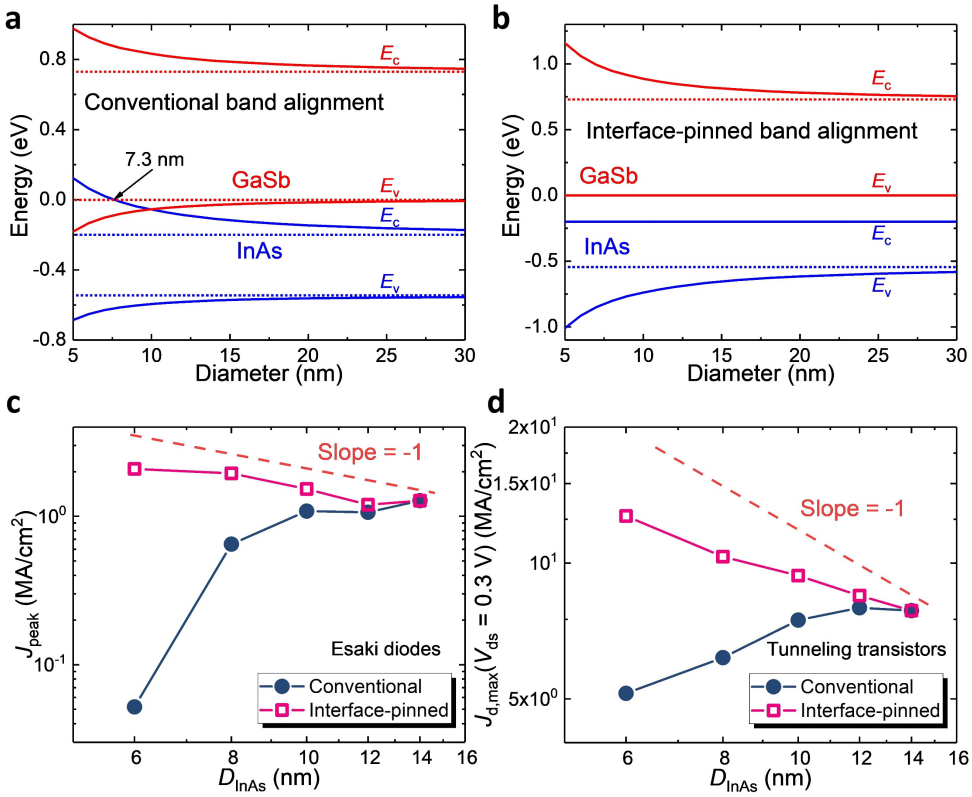
Supplementary Fig. 4| *I-V* characteristics of Esaki diodes. a, Linear-scale *I-V* curve of the device reported in Fig. 2a, showing a sharp linear turn-on in the positive V_{ds} branch. **b**, *I-V* curves for Esaki diodes with different diameters. Similar shapes of the curves with high PVCR were observed in all devices. $|V_{peak}|$ increases as D_{InAs} increases from 6 to 40 nm, and then stays nearly constant, as shown in Fig. 2c.



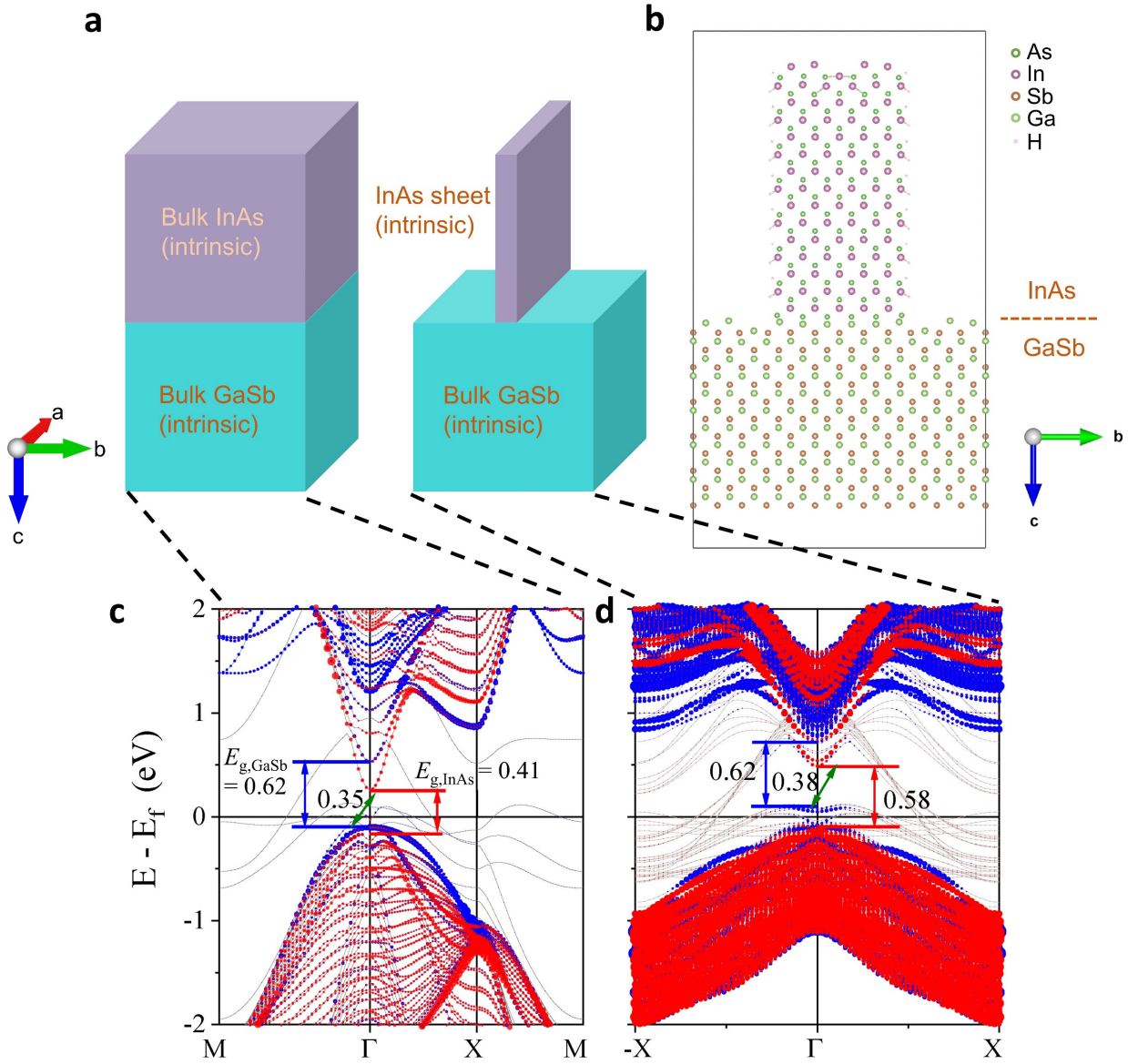
Supplementary Fig. 5| Two-dimensional simulations of nanowire cross-sections and resulting band diagrams. a, Electron effective mass (m_e^*) for InAs *versus* D_{InAs}. The dotted line indicates the value for the bulk material. m_0 denotes the mass of a free electron. The simulations were carried out using 8-band **k·p** approach with a circular semiconductor cross-sectional area surrounded by 3-nm Al_2O_3. **b**,**c**, Self-consistent Poisson-Schrödinger simulations using 8-band **k·p** approach with a circular n-InAs ($N_D = 5\times10^{18}$ cm^{-3}) cross-sectional area (except for simulations with D_{InAs} = 40 nm, in which the effective-mass method was carried out with the bulk InAs electron effective mass value) surrounded by a 3-nm Al_2O_3. In **b**, the position of the lowest conduction sub-band with respect to the Fermi level (i.e., $E_f - E_c$) was simulated as a function of diameter (solid symbols) without fixed charge in Al_2O_3. Due to the exponentially increasing computational burden together with convergence issues in the self-consistent 8-band **k·p** simulations, we carried out simulations till a largest diameter of 14 nm. The trend line is plotted till 40 nm. The position of the conduction band edge for bulk InAs is also indicated. In **c**, $E_f - E_c$ was simulated as a function of fixed charge density (Q_{fix}) in Al_2O_3 for D_{InAs} = 5 and 40 nm, respectively, indicating an accumulation of electrons as E_c is farther away from E_f with increasing Q_{fix}. Given that the presence of Q_{fix} has a minor influence on D_{InAs} = 40 nm devices but a significant influence on D_{InAs} = 5 nm devices, a possible Q_{fix} range is estimated. **d**, Schematic band diagrams for Esaki diodes with a broken-band alignment at the junction, where the influence of Q_{fix} is also shown. **e**, One-dimensional slice of electron concentration (n_e) across VNW with different D_{InAs} with and without Q_{fix} in Al_2O_3 is shown. All the simulations were performed at 300 K.



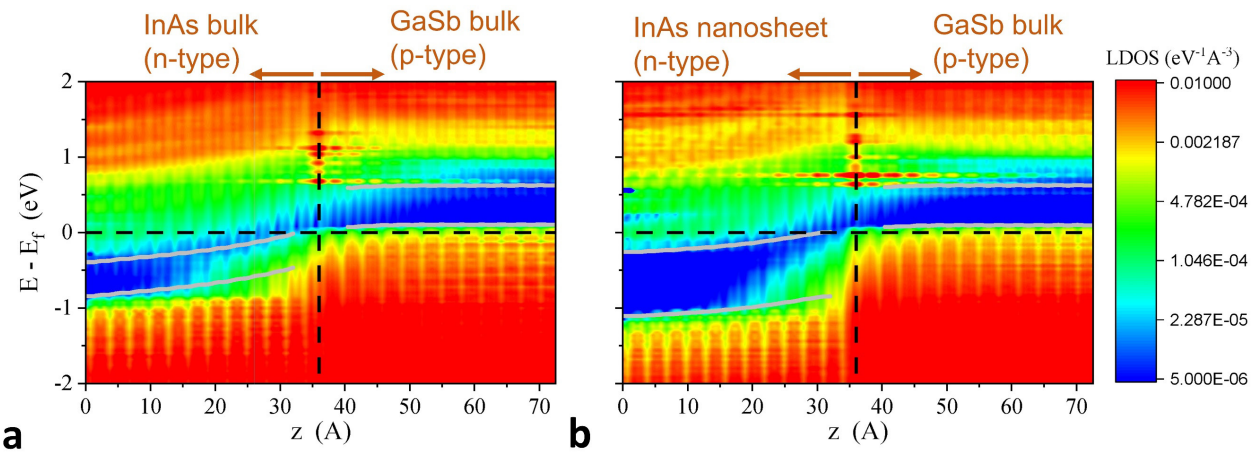
Supplementary Fig. 6| Subthreshold characteristics of four ultra-scaled devices with sub-thermionic operation. Tunneling transistors with diameter of 6 or 8 nm were measured at V_{ds} = 50 and 300 mV. A subthreshold swing in the range of 55-59 mV/dec was observed in these devices.



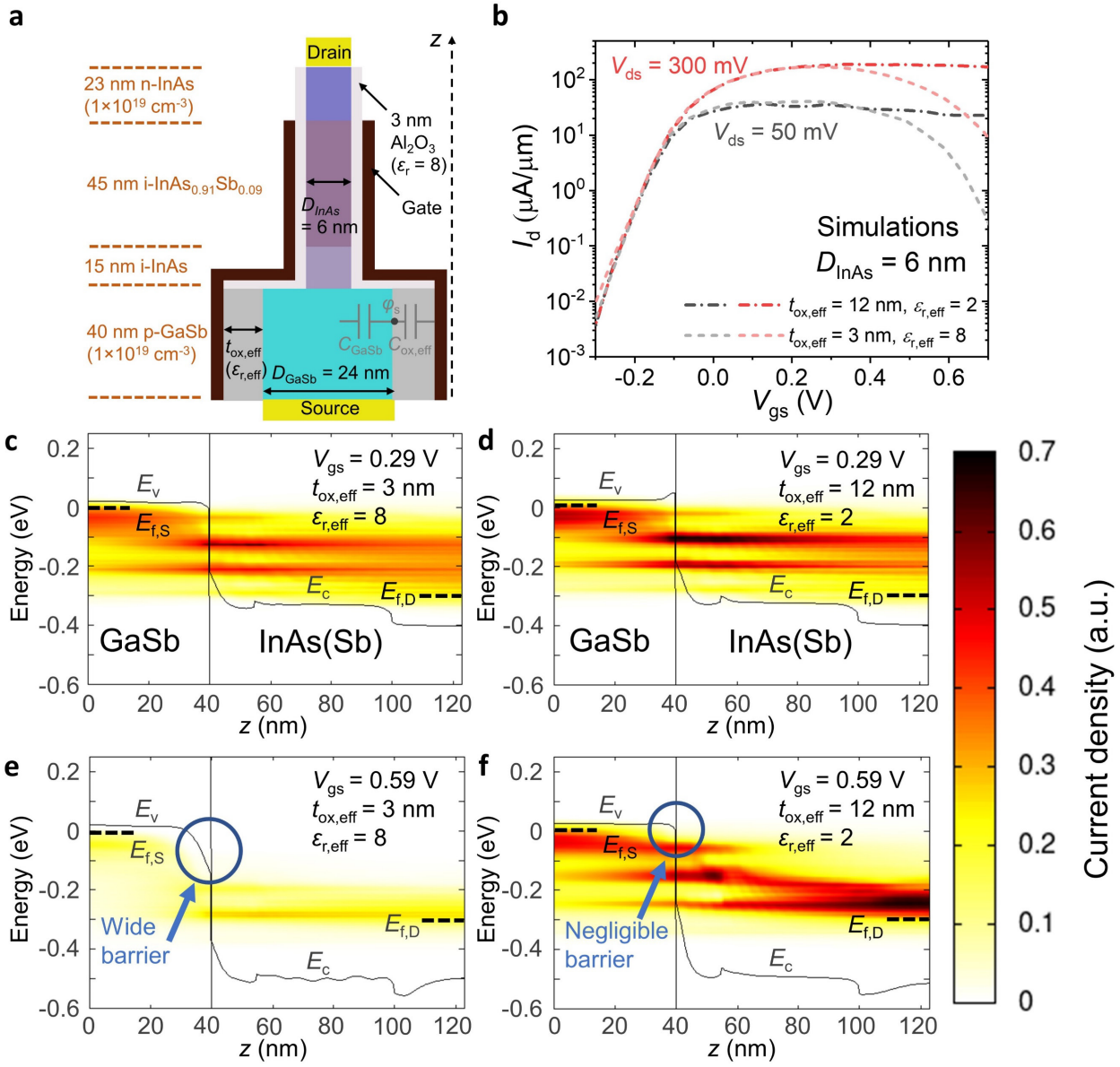
Supplementary Fig. 7| Two band alignment scenarios and corresponding transport simulations. a, Conventional understanding of effective band alignment as a function of diameter. E_c and E_v denote the lowest conduction sub-band and the highest valence sub-band, respectively. The dotted lines indicate the conduction and the valence band edges for the bulk materials. For a nanowire with a bulk-like GaSb section as studied in this work, the band alignment transition would occur at $D_{InAs} \approx 7.3$ nm. **b**, Interface-pinned band alignment as a function of diameter. The energy difference between $E_{c,InAs}$ and $E_{v,GaSb}$ is constant in spite of changing diameter. **c**, Simulated J_{peak} *versus* D_{InAs} for Esaki diodes for both scenarios without fixed charge in oxide. **d**, Simulated $I_{d,max}(V_{ds} = 0.3\ V)$ *versus* D_{InAs} for tunneling transistors for both scenarios. The simulation structure is discussed in Methods, and is shown in Supplementary Fig. 10a. The adopted effective oxide thickness ($t_{ox,eff}$) and the dielectric constant for the oxide surrounding the source ($\varepsilon_{r,eff}$) are 12 nm and 2, respectively. Only the interface-pinned alignment could reproduce experimental results well.



Supplementary Fig. 8| a, Schematic bulk GaSb/bulk InAs (left) and bulk GaSb/confined InAs (right) structures used in the calculations. **b**, Atomic structure of the bulk GaSb/confined InAs situation, in which a 2-nm-wide InAs nanosheet is adopted. **c**,**d**, Calculated dispersion relation of the bulk GaSb/bulk InAs structure (**c**) and calculated dispersion relation of the bulk GaSb/confined InAs structure (**d**). Blue and red dots show projected contribution from GaSb and InAs onto each eigenstate, respectively, where a larger dot indicates a higher contribution. Band edges of GaSb and InAs are extracted and labeled in blue and red for GaSb and InAs, respectively. The bandgap values of each material are also labeled (unit: eV). An interface-pinned band alignment is demonstrated, as the energy difference between $E_{c,InAs}$ and $E_{v,GaSb}$ is nearly constant in spite of the strong quantum confinement induced from the 2-nm-wide InAs nanosheet. Note that a staggered-band alignment is seen from the calculations, agreeing well with the previous report with a similar method[S4]. The absence of the broken-band alignment is commonly seen in these types of calculations.



Supplementary Fig. 9| Coupled DFT-NEGF calculations. a,**b**, Calculated projected local density of states (PLDOS) of the bulk GaSb/bulk InAs structure (**a**) and the bulk GaSb/confined InAs structure (**b**). Extracted band edges are labeled in ivory. A broken-band alignment at the interface could be obtained with a p- (n-) doping in GaSb (InAs).



Supplementary Fig. 10| 3D quantum transport simulations of ultra-scaled HJ tunneling transistors. a, Cross section along the transport direction, z, of the simulated device structure. Different effective oxide thicknesses ($t_{ox,eff}$) and dielectric constants ($\varepsilon_{r,eff}$) were used for the oxide surrounding the source. C_{GaSb}, $C_{ox,eff}$, and φ_s denote GaSb capacitance, effective oxide capacitance at the source, and the surface potential at the GaSb/oxide interface, respectively. In actual devices, a large interface trap density (D_{it}) of ~8×10^{13} cm^{-3} at the GaSb/Al_2O_3 interface is estimated, which is expected to severely degrade the gate coupling to the GaSb (ref. S1). Because interface traps were not included in the simulations, we effectively emulated the reduced gate coupling to the source region by decreasing $C_{ox,eff}$, which was achieved by increasing $t_{ox,eff}$ to 12 nm and by diminishing $\varepsilon_{r,eff}$ to 2. This is because the gate efficiency, $d\varphi_s/dV_{gs} = C_{ox,eff}/(C_{ox,eff} + C_{GaSb})$, decreases as $C_{ox,eff}$ decreases. **b**, Simulated transfer characteristics with different $t_{ox,eff}$ and $\varepsilon_{r,ox}$. Unless otherwise stated, the dielectric constant of Al_2O_3 was set to $\varepsilon_{r,ox} = 8$. All the simulated curves have been shifted by a constant gate voltage to match the experimental voltage range. **c-f**, Band diagrams and the corresponding energy-resolved current spectra at $V_{ds} = 0.3$ V in the on-

state with lower V_{gs} (**c** and **d**) and in the on-state with higher V_{gs} (**e** and **f**) for $t_{ox,eff}$ = 3 nm, $\varepsilon_{r,eff}$ = 8 (**c** and **e**) and $t_{ox,eff}$ = 12 nm, $\varepsilon_{r,eff}$ = 2 (**d** and **f**). A wide source depletion region induces a negative g_m at a high V_{gs} (**e**). A narrower source depletion region, stemming from the weaker gate-source coupling, leads to a much higher BTBT current (**f**). The simulation results suggest that a high gate control efficiency over the source is unfavorable, while that to the channel is of the essence. Note that the observed current leakage floor in the experimental device is due to unavoidable trap-assisted tunneling (TAT) (ref. S1). Minimizing D_{it} at the InAs/oxide interface is of utmost importance.

Material	***GaSb***	***InAs***	***InSb***
a **(Å)**	6.096	6.059	6.48
E^{Γ}_{g} **(eV)**	0.812	0.417	0.235
m_e (m_0)	0.039	0.026	0.0135
γ_1	13.4	20.0	34.8
γ_2	4.7	8.5	15.5
γ_3	6.0	9.2	16.5
E_p **(eV)**	22	18	18
Δ_{SO} **(eV)**	0.76	0.39	0.81
VBO (eV)	0.56	0	0.59

Supplementary Table 1| Band-structure parameters used in simulations. a denotes lattice constant. E^{Γ}_{g} denotes bandgap at Γ point at 0 K. m_e denotes bulk electron effective mass. γ_1, γ_2, and γ_3 denote Luttinger parameters. E_P is defined to characterize matrix elements of the momentum operator between conduction and valence bands[74]. Δ_{SO} denotes spin–orbit split-off energy. VBO denotes valence band offset. All the parameters were adopted from (ref. 74) except for the E_p values that were adopted from (ref. S5) to avoid spurious solutions.

	D_{ac} (eV)	D_{op} (eV/cm)	$\hbar\omega_{op}$ (meV)
Electrons	5.8	30×10^8	30
Holes	1	30×10^8	30

Supplementary Table 2| Phonon scattering parameters used in quantum transport simulations. D_{ac} denotes acoustic-phonon deformation potential. D_{op} denotes effective polar-optical-phonon deformation potential. $\hbar\omega_{op}$ denotes optical-phonon energy. D_{ac} and $\hbar\omega_{op}$ were adopted from (ref. 74) while D_{op} was adopted from our previous study (ref. 60).

References

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