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Supplementary information

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High-transconductance molybdenum disulfide top-gate transistors using epitaxial interface engineering

In the format provided by the authors and unedited

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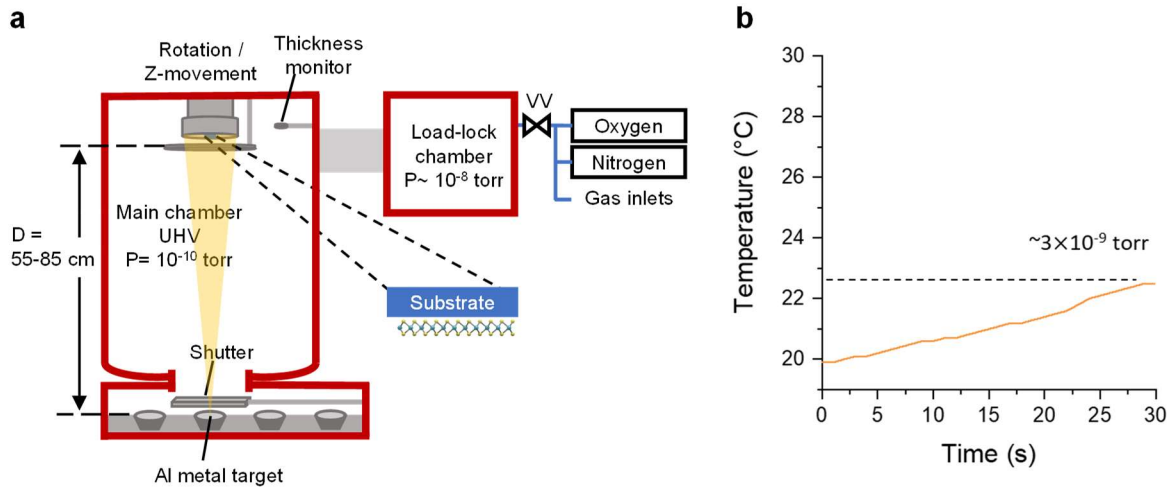
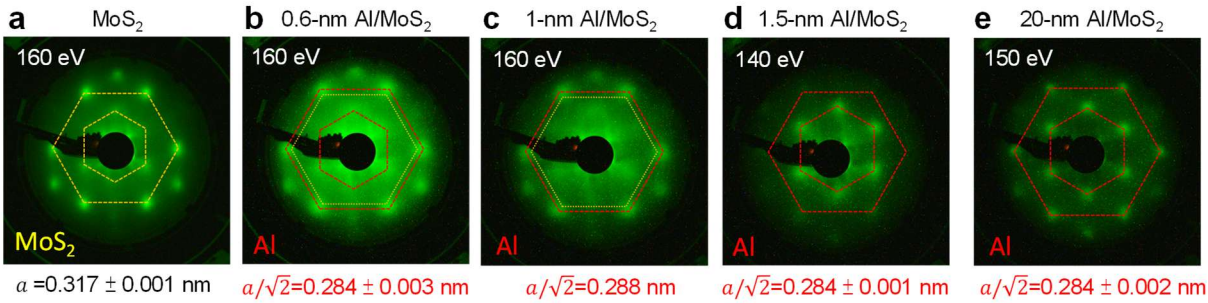
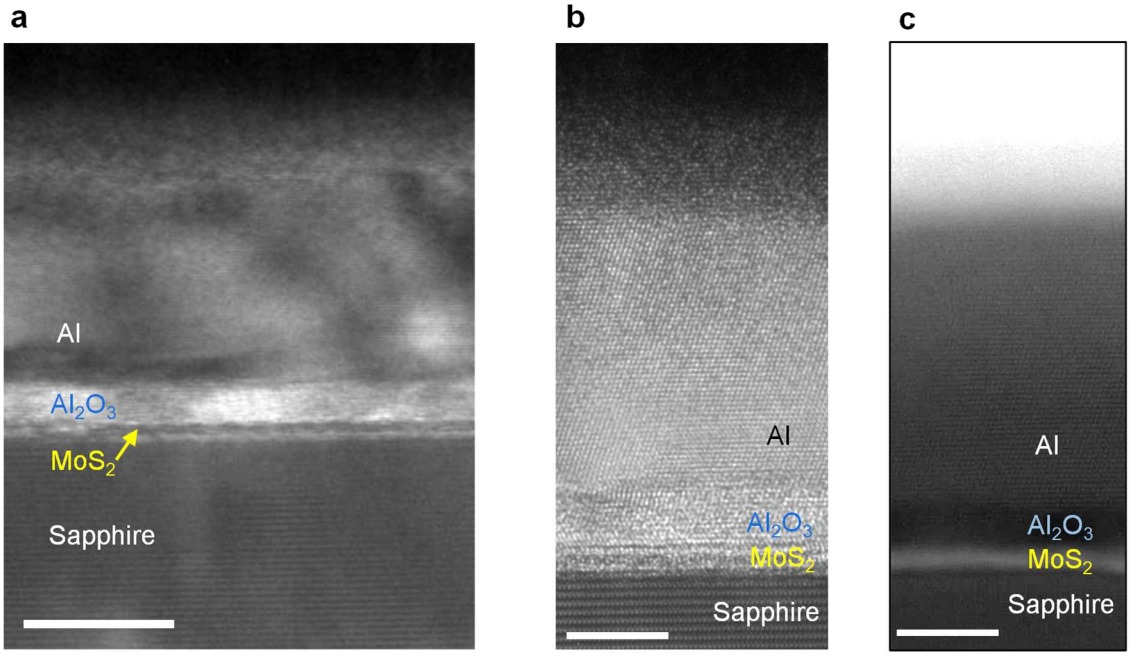


Supplementary Fig. 1 | UHV electron-beam evaporator and in-situ oxidation system. **a,** Schematic of the UHV electron-beam evaporator. The specially designed system consists of a main deposition chamber and a load-lock chamber with gas inlets (O_2 and N_2) for in-situ oxidation. Prior to deposition, the main chamber was maintained at a base pressure of ~10^{-10} torr. The working distance D between the target material and the sample holder is tunable from 55 to 85 cm and was kept at D~ 70 cm to avoid radiative heating of the MoS_2 by the melted metal. A low deposition rate of 0.1 Å s^{-1} was used to prevent damages on the MoS_2 surface. After deposition, the sample was transferred to the load-lock chamber for in-situ oxidation. By controlling the O_2 pressure and oxidation time, the deposited epitaxial Al can be fully oxidized in a gentle way, forming an ultrathin, dense, and uniform Al_2O_3 layer on the MoS_2 surface. **b,** The substrate temperature as a function of Al deposition time. The substrate temperature was monitored at the sample holder during the Al deposition for 30 seconds with a deposition rate of 0.1Å/s. The temperature increase is less than 3°C after Al deposition. During evaporating Al, the base pressure slightly increases to 3×10^{-9} torr.

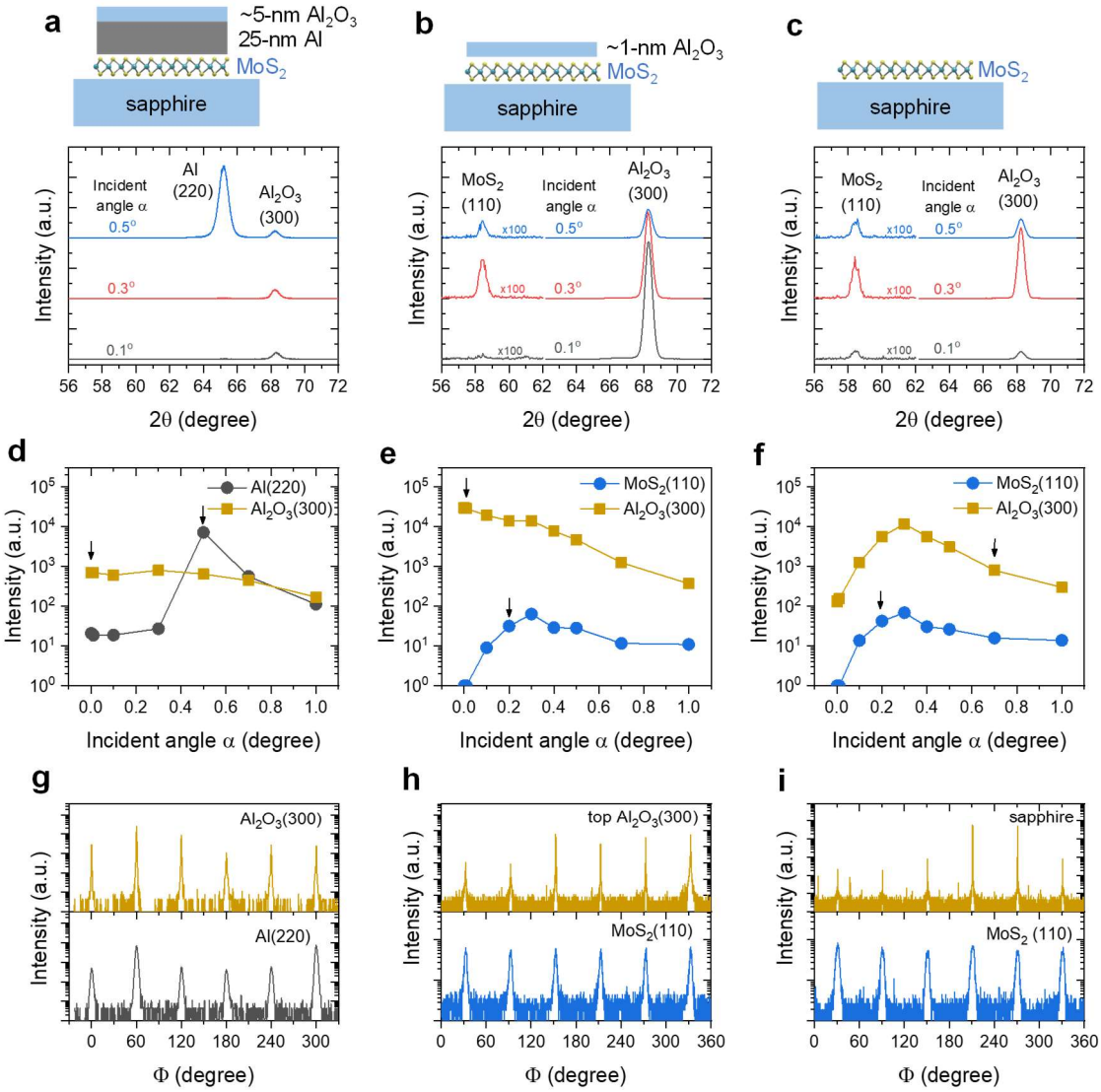


Supplementary Fig. 2 | LEED patterns of Al growth on monolayer MoS_2.
a, Pristine monolayer MoS_2 showing the characteristic hexagonal diffraction spots, corresponding to its lattice constant (interatomic spacing ≈ 0.317 nm). **b-e,** MoS_2 after deposition of Al with a nominal thickness of 0.6 (b), 1.0 (c), 1.5 (d) and 20 nm, respectively, where new diffraction spots emerge and expand outward, with an interatomic spacing of ~0.284 nm, consistent with the Al-Al spacing ($a/\sqrt{2}$) of the Al(111) surface. The Al diffraction spots are azimuthally aligned with those of MoS_2, indicating epitaxial alignment. The LEED patterns remain essentially unchanged for Al thicknesses ranging from 0.6 to 20 nm, confirming that epitaxial growth is continuously preserved from sub-nanometer coverage to thicker films. Given the LEED electron beam size of ~3 mm in diameter, the observation of well-defined diffraction spots further indicates that the epitaxial alignment extends over a millimeter-scale area.

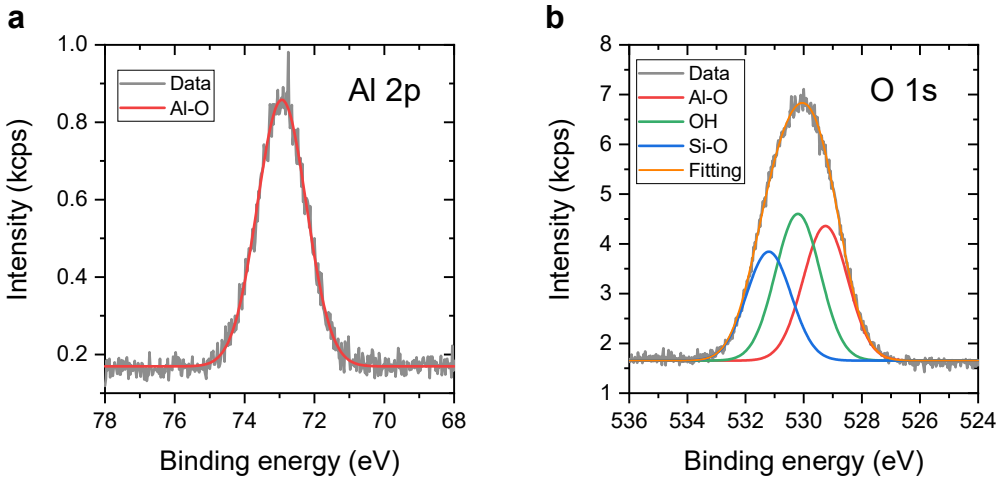


Supplementary Fig. 3 | Cross-sectional HR-TEM of Al/Al_2O_3/MoS_2 heterostructure on sapphire.

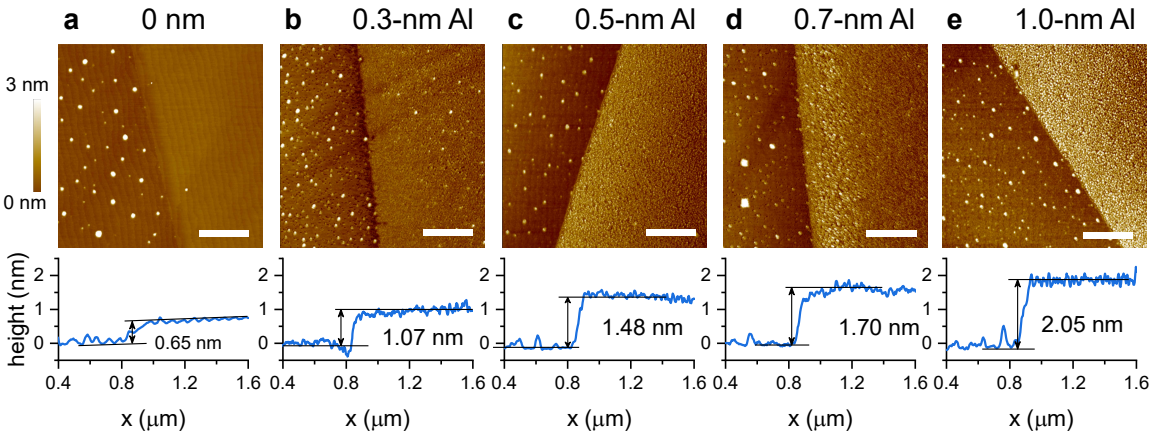
a, Low-magnification bright-field cross-sectional HR-TEM image of the Al/Al_2O_3/MoS_2/sapphire structure. Scale bar, 10 nm. **b,** Higher-magnification bright-field HR-TEM image of the same region, showing discernible lattice fringes in the Al_2O_3 interfacial layer and the overlying Al film. Scale bar, 5 nm. **c,** Corresponding high-angle annular-dark-field (HAADF) image of the region shown in b. Scale bar, 5 nm.



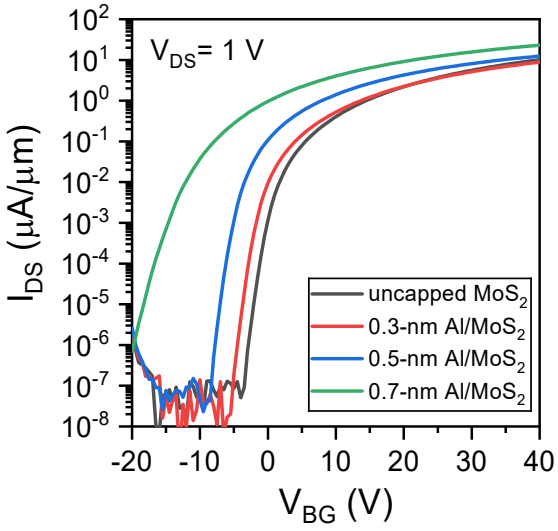
Supplementary Fig. 4 | Grazing-incidence in-plane x-ray diffraction (GIIXRD) characterizations of epitaxially derived Al_2O_3 interfacial layer. a-c, In-plane 2θ scans of the three representative sample structures measured at different incident angles (α=0.1°, 0.3° and 0.5°). Schematic illustrations of the corresponding sample structures are shown in the upper panels. **d-f,** Corresponding diffraction peak intensities as a function of incident angle α for the three sample structures shown in a-c. **g-i,** In-plane Φ scans of the surface Al_2O_3 and underlying Al (structure a), surface Al_2O_3 and underlying MoS_2 (structure b), and surface MoS_2 and sapphire substrate (structure c). The incident angle used for each Φ scan is indicated by arrows in d-f.



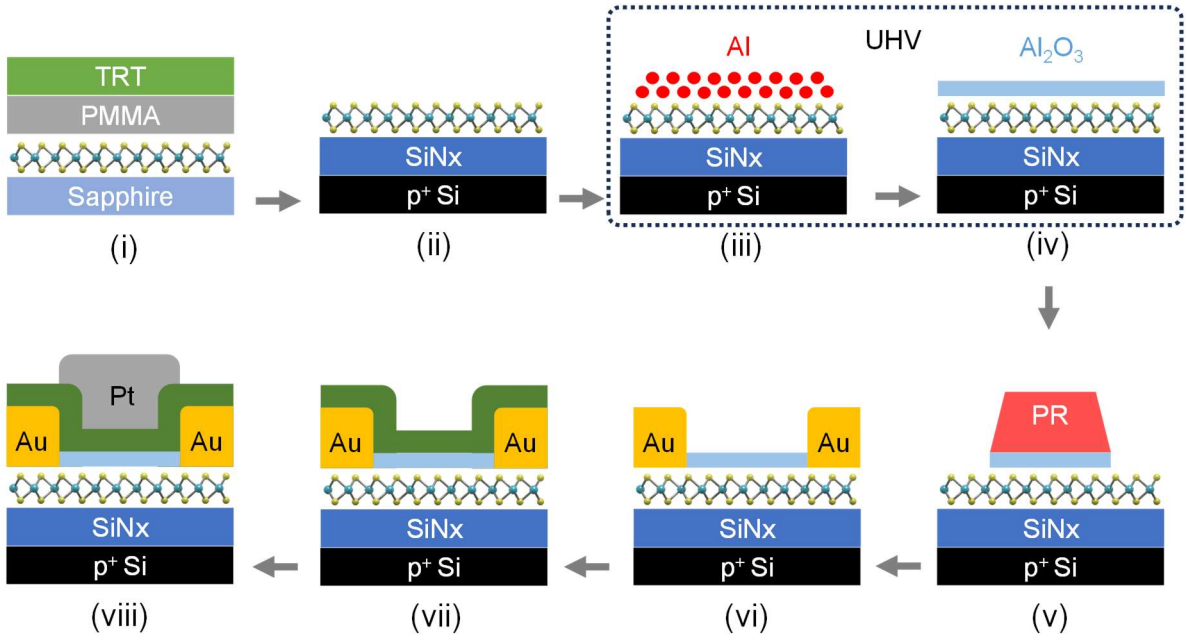
Supplementary Fig. 5 | XPS spectra of Al_2O_3 derived from epitaxial Al on MoS_2. **a,** The Al-2p core level spectrum of Al_2O_3/MoS_2, showing a single peak from the Al-O bonds without signals from Al-Al and Al–OH bonds, confirming that the 0.3-nm Al layer has been fully oxidized without detectable hydroxide related defects. **b,** The O-1s core level spectrum of the Al_2O_3/MoS_2, showing contributions from Al-O, OH, and Si-O bonds. Since doped Si substrate was used for XPS measurements, the Si-O and OH are attributed to the substrate signals. The ratio of Al and O bonded to Al is about 1:1.49 obtained from the peak area normalized to the sensitivity factor of the XPS system.



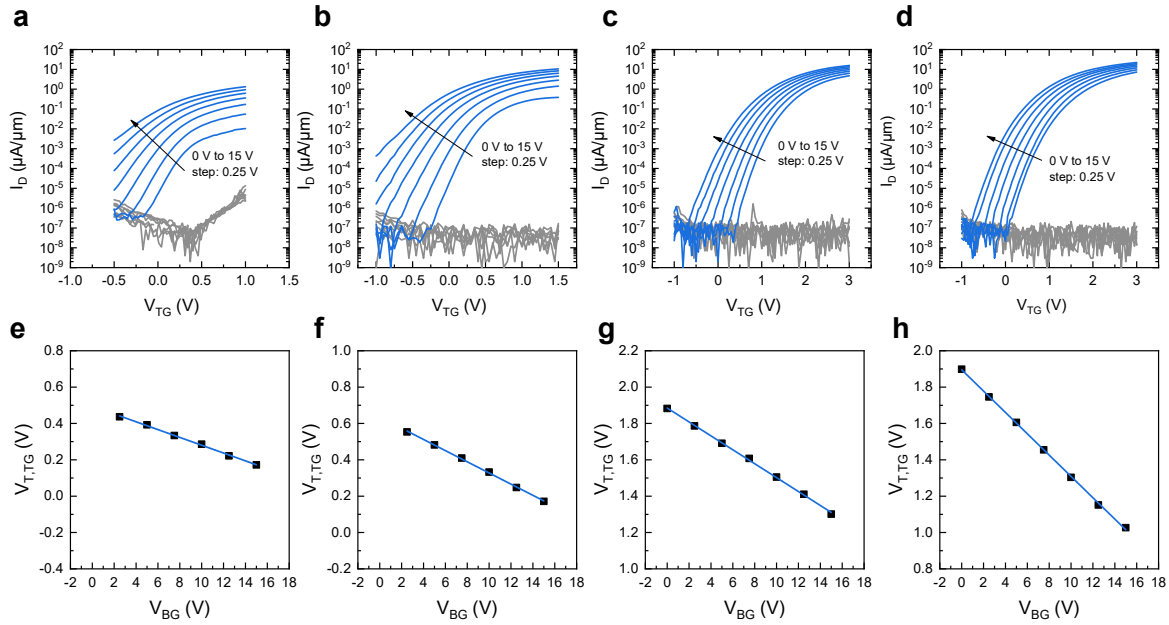
Supplementary Fig. 6 | AFM of Al_2O_3 on MoS_2 with different nominal Al thicknesses. a-e, AFM images of CVD-grown monolayer MoS_2 flakes covered with Al_2O_3 derived from epitaxially-grown Al layers with a nominal thickness of 0.3 nm (b), 0.5 nm (c), 0.7 nm (d), and 1 nm (e). The bottom panel shows the corresponding AFM line scans across the edge of MoS_2 flakes. The sapphire surface is not fully covered by Al due to the preferential island growth. We determine the height of single-layer MoS_2 and those covered with Al_2O_3 from the AFM line scans.



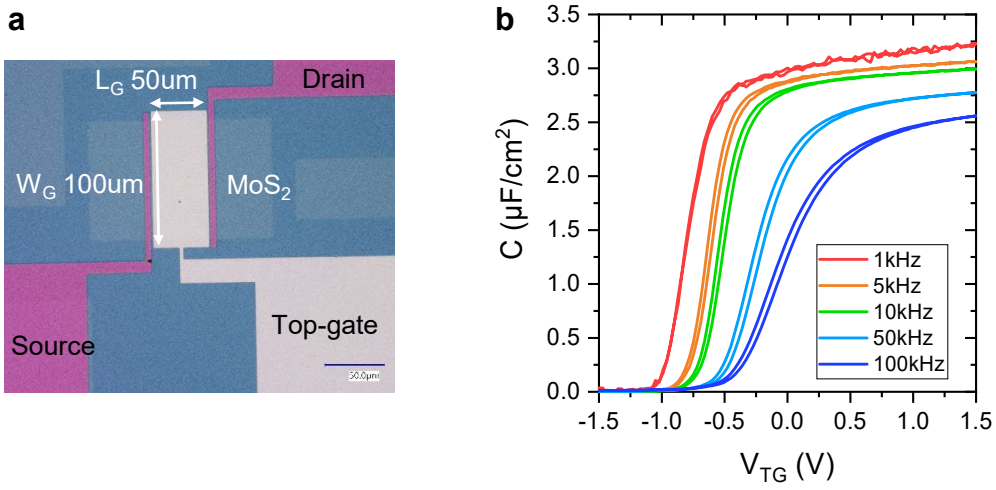
Supplementary Fig. 7 | Transfer curves of MoS_2 back-gate FETs with and without Al_2O_3 capping on the channel. The uncapped device (grey) shows a similar transfer characteristic with the device capped with 0.3-nm Al layer (red). As the Al thickness is gradually increased, the threshold voltage (V_T) shift becomes more pronounced. In particular, when the Al thickness reaches 0.7 nm, a substantial V_T shift is observed, clearly indicating strong n-type doping of the underlying MoS_2, consistent with previous reports on AlO_x-induced doping in MoS_2. These results highlight the critical role of using an ultrathin Al seeding layer in this work: by limiting the Al_2O_3 thickness to the sub-nanometer regime via epitaxial growth of Al and controlled oxidation, the doping effect on MoS_2 can be effectively minimized while still enabling uniform high-κ dielectric integration.



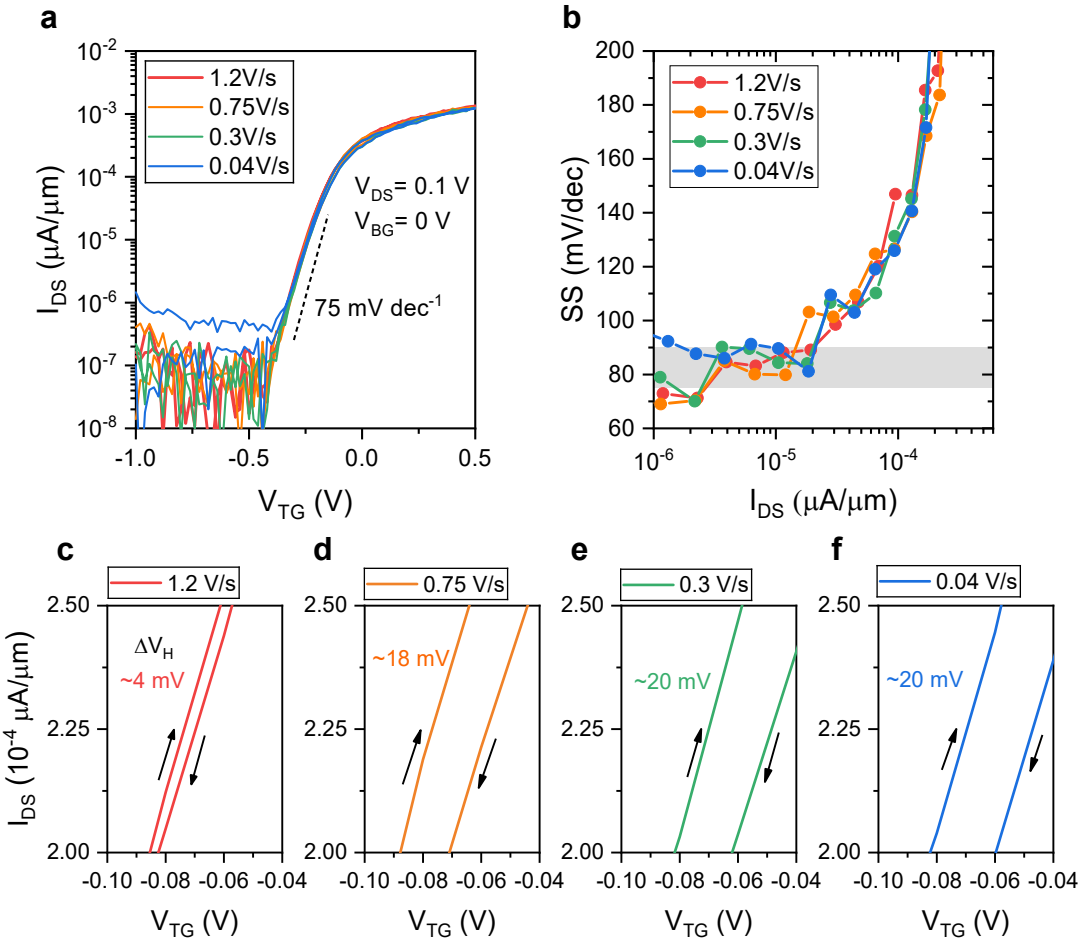
Supplementary Fig. 8 | The fabrication process flow of double-gate MoS_2 FETs. The process flow includes the following steps. (i) The CVD-grown MoS_2 film on sapphire was spin-coated with PMMA (950 A4) at 2000 rpm for 60 s (~300 nm thick) followed by baking at 180 °C for 180 s. Then a thermal release tape (TRT) was pressed on the PMMA/MoS_2/sapphire stack using a custom-built bonding tool. The TRT/PMMA/MoS_2 stack was detached from the sapphire substrate by immersing in 1M NaOH (aq) for 1 hour followed by rinsing in deionized water. (ii) The TRT/PMMA/MoS_2 stack was transferred in vacuum onto a 100-nm SiN_x/highly doped Si substrate using the bonding tool to obtain a wrinkle-free MoS_2 film on the SiN_x/Si substrate. The PMMA layer was then removed using acetone, followed by rinsing in isopropanol alcohol. Finally, the sample was subjected to a low-pressure rapid thermal annealing (RTA) process to remove surface residues. (iii) The sample was loaded into the main chamber of a UHV e-beam evaporator as described in supplementary Fig. S1 to grow a 0.3-nm Al epitaxial layer on MoS_2. (iv) The sample was then transferred to the load-lock chamber to proceed an in-situ low-pressure oxidation to form an Al_2O_3 interfacial layer (IL) but avoiding oxidation to the MoS_2. (v) The source/drain (S/D) contact regions were defined by photolithography on the Al_2O_3 IL, which is referred to as an Al_2O_3-first process. In the Al_2O_3-first process, the ultra-thin Al_2O_3 was etched away by the developer (AZ300MIF) used in S/D photolithography, leaving behind the S/D contact openings without photoresist residues on the MoS_2 surface. (vi) The contacts were formed by UHV e-beam evaporation of 25-nm Au followed by lift-off processes. (vii) A HfO_2 layer was grown by ALD on the Al_2O_3 IL to form the top-gate dielectric stack. (viii) The gate metal contacts were defined by photolithography and deposited by UHV e-beam evaporation. Finally, the devices were subjected to a low-pressure RTA (400°C, 6 torr, 1 min) in forming gas to remove organic residues caused during the fabrication process and to improve the dielectric quality before electrical measurements.



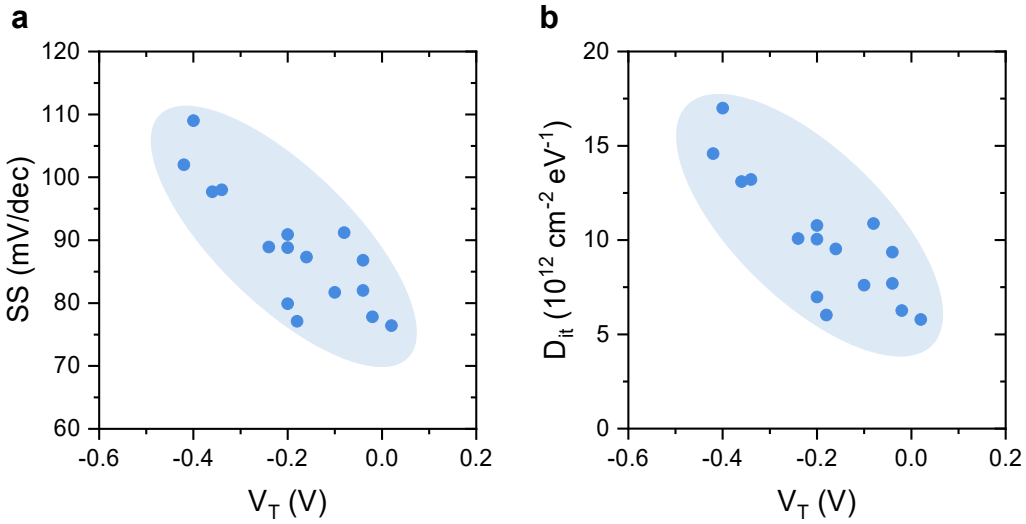
Supplementary Fig. 9 | Double-gate I-V measurements to extract C_{TG}.
a-d, Transfer curves of the top-gate FET with HfO_x thickness $t_{HfO_2} = 2.85$ nm (a), 3.65 nm (b), 5.45 nm (c), and 8.95 nm (d) at different back-gate voltages V_{BG} from 0 to 15 V with a step of 2.5 V. **e-h,** The extracted top-gate threshold voltage $V_{T,TG}$ as a function of applied V_{BG}. The capacitance ratio of C_{TG}/C_{BG} was obtained from the slope of the linear fit (red line) to the $V_{T,TG}$-V_{BG} relation. The C_{BG} was determined from capacitance measurements on the 100-nm thick SiN_x on a p-doped Si substrate.



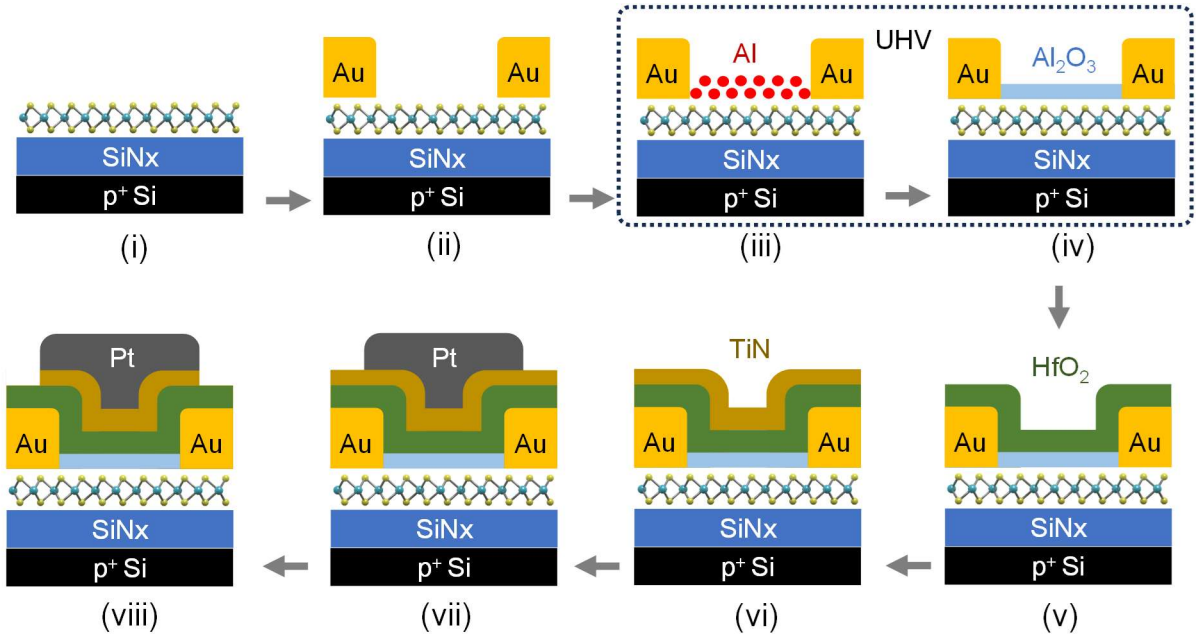
Supplementary Fig. 10 | C-V measurements of top-gate dielectric stacks on CVD-grown MoS_2. a, Optical microscope image of a super-long-channel ($L_G = 50$ μm) top-gate FET for C-V measurements. The large channel area of 5,000 μm^2 facilitates capacitance measurements. The gate stack consists of a 0.42-nm Al_2O_3 layer and a 2.85-nm HfO_2 layer. **b,** C-V curves measured at different frequencies from 1 kHz to 100 kHz. The C-V curves exhibit small hysteresis at low frequencies. The gate capacitance of 3.25 μF cm^{-2} corresponds to an EOT of 1.06 nm.



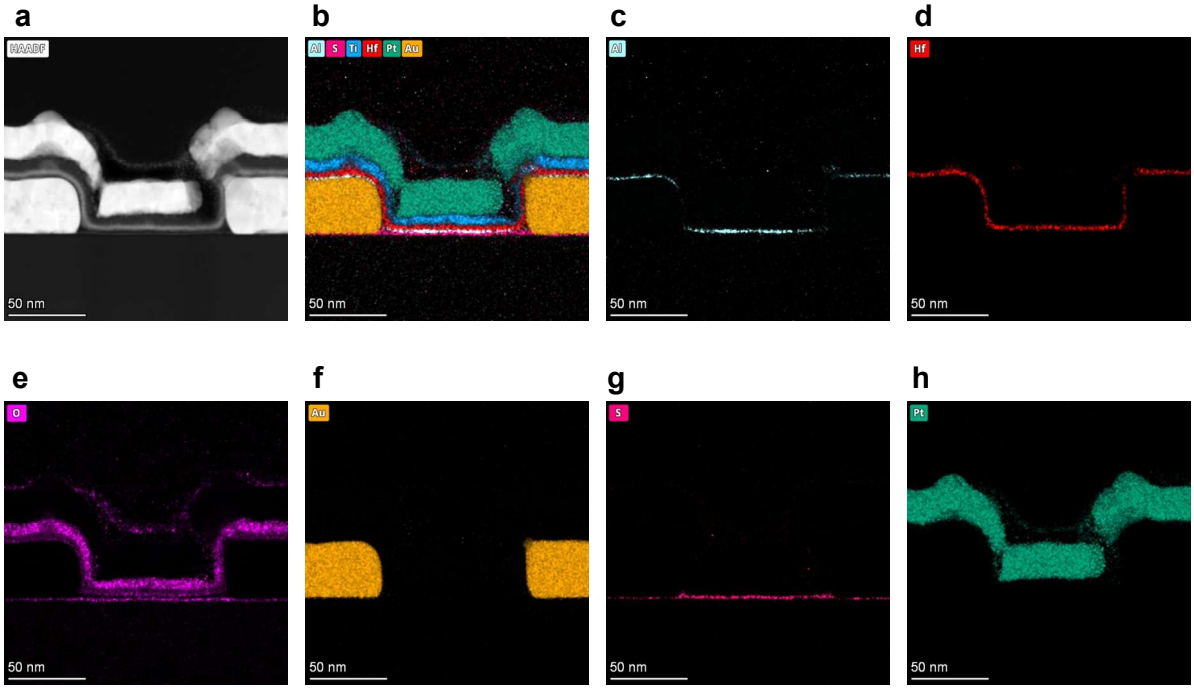
Supplementary Fig. 11 | Sweep-rate-dependent transfer curves, SS and hysteresis. **a,** Transfer curves measured at different top-gate-voltage sweep rates: 0.04, 0.3, 0.75 and 1.2 V s^{-1}. **b,** The extracted SS as a function of I_{DS} for different top-gate-voltage sweep rates. **c-f,** Zoom-in bidirectional transfer curves to visualize the hysteresis windows ΔV_H at different top-gate sweep rates: **c,** 1.2 V s^{-1}; **d,** 0.75 V s^{-1}; **e,** 0.3 V s^{-1}; **f,** 0.04 V s^{-1}. Arrows indicate forward and reverse sweeps. The close overlap of SS–I_{DS} characteristics indicates weak sweep-rate dependence. The hysteresis remains small even at the slowest sweep rate, suggesting that slow carrier capture/emission processes effects do not dominate the switching characteristics.



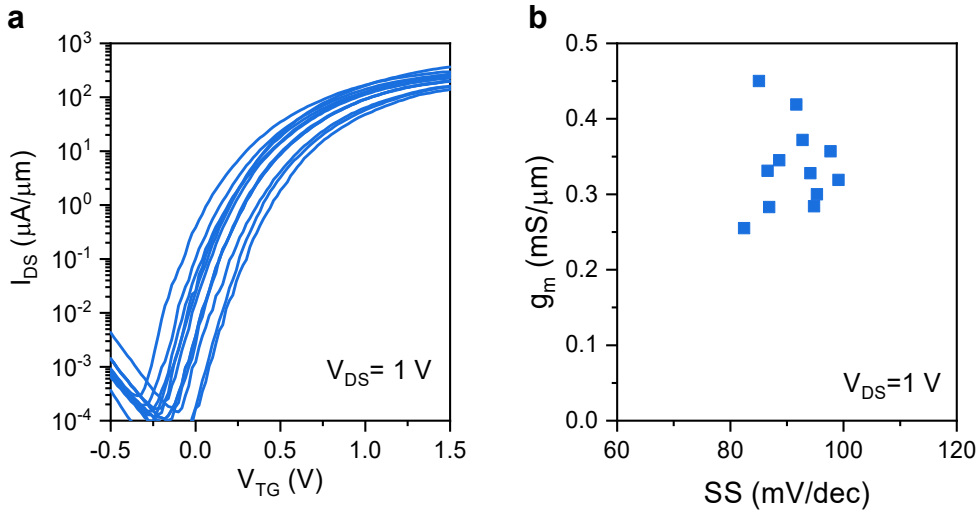
Supplementary Fig. 12 | The statistic distribution of the SS, D_{it} and V_T from Fig. 3i. **a**, Scatter plot of sub-threshold swing (SS) versus threshold voltage (V_T) extracted from I_D-V_{TG} curves of n=16 devices using $V_{DS} = 0.1$ V and $V_{BG} = 0$ V. **b**, The corresponding D_{it} extracted from **a**. The shaded ellipse highlights the overall dispersion. An increasing trend in SS with reducing V_T can be seen. We attribute this correlation to an additional interfacial capacitance introduced by organic residues trapped at the Al_2O_3/MoS_2 interface caused by the transfer process. The residues degrade the electrostatic integrity of the channel, and hence shifting V_T negatively and enlarging SS.



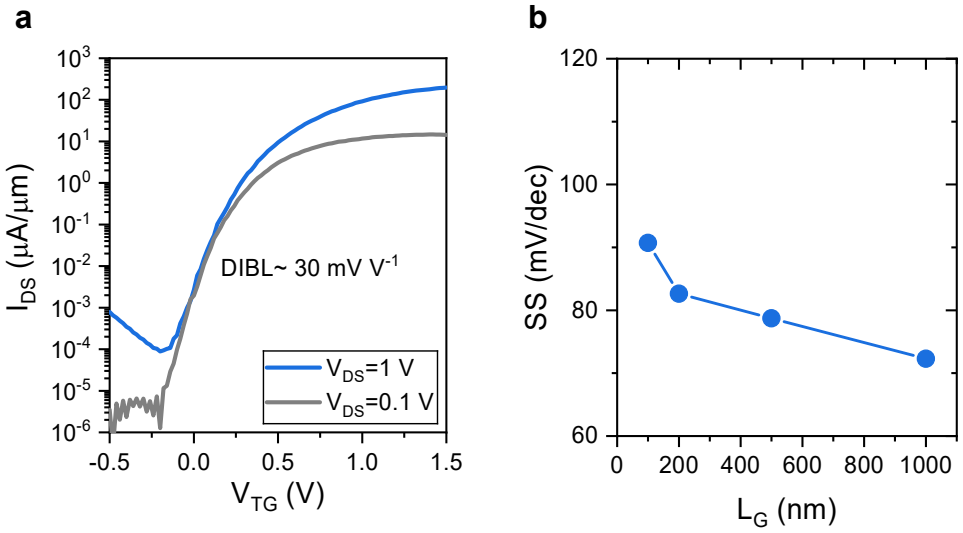
Supplementary Fig. 13 | The fabrication process flows of shorter channel top-gate FETs. (i) The MoS_2 films were transferred onto SiN_x/p^+ Si substrates using the same process as described in Fig. S8 for long-channel top-gate FETs. (ii) The S/D contact metals were fabricated by e-beam lithography (EBL) and e-beam evaporation prior to the formation of the Al_2O_3 IL, which is referred to as an Al_2O_3-last process. The primary reason for using the Al_2O_3-last process in the fabrication of shorter-channel devices is due to the fact that the EBL developer does not etch Al_2O_3. (iii) The Al_2O_3 IL was formed by epitaxial growth of Al by UHV e-beam evaporation, followed by (iv) low-pressure oxidation in the load-lock chamber. (v) The gate dielectric stacks were formed by ALD of a HfO_2 layer on the Al_2O_3 IL, followed by (vi) another ALD of a TiN layer as the gate metal. Due to the directionality of e-beam evaporation, the deposited metal may not fully cover the entire short-channel region. Therefore, ALD TiN was used as the metal to ensure conformal coverage on the channel region. (vii) A Pt layer was deposited to form a second gate metal overlapping the source/drain. (viii) Finally, the TiN outside the Pt top gate region was removed by dry etching.



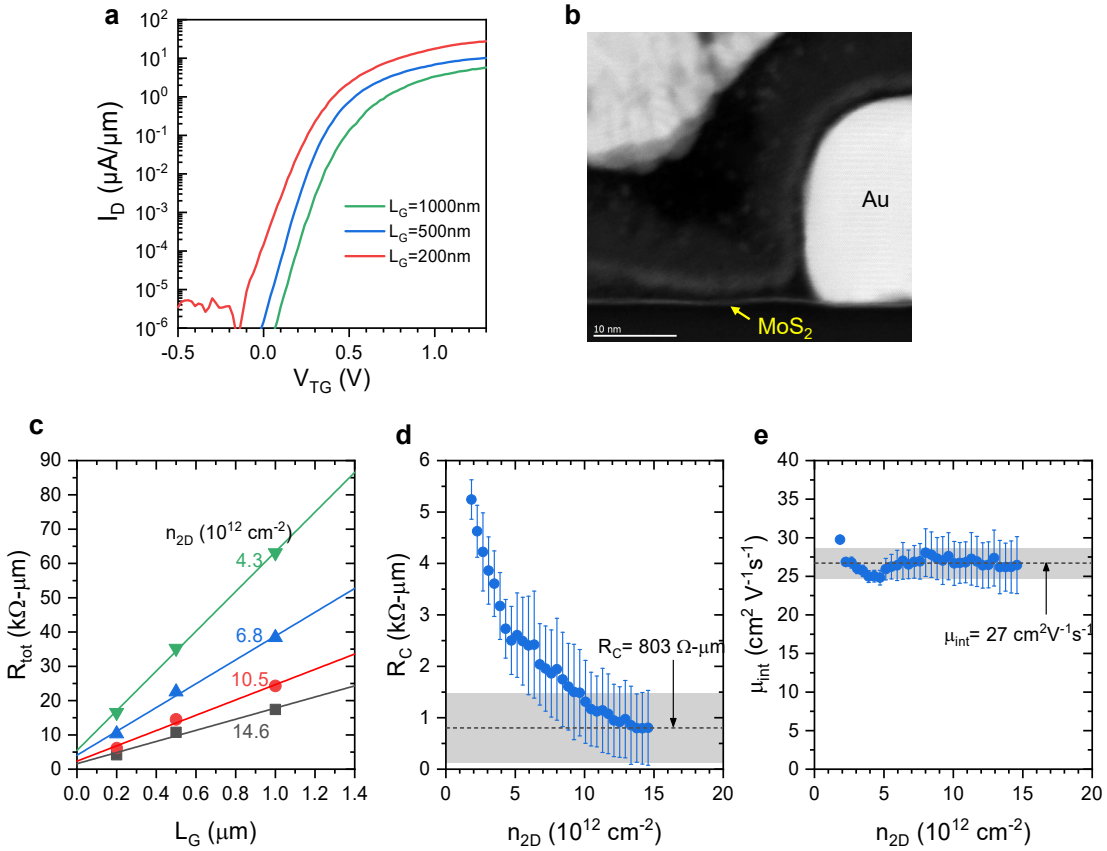
Supplementary Fig. 14 | Cross-sectional TEM characterizations of shorter channel top-gate FETs. a, Cross-sectional high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image of the shorter channel top-gate FET device. The fabricated source-drain distance is $L_{SD} \simeq 93$ nm with an effective gate length of $L_G \simeq 88$ nm. The scale bar is 50 nm. **b-i,** The energy-dispersive spectroscopy (EDS) maps of the spatial distributions for all elements (b), aluminum (c), hafnium (d), oxygen (e), gold (f), sulfur (g), and platinum (h). The EDS maps confirm the uniform and ultrathin Al_2O_3 and HfO_2 dielectric stack. Due to the Al_2O_3-last process, the Al_2O_3 IL covers on both the channel and the contact metals, enabling the ALD HfO_2 layer to cover conformally on the channel region.



Supplementary Fig. 15 | Statistical distribution of g_m and SS for shorter-channel devices. **a,** Top-gate transfer curves measured from n=12 devices with $L_{SD} \approx 100$ nm under the same bias condition ($V_{DS} = 1$ V and V_{BG} floating). **b,** Statistical distribution of g_m versus SS extracted from transfer curves. Each symbol represents an individual device.



Supplementary Fig. 16 |Short-channel electrostatic characteristics of top-gated MoS_2 transistors. a, Transfer characteristics of a representative device with $L_G \approx 100$ nm measured at low and high drain bias ($V_{DS} = 0.1$ and 1 V), showing a modest drain-induced barrier lowering (DIBL) of $\sim 30\ \mathrm{mV\,V^{-1}}$, indicative of good electrostatic control. **b,** Extracted subthreshold swing (SS) as a function of gate length L_G. Only a slight increase in SS is observed as L_G is scaled down to 100 nm, suggesting that conventional short-channel effects are not prominent at this dimension.



Supplementary Fig. 17 | Extraction of top-gate FET contact resistance via transfer length method. a, Transfer curves of the top-gate FET with L_G from 200 to 1000 nm at $V_{DS} = 0.1$ V. **b,** The cross-sectional HAADF-STEM images near the contact region. **c,** The total resistance R_{tot} as a function of gate lengths L_G at different carrier concentration n_{2D}. **d,** Measured R_C as a function of n_{2D}. The lowest contact resistance reaches $R_C = 803\ \Omega \cdot \mu m$ at $n_{2D} = 1.46 \times 10^{13} \mathrm{cm}^{-2}$. **e,** The extracted the intrinsic channel mobility μ_{int} as a function of n_{2D}. The average intrinsic mobility is $\mu_{int} = 27 \pm 2\ \mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$. The error bars are deduced from fitting errors.

Supplementary Table 1 | Benchmarking of EOT and SS of the state-of-the-art top-gate dielectric stacks integrated on 1L MoS_2.

Dielectric	Seeding method	Channel	EOT (nm)	SS ($mVdec^{-1}$)	D_{it} (10^{12} cm^{-2} eV^{-1})	Thermal stability	Ref
ALD 200°C HfO_2	Ozone	Exfoliated 1L MoS_2	1.5	69	0.02	400°C FGA	1
ALD 95°C HfO_2	Ozone	Exfoliated 1L MoS_2	2.1	75	5	NA	2
ALD 300°C Al_2O_3	Forming gas plasma	Exfoliated 1L MoS_2	3.55*	85	2.6	300°C ALD	3
ALD 200°C Al_2O_3	Oxygen plasma	Exfoliated 1L MoS_2	2.9	101	5.1	NA	4
ALD 150°C Al_2O_3	PTCDA	Exfoliated 1L MoS_2	1	60	0.8	NA	5
ALD 150°C Al_2O_3	PTCDA	CVD 1L MoS_2	1.3	160	~1	NA	5
ALD 95°C HfO_2	TE 1-nm Y	Exfoliated 1L MoS_2	4.42*	65	2.3	NA	6
ALD 250°C HfO_2	EBE 3-nm Hf	Exfoliated 1L MoS_2	2.3*	180	19*	NA	7
ALD 150°C ZrO_2	Direct LT-ALD	CVD 1L MoS_2	2.3	90	2.6	300°C PDA	8
ALD 200°C HfO_2	Nanofog AlO_x	CVD 1L MoS_2	1.3	100	11*	NA	9
ALD HfO_2	TE 1.5-nm Al	CVD 1L MoS_2	2	140	15*	NA	10
TE Er_2O_3	TE and oxidation	Exfoliated 1L MoS_2	1.1	90	0.6	NA	11
ALD 140°C HfO_2	TE Sb_2O_3	Exfoliated 1L MoS_2	0.67	60	0.22	NA	12
ALD 140°C HfO_2	TE Sb_2O_3	CVD 1L MoS_2	1	73	4.9*	NA	12
ALD 200°C HfO_2	EBE 0.3-nm Si	CVD 1L MoS_2	0.9	80	8.2*	NA	13
ALD 250°C HfO_2	EBE 0.3-nm epitaxial Al	CVD 1L MoS_2	1.06	75	5	400°C PMA	This work

* Calculated value from other parameters

ALD: Atomic layer deposition; PGA: Forming gas annealing; LT: Low-temperature; PDA: Post-deposition annealing; TE: Thermal evaporation; EBE: E-beam evaporation

Supplementary Table 2 | Benchmarking of EOT and transconductance g_m maximum of 2D FETs with different channel length L_G.

L_G (nm)	Channel	IL	Dielectric	Gate	EOT (nm)	g_m (mS μm^{-1})	I_{ON} @V_D= 1V ($\mu A\ \mu m^{-1}$)	S.S. (mV dec^{-1})	Ref.
10	Exfoliated 4-6 nm MoS_2	NA	7.5-nm HfO_2	LBG	2.5	0.142	520	130	14
50	CVD 1L WS_2	NA	8-nm BeO	BG	3.55	0,15	325	130	15
400	CVD 1L MoS_2	NA	16-nm HfO_2 1.2-nm TiO_2	LBG	NA	~0.025	~70	NA	16
100	CVD 1L MoS_2	NA	7-nm HfO_2	LBG	2	0.31	750	71.4	17
100	MOCVD 2L WS_2	ALD 1-nm Al_2O_3	10-nm HfO_2	DG	1.27 (CET)	0.12	210	109	18
100	MOCVD 1-2L MoS_2	ALD 1-nm $GdAlO_x$	4-nm HfO_2	DG	0.75 (CET)	0.32	420	~90	19
800	MOCVD 1L MoS_2	ALD 3.6-nm aBN	5.5-nm HfO_2	DG	NA	~0.05	~100	76.5	20
100	CVD 1L MoS_2 (2 sheets)	NA	15-nm HfO_2	GAA	NA	0.075	408	126	21
100	CVD 1L MoS_2	EBE 0.3-nm epitaxial Al	2.85-nm HfO_2	TG	1.06	0.45	330	90	This work

IL: interfacial layer; BG: back-gate; LBG: local back-gate; TG: top-gate; GAA: gate-all-around.

Reference

1. Bolshakov, P. *et al.* Improvement in top-gate MoS_2 transistor performance due to high quality backside Al_2O_3 layer. *Appl. Phys. Lett.* **111**, (2017).
2. Wang, J. *et al.* Integration of high-k oxide on MoS_2 by using ozone pretreatment for high-performance MoS_2 top-gated transistor with thickness-dependent carrier scattering investigation. *Small* **11**, 5932–5938 (2015).
3. Wang, X. *et al.* Improved integration of ultra-thin high-k dielectrics in few-layer MoS_2 FET by remote forming gas plasma pretreatment. *Appl. Phys. Lett.* **110**, 053110 (2017).
4. Yang, W. *et al.* The Integration of Sub-10 nm Gate Oxide on MoS_2 with Ultra Low Leakage and Enhanced Mobility. *Sci. Rep.* **5**, 11921 (2015).
5. Li, W. *et al.* Uniform and ultrathin high-κ gate dielectrics for two-dimensional electronic devices. *Nature Electronics* **2**, 563–571 (2019).
6. Zou, X. *et al.* Interface engineering for high-performance top-gated MoS_2 field-effect transistors. *Adv. Mater.* **26**, 6255–6261 (2014).
7. Kim, H. *et al.* Ultrathin monolithic HfO_2 formed by Hf-seeded atomic layer deposition on MoS2: Film characteristics and its transistor application. *Thin Solid Films* **673**, 112–118 (2019).
8. Chang, W. H. *et al.* ALD-ZrO_2 gate dielectric with suppressed interfacial oxidation for high performance MoS_2 top gate MOSFETs. *Jpn. J. Appl. Phys.* **60**, SBBH03 (2021).
9. Ko, J.-S. *et al.* Ultrathin Gate Dielectric Enabled by Nanofog Aluminum Oxide on Monolayer MoS_2. in *ESSDERC 2023-IEEE 53rd European Solid-State Device Research Conference (ESSDERC)* 1–4 (IEEE, 2023).
10. Xu, K. *et al.* Sub-10 nm Nanopattern Architecture for 2D Material Field-Effect Transistors. *Nano Lett.* **17**, 1065–1070 (2017).
11. Uchiyama, H., Maruyama, K., Chen, E., Nishimura, T. & Nagashio, K. A monolayer MoS2 FET with an EOT of 1.1 nm achieved by the direct formation of a high-κ Er_2O_3 insulator through thermal evaporation. *Small* **19**, 2207394 (2023).
12. Xu, Y. *et al.* Scalable integration of hybrid high-κ dielectric materials on two-dimensional semiconductors. *Nat. Mater.* **22**, 1078–1084 (2023).
13. Ko, J.-S. *et al.* Sub-nanometer equivalent oxide thickness and threshold voltage control enabled by silicon seed layer on monolayer MoS_2 transistors. *Nano Lett.* **25**, 2587-2593 (2025)14. Yang, L., Lee, R. T., Papa Rao, S. P., Tsai, W. & Ye, P. 10 nm nominal channel length MoS2 FETs with EOT 2.5 nm and 0.52 mA/μm drain current. in *2015 Annual Device Research Conference (DRC)*, pp. 237–238 (2015)..
15. Shi, X. *et al.* Improved Self-Heating in Short-Channel Monolayer WS_2 Transistors with High-Thermal Conductivity BeO Dielectrics. *Nano Lett.* **22**, 7667–7673 (2022).
16. Zhu, Y. *et al.* Monolayer Molybdenum Disulfide Transistors with Single-Atom-Thick Gates. *Nano Lett.* **18**, 3807–3813 (2018).
17. Fan, D. *et al.* Two-dimensional semiconductor integrated circuits operating at gigahertz frequencies. *Nature Electronics* **6**, 879–887 (2023).
18. Lin, D. *et al.* Dual gate synthetic WS_2 MOSFETs with 120μS/μm G_m 2.7μF/cm^2 capacitance and ambipolar channel. in *2020 IEEE International Electron Devices*

Meeting (IEDM), pp. 3.6.1–3.6.4 2020).

19. Wu, X. *et al.* Dual gate synthetic MoS_2 MOSFETs with 4.56μF/cm^2 channel capacitance, 320μS/μm Gm and 420 μA/μm Id at 1V Vd/100nm Lg. in *2021 IEEE International Electron Devices Meeting (IEDM)*, pp. 7.4.1–7.4.4 (2021).
20. Chen, C. Y. *et al.* Tailoring amorphous boron nitride for high-performance two-dimensional electronics. *Nat. Commun.* **15**, 4016 (2024).
21. Xiong, X. *et al.* Demonstration of Vertically-stacked CVD Monolayer Channels: MoS_2 Nanosheets GAA-FET with I_{on}>700 μA/μm and MoS_2/WSe_2 CFET. in *2021 IEEE International Electron Devices Meeting (IEDM)* , pp. 7.5.1–7.5.4 (2021).