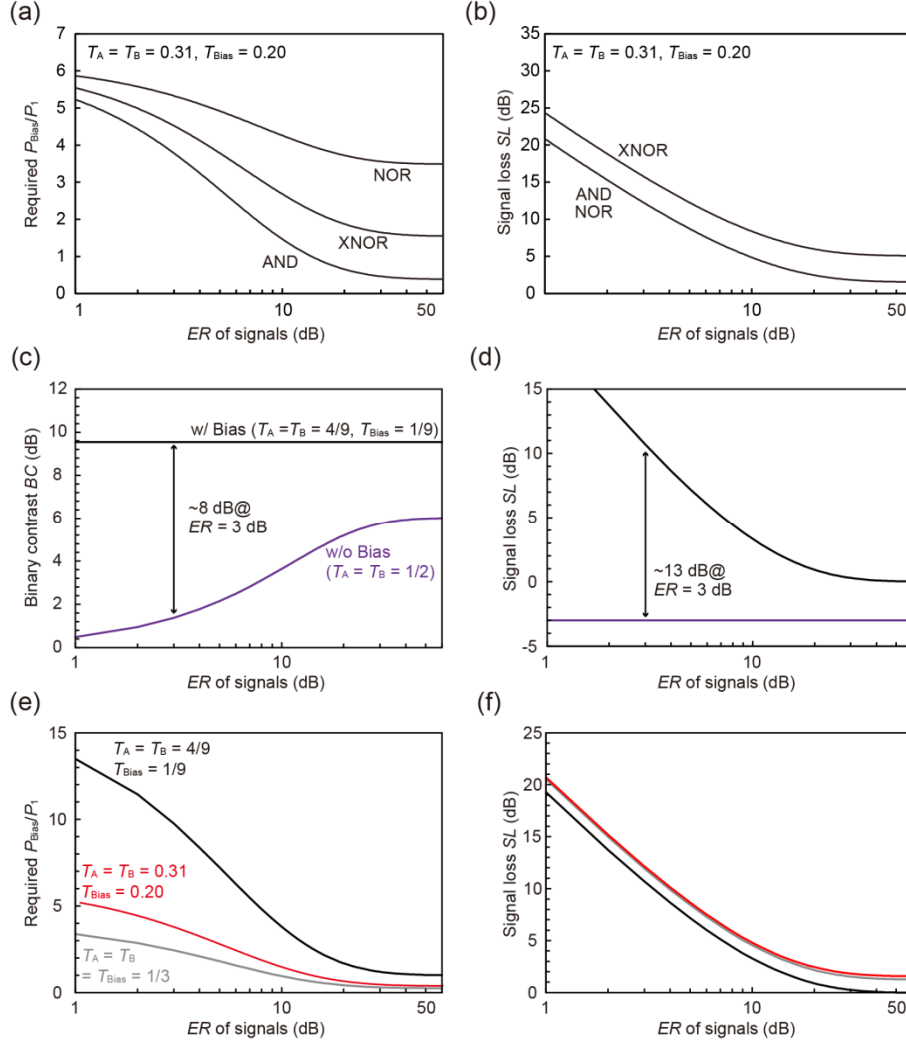
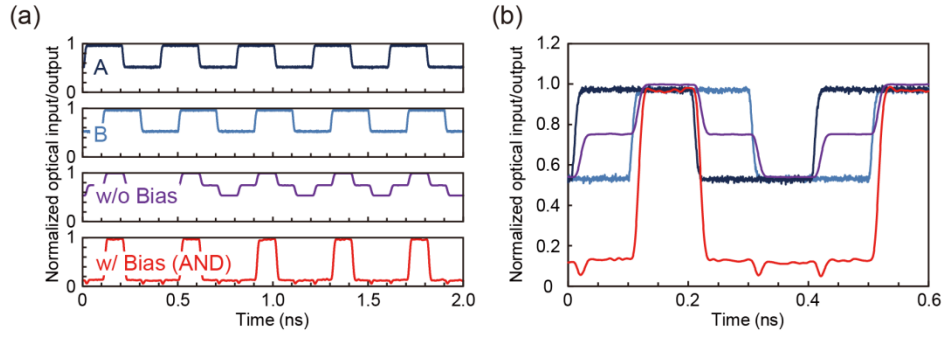


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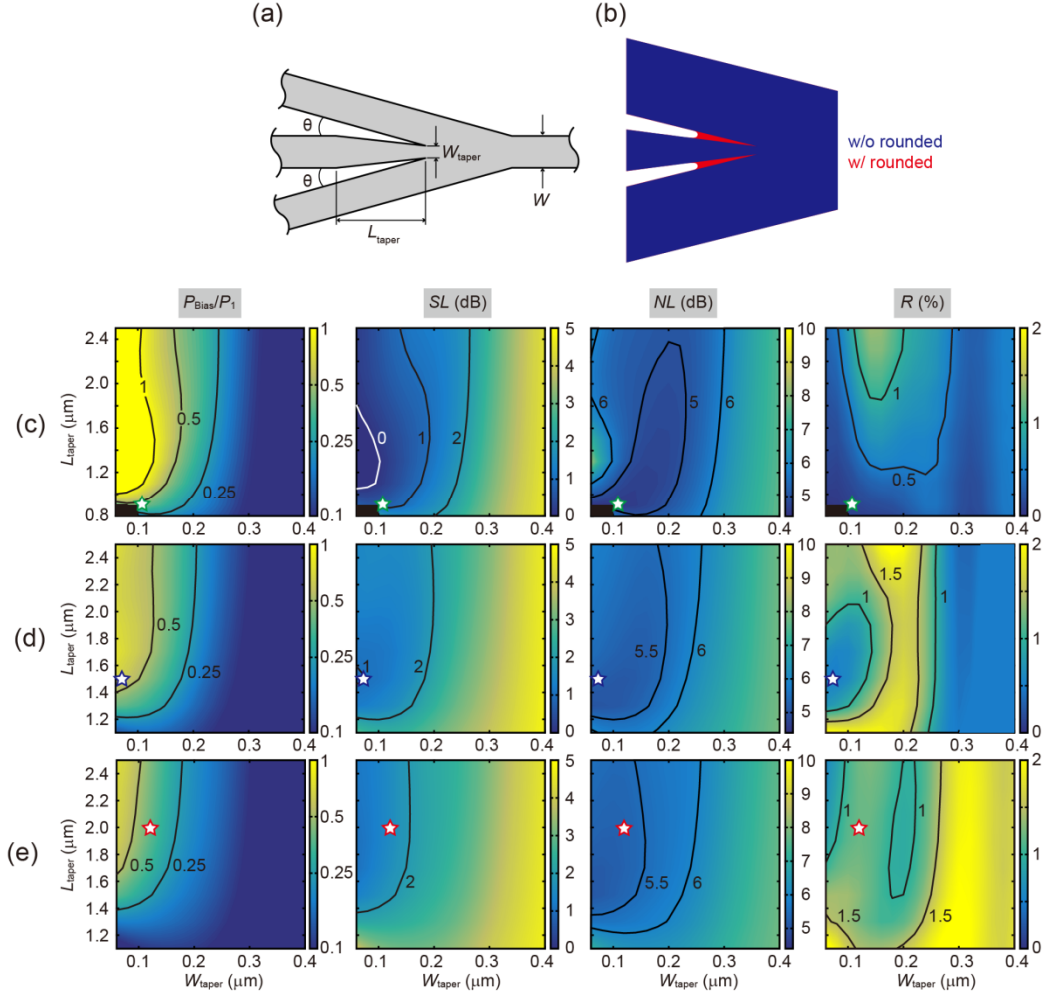
Supplementary Figures



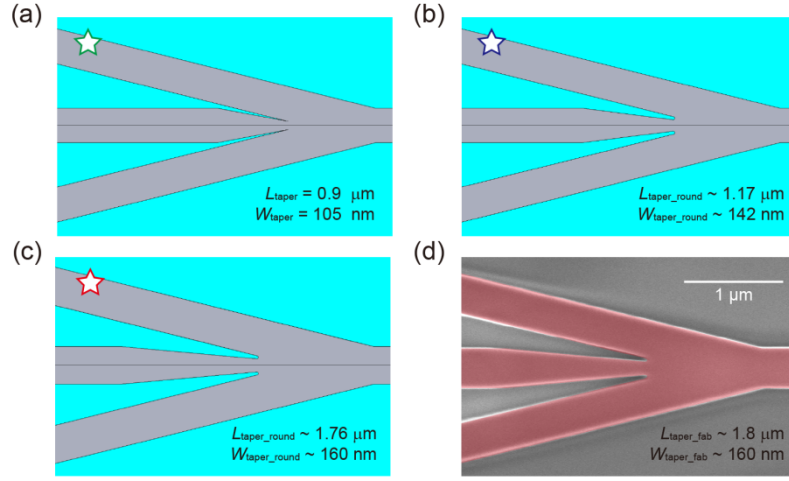
Supplementary Figure 1 | Operation conditioning under finite extinction ratio ER input signals with transmittances. (a) Required relative bias power P_{Bias}/P_1 vs. ER for different operations with assuming the experimental Ψ gate in the main text. (b) Signal loss SL vs. ER for different operations with assuming the experimental Ψ gate. The lines for AND and NOR are identical. (c) Binary contrast BC vs. ER for a Ψ gate (black line) and an ordinary beam splitter (purple line). (d) SL vs. ER for a Ψ gate (black line) and an ordinary beam splitter (purple line). (e) P_{Bias}/P_1 vs. ER for different Ψ gates. (f) SL vs. ER for different Ψ gates.



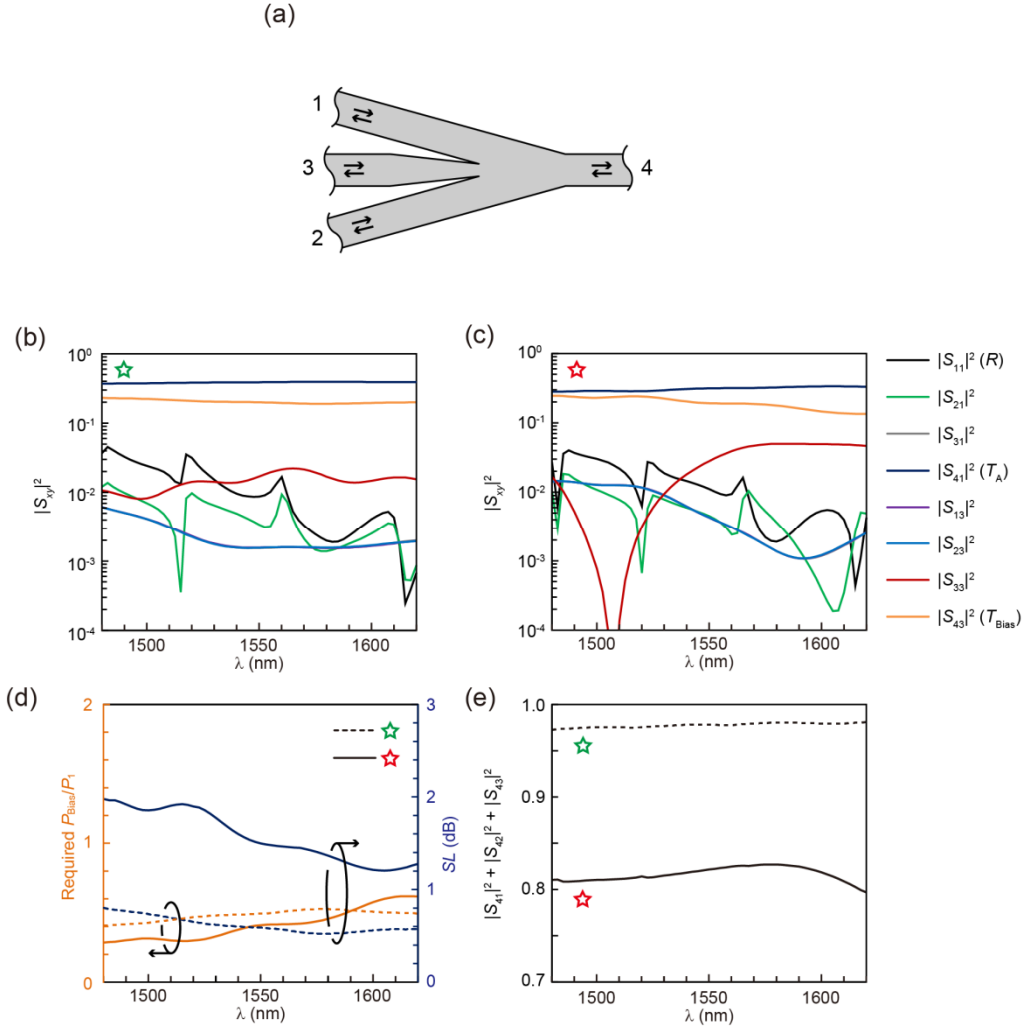
Supplementary Figure 2 | Simulation showing binary contrast *BC* recovery effect by applying larger Bias against poor extinction ratio *ER* input signals. (a) Simulated time waveforms of input and output without and with Bias. (b) Detail comparison of all the waveforms.



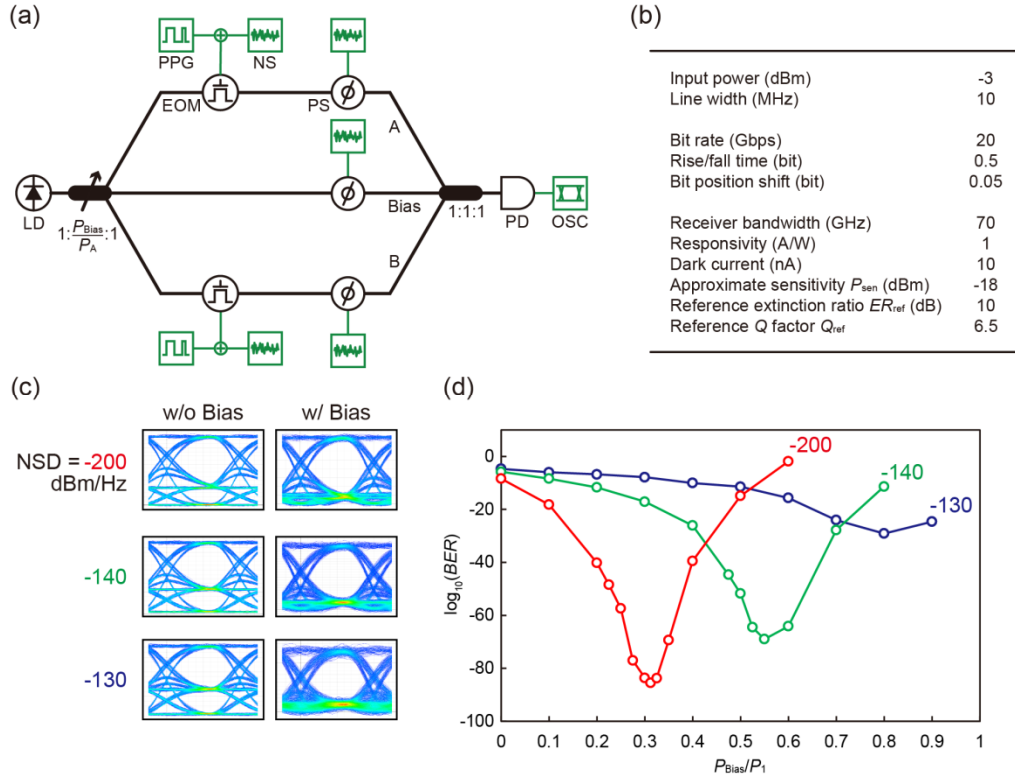
Supplementary Figure 3 | Investigation of performances for logic operations with varying the structural parameters with considering the actual fabrication resolution. (a) Schematic of a Ψ gate denoting the structural parameters. (b) One example of the simulation models without and with rounded corners around the narrower gap part. (c) W_{taper} and L_{taper} dependencies for all the performances (Required relative bias power P_{Bias}/P_1 , signal loss SL , net loss NL , and reflection R) without rounded ($W = 440$ nm). The green stars correspond to the simulated structure with $W = 440$ nm, $H = 220$ nm, $\theta = 14.0^\circ$, $L_{taper} = 900$ nm, and $W_{taper} = 105$ nm. The region painted as the black boxes correspond to the structure with boundary crossings which cannot be simulated. (d) W_{taper} and L_{taper} dependencies for all the performances with fillet process ($W = 440$ nm). The blue stars correspond to the notable structure with the almost lowest SL , NL , and R . (e) W_{taper} and L_{taper} dependencies for all the performances with fillet process ($W = 480$ nm). The red stars correspond to the designed structure for the actual fabrication.



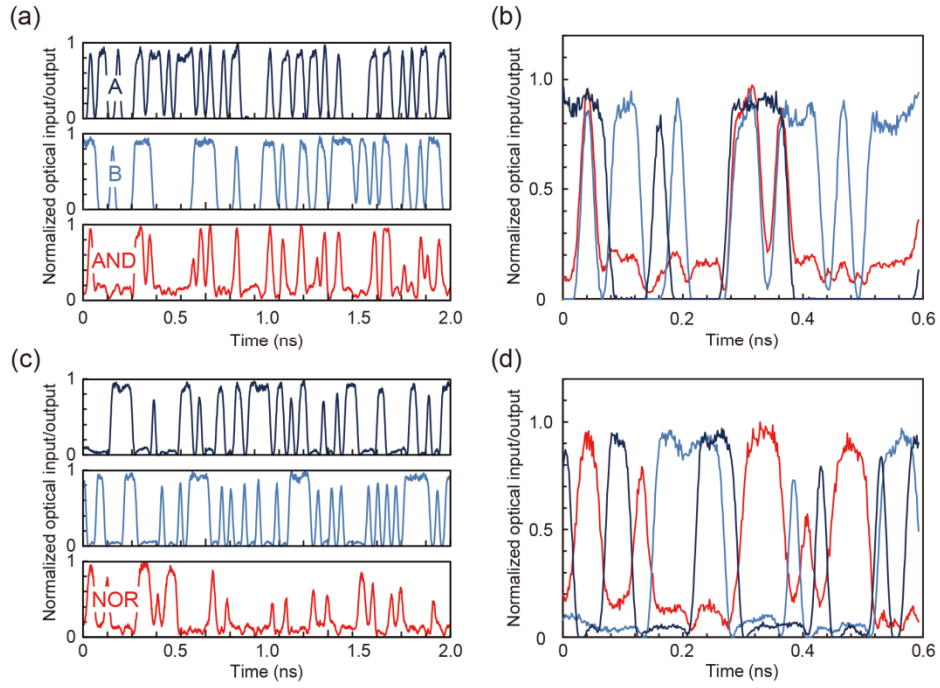
Supplementary Figure 4 | Representative simulated models. (a) – (c) Magnified images of generated models in COMSOL for individual colored stars. (d) Overlapped image of the fabricated device (scanning electron microscope (SEM) image) and the simulation model corresponding to (c) (transparent red region). L_{taper_round} and W_{taper_round} denote the actual L_{taper} and W_{taper} after the fillet process. L_{taper_fab} and W_{taper_fab} are the measured L_{taper} and W_{taper} for the fabricated sample.



Supplementary Figure 5 | Investigation of operation wavelength λ characteristics for two different Ψ gates. (a) Definition of the port numbers for S -parameters. (b) Transmission and reflection spectra for the green star structure. (c) Transmission and reflection spectra the red star structure. (d) Comparison of required relative bias power P_{Bias}/P_I and signal loss SL . (e) Comparison of the sum of the transmittances.

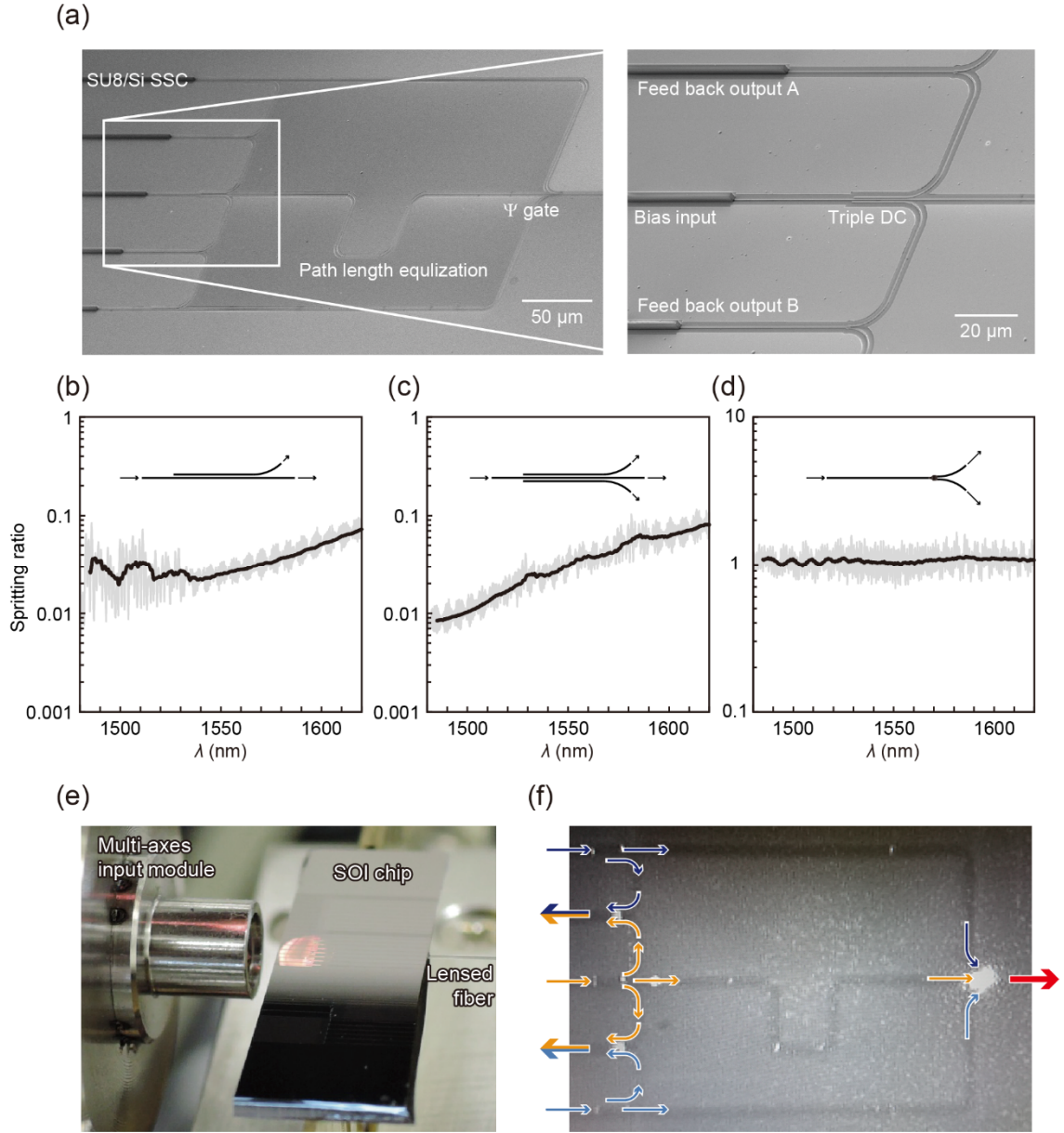


Supplementary Figure 6 | Simulation of eye diagrams for verification. (a) Block diagram for simulations (LD: laser diode, PPG: pulse pattern generator, NS: noise source, PS: phase shifter, EOM: electro-optic modulator, PD: photodiode, OSC: oscilloscope). (b) Simulation parameters. (c) Simulated eye diagrams with different conditions. (d) Simulated bit error rate BER vs. required relative bias power P_{Bias}/P_1 for three different noise spectral density NSD.

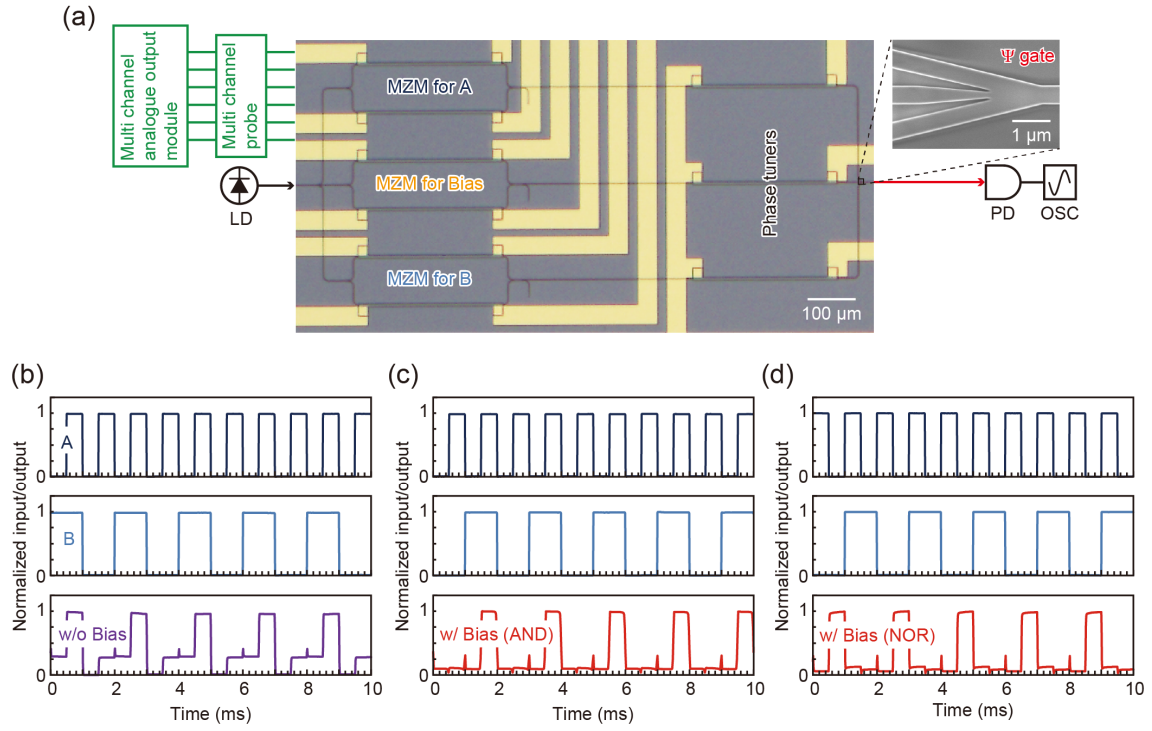


Supplementary Figure 7 | Measured time waveforms for the verification of 40 Gbps operation.

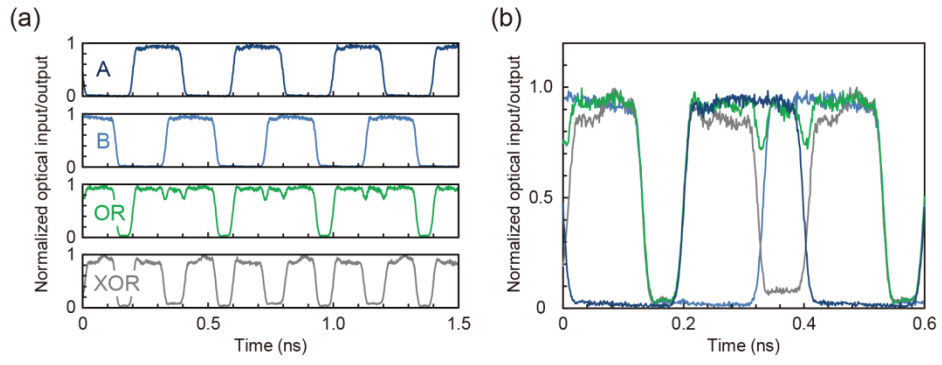
(a) Input and output of AND operation. (b) Detail comparison of AND. (c) Input and output of NOR operation. (d) Detail comparison of NOR.



Supplementary Figure 9 | Optical I/O of the silicon on insulator (SOI) chip. (a) Tilted scanning electron microscope (SEM) images around the on-chip Si wire interferometers with Y branches and a triple directional coupler (DC) and SU-8 spot size converters (SSCs). (b) – (d) Wavelength dependencies of the experimental splitting ratio of single DC, single triple DC, and single Y branch, respectively. The gray and black solid lines denote before and after moving average, respectively. The insets denote the computer-aided design (CAD) patterns with input and output directions. (e) Picture showing the optical coupling to the SOI chip with the 6-input lens module and the lensed fiber. (f) Near infrared image of the device under the test observed through an optical microscope ($\times 20$). The blue (orange) arrows indicate the flow of signals A and B (Bias).



Supplementary Figure 10 | Demonstration of AND and NOR operations with a silicon wire Ψ gate with on-chip integrated phase shifters. (a) Schematic of the measurement setup. The inset shows an optical microscope image of the fabricated circuit and a scanning electron microscope (SEM) image of the Ψ gate (LD: laser diode, MZM: Mach-Zehnder modulator, PD: photo diode, OSC: oscilloscope). (b) Time waveforms for electrical inputs and optical output without Bias. (c) Time waveforms with Bias for AND operation. (d) Time waveforms with Bias for NOR operation.



Supplementary Figure 11 | Demonstration of OR and XOR operations without Bias. (a) Time waveforms of the input and output bit patterns. (b) Detail comparison of all the waveforms.

Supplementary Note 1

Linear optical logic operations with finite extinction ratio (ER)

The input signals have some imperfection in terms of time response, power symmetricity, and ER . Here we focus on ER because the experimental input signals obviously have a finite ER ($ER = 10\log_{10}(P_I/P_0)$, $P_0 \neq 0$) and we found that it quite changes required P_{Bias}/P_I for maximizing BC . When we assume finite ER for A and B, the required P_{Bias}/P_I is easily derived as;

$$\frac{P_{Bias}}{P_I} = \frac{T_A}{4T_{Bias}} \left(1 + 3 \sqrt{\frac{P_0}{P_I}} \right)^2 \quad (\text{for AND}), \quad (S1)$$

$$\frac{P_{Bias}}{P_I} = \frac{T_A}{T_{Bias}} \left(1 + \sqrt{\frac{P_0}{P_I}} \right)^2 \quad (\text{for XNOR}), \quad (S2)$$

$$\frac{P_{Bias}}{P_I} = \frac{T_A}{4T_{Bias}} \left(3 + \sqrt{\frac{P_0}{P_I}} \right)^2 \quad (\text{for NOR}). \quad (S3)$$

Supplementary Figures 1a and 1b show required P_{Bias}/P_I relative to the signal input varying between P_I or P_0 , and signal loss SL ($= 10\log_{10}(P_{out}/P_I)$) for different operations, respectively. The experimental transmittances ($\lambda \sim 1.55 \mu\text{m}$ in Fig. 5a in the main text) are assumed for here's analysis. P_{Bias}/P_I is almost constant and similar to the ideal case while $ER > 30$ dB. When ER gets smaller and smaller, all the operations need larger P_{Bias}/P_I in order to remove the additional DC component. In other words, the maximum BC of ~ 9.5 dB can be maintained even with the degraded ER by modifying P_{Bias}/P_I . Larger P_{Bias}/P_I causes larger SL because the modulation depth between “0” and “1” states cannot be enlarged absolutely (no actual gain for “1” state because of the linearity). For AND and NOR operations, they have totally identical SL while NOR needs larger P_{Bias}/P_I . Supplementary Figures 1c and 1d respectively compare BC and SL for with and without Bias to show the effect of Bias. For the case with or without Bias, we assume a Ψ gate with $T_A = T_B = 4/9$, $T_{Bias} = 1/9$ (this condition realizes $SL = 0$ dB with a proper design as shown in the next section) or a simple Y branch ($T_A = T_B = 1/2$). When ER gets smaller, the difference of BC between with and without Bias gets larger (e.g. ~ 8 dB difference at $ER = 3$ dB). On the other hand, the difference of SL also gets larger (13 dB difference at $ER = 3$ dB). So here we want to emphasize BC can be always recovered up to the same maximum level (~ 9.5 dB) for any degraded ER with the additional SL . But, note that a simple Y branch has a negative SL (effectively gain) of -3 dB. Supplementary Figures 1e and 1f show the difference of P_{Bias}/P_I for AND operation and SL among the three different combinations of the transmittances. One of them as denoted black solid lines is set to $T_A = T_B = T_{Bias} = 1/3$ because this condition is ideal for minimizing P_{Bias} . But SL cannot be smaller than the case of $T_A = T_B = 4/9$, $T_{Bias} = 1/9$ as shown in Supplementary Fig. 1f.

Supplementary Figures 2a and 2b show one ideal simulation results with poor ER signals of 3 dB. In this simulation, the high enough input power relative to the PD's sensitivity is assumed even with additional SL with applying Bias. So the output with Bias simply shows the BC recovery effect from ~ 1.4 dB to ~ 9.5 dB with negligible noise level, which corresponds to the previous theoretical analyses. Note that in the simulation, we could only assume a Ψ gate with $T_A = T_B = T_{Bias} = 1/3$. In this case, P_{Bias}/P_I and SL are ~ 2.5 and ~ 12.8 dB, respectively. This simulated result almost corresponds to the analytical result shown in Supplementary Fig. 1f.

Supplementary Note 2

Design and comparison of Si wire Ψ gates

In terms of the actual Ψ gate design for the experimental demonstration, we define one useful figure of merit – net loss NL as following;

$$NL = 10\log_{10}\left(\frac{P_{out}}{2P_1 + P_{Bias}}\right). \quad (S4)$$

NL counts all the input power including Bias. Thus, NL is a good indicator for balancing P_{Bias}/P_1 and SL with smaller power consumption. NL is minimized down to ~ 4.4 dB with $T_A = T_B = 0.4$, $T_{Bias} = 0.2$ while $SL \sim 0.46$ dB, $P_{Bias}/P_1 = 0.5$. With including NL , we considered the design rule of our Ψ gates for AND operation as following;

1. $T_A = T_B$ (symmetric design)
2. Shorter L_{taper} for lower latency
3. $P_{Bias}/P_1 \leq 0.5$ (= smaller power consumption)
4. Smaller $SL < 2$ dB
5. Lower NL
6. Smaller signal reflectance R
7. Better fabrication tolerance (= structural insensitive)

Supplementary Figure 3a illustrates the schematic of the Ψ gate with the structural parameters again. All the devices usually get rounded because of the fabrication resolution. To consider this effect, we also simulated the model with the rounded corners to determine the parameters for computer-aided design (CAD). The round-off radius is fixed to 20 nm based on our fabrication resolution, as shown in Supplementary Figure 3b. Thus, the original structures with gaps < 40 nm are strongly deformed to the structures with shorter L_{taper} and wider W_{taper} . We have referred Ref. [1] for the refractive index of Si. Supplementary Figures 3c – 3e compare the structural dependencies for 4 performances (P_{Bias}/P_1 , SL , and NL for AND operation, and R) against three different basic structures with varying L_{taper} and W_{taper} , but fixing $H = 220$ nm, $\theta = 14^\circ$. Input λ is fixed as 1.55 μm . Supplementary Figure 3c shows the results for the optimized structure without rounding process. SL can be lower than 0 dB with narrower $W_{taper} < 100$ nm since T_A becomes very large as ~ 0.44 . In this case, due to the relationship of $T_A + T_B + T_{Bias} \leq 1$, T_{Bias} automatically becomes smaller than 0.1. As the result, P_{Bias}/P_1 becomes larger than 1. To balance both SL and P_{Bias}/P_1 , the design pointed by the green stars has been employed as our conceptual design shown in Figs. 2c and 2d of the main text, and Supplementary Fig. 4a because of the reasonable P_{Bias} (~ 0.45), lower SL (~ 0.63 dB), almost the lowest NL (~ 4.5 dB) and quite lower R ($< 0.1\%$) with the shortest L_{taper} (0.9 μm), which is satisfying almost all the above criteria except for the fabrication tolerance. Supplementary Figure 3d shows the result with the rounded corners otherwise same as Supplementary Fig. 3c. First of all, almost all the performances related to the losses are degraded, but P_{Bias}/P_1 and the fabrication tolerance become

better. Because of the gap size widening, SL and NL are degraded with R increase. But still the structure marked by the blue star has almost the lowest SL (~ 1.0 dB) and NL (~ 5.3 dB) with lower R ($\sim 0.52\%$). This structure is also valuable, but P_{Bias}/P_I becomes a bit higher (~ 0.68) than our criteria. R also shows some structural sensitive behavior against W_{taper} . Next we try to find the structure with better fabrication tolerance with smaller P_{Bias}/P_I . Supplementary Figure 3e shows the result with wider W (480 nm). In general, wider W decreases P_{Bias}/P_I , SL , and R with keeping similar NL with Supplementary Fig. 3d. R for narrower W_{taper} structure gets reduced with the better fabrication tolerance. The structure marked as the red stars has well balanced performances ($P_{Bias}/P_I \sim 0.38$, $SL \sim 1.5$ dB, $NL \sim 5.3$ dB, $R \sim 1.2\%$) with the better fabrication tolerance. So we adopted this red star one for the actual CAD design.

Supplementary Figure 4 compares the fabricated device and the simulated model with the rounded corners. The simulation model closely overlaps to the fabricated sample. So the fabrication has been completed successfully.

We also simulated λ dependencies for the structures corresponding to the green and red stars marked in Supplementary Figs. 3 and 4. Supplementary Figure 5a defines the port numbers to identify the series of S -parameters (“1”, “2”, “3” and “4” correspond to A, B, Bias, and Output, respectively). Supplementary Figures 5b and 5c are the simulated transmission and reflection spectra for 8 combinations of the input and output ports (from A to all the ports, and from Bias to all the ports). So there are extra 5 reflection spectra more than Fig. 2c of the main text. The green star one has almost flat spectra for T_A and T_{Bias} . In terms of the reflection, only $|S_{11}|^2$ (R) and $|S_{33}|^2$ seems to be dominant. Actually the red one has a bit larger $|S_{33}|^2$ of $> 4\%$ for the longer λ side ($> 1.57 \mu\text{m}$). Supplementary Figure 5d compares P_{Bias}/P_I and SL for the three structures. Thanks to the high T_A , the green one has twice smaller SL than the red one, but P_{Bias}/P_I is almost comparable. Supplementary Figure 5e compares the sum of the three transmittances to the port 4 ($T_A + T_B + T_{Bias} = |S_{41}|^2 + |S_{42}|^2 + |S_{43}|^2 \leq 1$) to clarify the excess radiation losses. The green one shows $0.97 - 0.98$, which means there is almost no excess radiation loss compared to the red one. We may need more structural optimization to find the lower loss one even with the finite fabrication resolution with utilizing some algorithms [2] or machine learning [3, 4].

Supplementary Note 3

Simulation for eye diagrams of AND operation

We have used the commercial software (OptiSystem, Optiwave Systems) to simulate all the eye diagrams. Supplementary Figure 6a illustrates the block diagram of the simulation. As same as the experimental setup, we separated the coherent light from one laser diode (LD) source into A, B and Bias. We applied independent white noise sources (NS) for all the pulse pattern generators (PPGs) connected to electro-optic modulators (EOMs) and the phase shifters (PSs) with the phase variation within $\pm\pi$ for the implementation of the mechanical vibration of the fiber optics. For Bias, the relative phase $\Delta\Phi_{Bias} = \pi$ was set. The combining ratio of the Ψ gate is 1:1:1 (i.e. $T_A = T_B = T_{Bias} = 1/3$), which is technically limited in OptiSystem. Finally the optical output was converted to the electrical signal through a photodiode (PD) whose performances are similar to the experimentally used PD. Finally, the eye diagrams were visualized with an oscilloscope (OSC). Supplementary Figure 6b summarizes the simulation parameters. Approximate sensitivity P_{sen} , reference extinction ratio ER_{ref} , and reference Q factor Q_{ref} are defined for the determination of the power level of P_I and P_0 , and the associated shot noise and thermal noise RMS currents [5]. Supplementary Figure 6c presents the observed eye diagrams under the different noise spectral density (NSD). We also compare the eye diagrams without and with Bias. Note that the total input power is always fixed to -3 dBm between without and with Bias. Thus, the total power consumption of the operations are always same. NSD = -200 dBm/Hz actually corresponds to the case of almost noise-less environment. NSD = -130 and -140 dBm/Hz are comparable to the experimental PPG. Even with noise-less electrical drive signal, a bit larger P_{Bias}/P_I of ~ 0.3 was required than the ideal case of 0.25. This indicates ER degradation by relatively slow rise/fall time ($= 0.5$ bit). For any NSD cases, BC can be maximized with calibrating P_{Bias}/P_I . Supplementary Figure 6d shows the bit error rate BER vs. P_{Bias}/P_I for the different NSD. In this BER calculation, the signal dispersions σ_I and σ_0 against the binary intensity levels of P_I and P_0 are estimated by using a Gaussian fitting to the histograms of the signal distribution at the center of the simulated eye diagrams. σ_0 is estimated from the distribution below the P_I level, and so it is obvious that σ_0 becomes much larger with a certain P_{Bias}/P_I . Minimum BER gets smaller when NSD is smaller. According to the results, BC recovery should be achieved even with larger NSD with larger P_{Bias} .

Supplementary Note 4

AND and NOR operations with 40 Gbps pseudo random bit sequence (PRBS)

Supplementary Figure 7 summarizes the results for AND and NOR operations with 40 Gbps PRBS (2^9-1). Both of operations seem to work with some degradation because of the finite rise/fall time of the input signals (~ 30 ps).

Supplementary Note 5

Measurement setup including 2-channel optical phase lock loops (OPLLs)

Supplementary Figure 8 depicts the detail of our setup. As explained in the main text, we have several off-chip optical components connected with a bunch of fiber patch cords. Therefore, the relative phases of input signals always suffer from the phase fluctuations due to the mechanical vibrations. To cancel this fluctuation, we utilized fiber stretchers (PZ1-PM1-APC-E-155P, Optiphase) controlled by a digital laser stabilizer (LaseLock, TEM Messtechnik). Actually one LaseLock has a lock-in amplifier with 2-channel independent PID regulators whose sampling rate is up to 2.5 MS/s. All necessary electrical digital functions such as a dithering oscillator, filters, amplifiers etc. are promptly performed within the field-programmable gate array (FPGA) in LaseLock. For better understanding, we depict the fundamental electrical components in Supplementary Fig. 8.

The output power of the tunable laser diode (LD) was set to 8 dBm for all the experiments. First the laser light was split into two by a tunable coupler. For generating arbitral optical bit patterns, an optical transmitter connected to a pulse pattern generator (PPG) with a radio-frequency (RF) signal multiplexer (MUX) was used. The generated optical bit patterns were separated into two by a 3dB coupler. After the intensity tuning with a multi-channel variable optical attenuator (VOA), the two signals were separated into A and B by shifting the bit pattern with a fiber delay line (DL). The signals went through the piezo-driven fiber stretchers (PZT FS) controlled by the OPLL system. All the input and output lights were coupled to the silicon-on-insulator (SOI) chip by using a lens module and a lensed fiber as shown in Supplementary Fig. 9c. The output light was amplified by an erbium doped fiber amplifier (EDFA). After removing the amplified spontaneous emission noise by using an optical bandpass filter (BPF), the output bit patterns were observed by optical sampling oscilloscope (OSC) whose bandwidth is 70 GHz.

In terms of the OPLLs, we set Bias channel as the phase standard. The phase of Bias was weakly modulated by the fiber-input phase modulator (PS) with 200 kHz. The modulation sinusoidal wave was generated by a function generator (FG) which synchronized to the dithering signal (rectangular waveform) of the LaseLock. For the OE converters (PD), we had to choose a proper load resistance to avoid the output saturation. The converted electrical signal was input to LaseLock, and electrically amplified again. After the DC block, the interference signal and the dithering signal were input to a mixer. From the mixer's output, the phase error signal was obtained by extracting the DC component with a low-pass filter (LPF). The error signal was input to a PID regulator. The PID output was input to the high voltage amplifier (HV amp) for driving the fiber stretcher.

For setting the PID parameters in LaseLock, we started from the proportional (P) gain. By gradually

increasing the P gains for both channels. At some point, the error signal became smaller and converged, but it was still off from the zero level. To cancel this constant error, we applied integral (I) gains slightly. In the most of cases, the phase fluctuation was suppressed enough after adjusting the I gains. And usually the differential (D) gain is not necessary for our case. For controlling the relative phase relationships, we utilized the internal functions of “Sign” and “Set point” in LaseLock. For “Sign”, we can flip the sign of the feedback output anyways (the combination of “Sign” need to be selected appropriately, *e.g.* we chose both “negative” for AND/XNOR/NOR operations, but “positive” and “negative” for XOR operation in Supplementary Fig. 11). For “Set point”, we can add a specified offset to slightly modify the relative phase. However, the phase lock stability could be pretty worse when we applied too much offset.

Supplementary Note 6

On-chip interferometers for phase error detection

Supplementary Figure 9 shows the detail of our optical I/O system. For operating a single Ψ gate with the off-chip optical transmitter, two couples of on-chip interferometers between A and Bias, and B and Bias are necessary as shown in Supplementary Fig. 8. For the signal splitting and combining, we employed two kinds of directional couplers (DCs) and an optimized Y branch for telecom regime [6]. We applied the path length equalization for Bias port for better wavelength-insensitive operation. Supplementary Figures 9b – 9d summarizes the experimental splitting ratio of these devices. The coupling length and the waveguide gap of all DCs were designed as 20 μm and 0.4 μm , respectively. The splitting ratio varies in the range of 0.01 – 0.1 (the output from the cross port was much smaller than the bar port). This ratio is sufficient for the phase error detection whose bandwidth of the fluctuation is ~ 1 kHz. On the other hand, the splitting ratio of Y branch is wavelength-insensitive. In terms of the optical coupling, we utilized a lens module (6 channels with 50 μm spacing) for the input side, and a lensed fiber for the output side as shown in Supplementary Fig. 9e. Supplementary Figure 9f shows the near infrared picture during the measurement. The stronger light scattering can be seen around the Ψ gate. This indicates the radiation loss whose degree is determined by the relative phases of inputs.

Supplementary Note 7

On-chip integrated linear optical logic circuit

In the application, it is more practical to monolithically integrate electro-optic modulators with these linear optical gate circuits, which maximize the merit of Si-photonics interferometric circuits. To demonstrate its feasibility, we have fabricated a Si Ψ gate with on-chip integrated thermo-optic phase shifters as shown in Supplementary Fig. 10a. The device with on-chip integrated phase shifters has been fabricated with using almost same procedures as mentioned in Methods of the main text. After forming Si wire waveguides, 1.5 μm thick SiO_2 cladding layer was deposited. Next, lift-off processes were performed for Ta heaters, Au/Cr electric pads and wires. The length of each heater is 300 μm . The fabricated optical logic circuit has two Ψ gates for the splitter and the combiner. For each arm, a pair consisting of a Mach-Zehnder modulator (MZM) and a phase tuner is inserted to condition the signal A, B and Bias. To independently control multiple heaters, a multiple channel probe (Multi $|Z|$ probe, Form Factor) was touched onto all the channel of pads instead of performing wire bonding processes. The probe was connected to a 32 channels analog output module (NI PXIe-6738, National Instruments) via a panel mounting template (SCB-68A, National Instruments). After conditioning all the 9 heaters, each MZM was operated with twice different frequencies (2 kbps and 1 kbps). The output was detected by a PD (XPDV3120, Finisar) and directly observed the signal with a mixed signal oscilloscope (MSO6104A, Agilent Technologies). After calibrating all the heaters, MZM A and B were modulated with two different frequencies (2 kbps and 1 kbps, respectively). The output was observed with different Bias power conditions as shown in Supplementary Figs. 10b – 10d. Nearly ideal AND and NOR operations with a BC of ~ 9.5 dB have been demonstrated without any optical phase lock loops. In the near future, all the phase shifters would be replaced by other shorter (10 – 50 μm) and faster (40 – 100 GHz) phase shifters [7, 8] to realize much higher throughput as well. The proposed linear gates themselves never are the bottleneck for the performances of the optical computation circuits.

Supplementary Note 8

Other logic operations without Bias

The experimental results are shown in Supplementary Fig. 11. So both OR and XOR were also demonstrated with 10 Gbps. *BC* of both operations are estimated $\sim 10 - 20$ dB. Note that we still needed to apply small Bias ($\sim 1/10$ of AND operations) for the optical phase lock between A and B. *BC* of both operations can be infinite ideally, but this could be degraded because of this weak Bias input.

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