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Supplementary Information: Historical Developments

Introduction

Segmented silicon detectors have become as important to particle physics for measuring the passage of charged particles as they have in astronomy for the detection of light. In parallel, there have been huge developments in commercial systems, with a global market for digital cameras in smartphones, and so on, approaching $15 billion. Since the early beginnings for silicon detectors for particle physics roughly 40 years ago, the size of the detector systems has grown from a few thousand channels and a few cm^2 to systems of 10 billion channels and areas of hundreds of m^2 (see Figure 3 in the main document). Demands in terms of radiation hardness have also grown from levels of tens of Gy (total ionising dose) and particle fluences of a few $10^{10}cm^{-2}$ up to future requirements in the ten MGy and $10^{16}cm^{-2}$ range and even well beyond these values at possible future colliders. For the electronics, services, mechanics and cooling the problems have not only been to cope with these large increases in channel count, detector areas and radiation environment but to also provide several orders of magnitude increases in front-end read-out speed to cope with many billions of interactions per second event rates, along with the corresponding required complexity of on-detector data handling, data storage, data processing and off-detector transmission.

The use of such detectors has become ubiquitous across a large range of particle, astro-particle, nuclear and medical physics experiments. The importance of the development of this technology was recognised in the award of the 2017 High Energy and Particle Physics Prize of the European Physical Society to Erik Heijne, Robert Klanner and Gerhard Lutz, three highly distinguished leaders in this field, "*for their pioneering contributions to the development of silicon microstrip detectors that revolutionised high-precision tracking and vertexing in high energy physics experiments*". This overview covers some of the history and recent developments in this vast field, with references to many key contributions as well as other review articles and books that cover many topics in much greater depth than is possible here.

The trends in silicon detector development over last four decades discussed above have only been possible thanks to the remarkable, exponential growth in semiconductor technologies since the invention of the first semiconductor transistor in 1947, for which John Bardeen, Walter Brattain and William Shockley received the 1956 Nobel Prize in physics. This exponential development is often expressed in various versions of what is known as Moore's law [1] which extrapolates the number of transistors on an integrated circuit to roughly double every two years, with many other related quantities also projected to follow a similar trend. This growth has been achieved in large part through miniaturisation, as the smallest feature sizes that can be mass produced using lithographic

techniques continue to shrink towards atomic scales. Although the increasing importance of quantum effects must ultimately limit the scope for further reduction in component dimensions, the technologies relevant to particle physics follow some way behind the leading edge in this regard and so may expect to benefit from the corresponding expected cost and performance improvements for quite some time to come. In practice, for many silicon devices in particle physics, the more important cost driver has been the huge increase in the market for silicon devices which has driven down equipment and materials costs and greatly improved automation for device processing and characterisation.

1. The First Vertex Detector Arrays

Early applications [2], [3] had focussed on 'fixed target' experiments primarily searching for production of hadrons with the recently discovered charm quantum number, for which tracks of interest through the detector do tend to pass close to normal incidence. However, the silicon detectors for early collider experiments ($S\bar{p}pS$, SLC, LEP) needed to provide greater angular coverage (see, for example, [4], [5], [6], [7], [8], [9], [10]) usually in the presence of an intense magnetic field. In the case where the strips are used only to measure the ϕ (azimuth) coordinate -- assuming a spherical polar coordinate system (r, θ, ϕ) with z-axis along the collision axis in the experiment -- the ϕ measurement typically defines measurement in the bending plane due to the magnetic field along the z-direction. For high transverse momentum (p_T) tracks, the tracks through a cylindrical array of detectors will pass through detectors at close to 90° in the r-ϕ projection, but low p_T tracks will be more inclined towards the detector surface and so can still cross below many strips within the sensitive volume of the detector, giving signal on many channels.

An early example with segmentation in two dimensions was the highly innovative CCD based SLD vertex detector (with first a 120 Mpixel and then a 307 Mpixel array [7]) which got round the problem of large θ (polar) angles firing many pixels by having a sensitive thickness similar to the electrode pitch, introducing the idea of a 'voxel' measuring a tiny volume in 3 dimensions associated to every hit in the silicon detector. However, the then available CCD frame-rate did not lend this approach to other collider environments although this approach probably helped inspire later 'monolithic' silicon pixel detector designs.

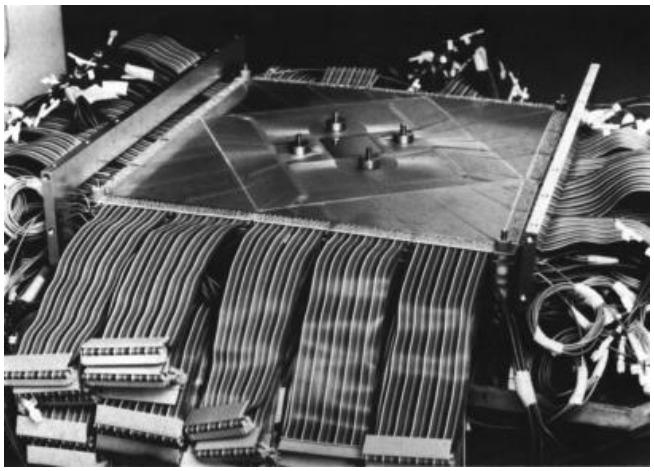

Figure 1 NA14 Detector Stack. Each plane has a single-sided 1000 strip 5cm×5cm silicon detector at its centre. Reproduced from Ref. [2]

The main early developments were in planar strip detector designs using variants of the technologies outlined in the Detectors Technology. The challenge for any collider experiment is that there has to be multiplexing of the channels onto a small number of read-out lines, as it is physically impossible

to connect every strip to the outside world in the way that was done for the early fixed target experiments (see Figure 1). The key development to cope with the large number of channels in a strip detector was the development of microelectronics amplifying and multiplexing silicon ASICs that could be connected directly to the read-out strips [11]. Several different variants of such 'microplex' chips were developed for the different experiments (see [12], [13], [14], [15], [16]), with typically 128 channels per readout chip, either directly wire-bonded to the strips of the detector or via a glass adaptor or possibly through an AC decoupling chip (see Detector Technologies). The ASICs were typically mounted on a ceramic printed circuit support board ('hybrid') such that an entire sensor (or set of sensors wire-bonded together to make a ladder of detectors) could be read out down a single ribbon cable. Figure 2 (a) shows such a ladder and how an array of these was mounted around the vacuum pipe of the accelerator within which the particle collisions took place [9]. These arrays were used to both tag the presence of and measure the properties of hadrons containing *b* and *c* quarks, as well as τ-leptons, all having lifetimes in the picosecond range. References [17] and [18] contain many useful equations on the resolutions achievable with such tracking detectors, including the ability to separate secondary vertices (due to decays of short-lived particles) from the primary vertex (the point where the beam particle collision has taken place). Some of these are discussed in the box which shows that for low momentum tracks it can be more important to reduce the tracker material than to improve the detector spatial resolution.

As an example, extrapolation of charged particle tracks back to the locations within the vacuum pipe where they were produced for an N layer vertex detector is achieved for orthogonal tracks with resolution, $\sigma_{d_0} = \frac{\sigma_{point}}{\sqrt{N}} \sqrt{1 + \frac{12(N-1)}{(N+1)} \left(\frac{r}{L}\right)^2} \oplus \theta_0 r_{pv} \sqrt{\frac{N(2N-1)}{6(N-1)^2}}$ with $\theta_0 = \frac{13.6\text{MeV}/c}{\beta p} \sqrt{x/X_0}$ [18]. The first term depends on the silicon sensor spatial resolution, σ_{point}, and the ratio of the track extrapolation distance, r, to the length through the tracker, L. The second term, added in quadrature, comes from the track multiple Coulomb scattering in the tracker material (with thickness, x, and radiation length, X_0) which decreases as $1/p$ with momentum, p, ($\beta = v/c$ the ratio of particle speed to that of light) and also depends on the distance from the vertex to the first tracker layer r_{pv}. Depending on geometry, the first term can be as low as 10μm with the second more typically $100\mu\text{m} \times 1/p$ with p in units of GeV/*c.* It can be seen from this that up to momenta of around 10 GeV/c, tracker material can matter more than spatial resolution, σ_{point}.

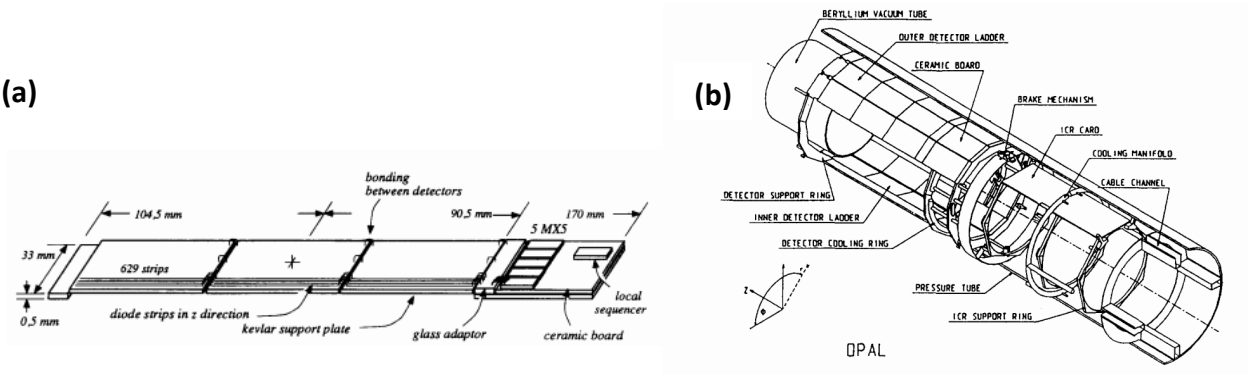

Figure 2 (a) OPAL Silicon Micro-strip Ladder with MX5 Read-out Chips and (b) the 25 Ladder Microvertex Array. Both panels are reproduced from Ref. [9]

In addition, as mentioned in the main article, 2D read-out could also be achieved with double-sided detectors. For sparse environments, the ambiguities inherent in having two projections rather than a truly pixelated sensor can be resolved and the read-out of all signals from 2N strips typically is much quicker than reading out all of the corresponding N^2 pixels for the same x-y segmentation. The major advantage in measuring the tracks in two projections and reconstructing 3-dimensional primary and secondary vertex locations does come at the price of increased number of channels and that, for detectors at large polar angle, θ, the signal can be spread over many strips. Most vertex detectors employed electronics with analogue readout (meaning that the multiplexed signal from the readout provided pulse-height information) and a typical signal/noise of 15-20 defined in terms of the a most probable signal of 22.5ke$^-$ for a minimum ionising particle traversing 300μm of silicon. The noise depends on the ASIC design and the capacitive load due to the strips seen by the input of the amplifier circuit (see Detector Technologies) With adequate signal/noise, not only can even highly angled tracks with signal spread over many channels be detected with good efficiency, but the profile at the start and finish of the long cluster of hit channels can be used to interpolate the entry and exit point of the track in the sensitive silicon. Furthermore, the large variability (a Landau distribution [19] as illustrated in Figure 3(a)) of the deposited charge means that in double-sided measurements (where for a given track the same number of electrons and holes are generated) any ambiguities as to which hit strip cluster on one side goes with which on the other side could be mitigated by comparing the total deposited charge in the corresponding clusters, as long as the noise is a small fraction of the signal. Finally, signal/noise is important to improved precision in interpolating hit positon from pulse heights on neighbouring strips. With the signal/noise performance shown in Figure 3 for the detector described in Figure 2, a read-out pitch of 50μm (strip pitch 25μm) resulted in a spatial resolution, σ_{point}, of 6μm giving an extrapolated high momentum track precision at the collision vertex, σ_{d_0}, of 18μm.

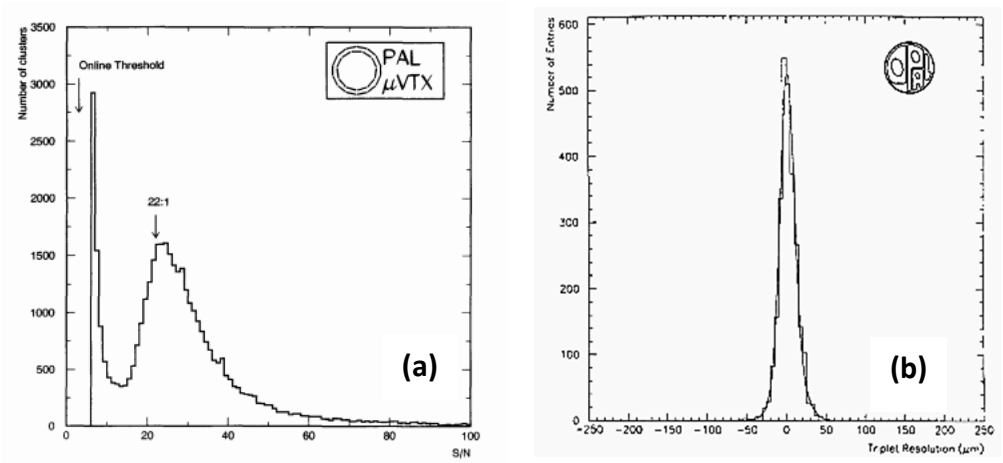

Figure 3 (a) Signal in Units of Electronics Noise and (b) Spatial Resolution of a LEP Vertex Detector. Both panels are reproduced from Ref. [9]

Although microplex chips made it possible to have a very large number of channels in small volume detectors buried at the heart of very large particle physics experiments, optimised physics performance required continuously reducing the material in the vertex detector arrays. The first double-sided detector had the read-out chips for the orthogonal strips, measuring the z-coordinate along the silicon ladder, distributed down the length of the ladder [20], adding silicon and services material in the sensitive volume of the detector. An alternative was to incorporate a second layer of bussing strips on top of the z-measuring strips to route the signals from these to the end of the ladder [21, 22] outside the sensitive volume. Given the shape of the ladder, the far larger number of strips in the z-coordinate, means multiple strips have to connect to the same electronics channel if the ladders have the same number of chips for the r-ϕ as the z read-out. However, the daisy chaining of sensors together does not have to be z-side to z-side or rϕ-side to rϕ-side. Given the opposite signal for hole and electron collecting sides, the DELPHI Microvertex Detector used the signal polarity in such a "flipped module" concept to determine which sensor in the ladder was hit, thus greatly reducing ambiguities [21].

2. From Vertexing to Tracking and Beyond

The evolution of strip detectors continued at CERN for LEP and at many other laboratories with different optimisations, either to reduce material for dedicated experiments with relatively low energy collisions optimised to study short-lived particles (CLEO [23], BaBar [24], Belle [25]) or for other energy frontier facilities at DESY (H1 [26], ZEUS [27]) and the Tevatron (CDF [28] [29], [30] [31], D0 [32]). The largest silicon array in the 20th century, encountering some of the most demanding specifications in terms of speed and radiation, was that for the CDF experiment [17] which also saw silicon strips become a tracking as well as vertex finding technology. As will be discussed below, this was a significant intermediate step from the first e^+e^- vertex detectors to the huge silicon tracking arrays of the ATLAS [33] and CMS [34] experiments at the LHC.

As hit densities become sufficiently high, resolving the 2D hit position in the silicon plane from the projections provided by strip systems becomes progressively more difficult as the ambiguities grow. Up to some point, extrapolation from other tracking systems can help correctly associate the right pairs of crossed strips to the hit location in the silicon plane, but within jets or close to the beam axis (particularly in fixed target experiments) strips become less effective. Pixelated detectors are much better, but harder to read out quickly (see Detector Technologies). The first applications used CCD based detectors (which had only been invented a decade earlier at Bell Labs [35]) initially for the fixed target NA32 experiment [36] and then for the e^+e^- SLD experiment [7]. However, the problems

of slow CCD frame-rate necessitated the development of hybrid detectors with planar silicon sensors as above, but segmented into pixels not strips. The challenge for such detectors was primarily in the design of the very high density micro-electronics, but also in adapting for particle physics specifications the 'flip-chip' interconnect technology to mount the read-out chips on the sensors as illustrated in Figure 4. Again the first application was for a fixed target experiment, WA97, [37] and then to cover the forward regions of the DELPHI Microvertex Detector [38]. As strip detectors at hadron colliders evolved to provide large area tracking arrays [39], the problems of multiple collisions per beam crossing and the high track densities close to the vertices of the LHC general purpose detectors necessitated the development of large array hybrid pixel solutions for both ATLAS [40] and CMS [41].

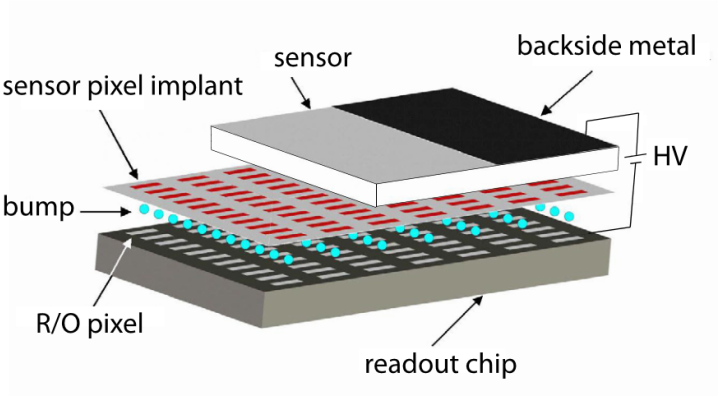

Figure 4 Principle of the Hybrid Pixel Detector. Reproduced from Ref. [18]

Outside the LHC developments, plans for future e^+e^- linear colliders (see Linear Collider Collaboration at [42]) at energies far surpassing those of LEP2 [43] were inspiring development of a new generation of ultra-precise, very low mass pixelated vertex detectors. The time structure of the interactions, with trains of many closely spaced bunches colliding followed by relatively long periods between bunch trains, lends itself to novel read-out and powering strategies. The physics goals of experiments at such colliders depend critically on the best possible vertex measurement capability so both the pixel size and layer thickness (in radiation lengths) must be minimised. Although thinned hybrid solutions can meet the requirements (and allow sensor and electronics to be separately optimised), many proposed solutions require monolithic solutions, either as developments of the SLD style CCD approach, taking advantage of mass production technologies that for commercial applications are largely replacing CCDs (CMOS Imaging Sensors, CIS [44]) or with completely new bespoke detector solutions. LC inspired technologies have recently found application in both lower energy e^+e^- experiments (for example DepFETs for Belle-II [45]) and heavy ion colliders MAPS for STAR at RHIC [46] and ALICE and the LHC [47]).

3. Current and Future Trends

Figure 3 in the main document (after [48] and [17]) shows not only the increase in the number of channels in silicon trackers with time but also the surface areas. Future projects are also shown where the dates for ILC and FCC are clearly tentative. While the growth in the number of channels which can be afforded benefits directly from Moore's Law [1], the exponential growth in the area of detectors is more surprising. The pressures in the microelectronics industry tend to push down the

cost per transistor not the cost per silicon wafer. The move towards CIS technologies and monolithic designs is assumed to bring the benefits of working with much larger throughput suppliers than those who have mastered the niche market of hybrid sensors. However, the hybrid sensor market is also expected to grow as the demands of extreme radiation hardness and ultra-fast timing capabilities will for a long time remain only achievable in separately optimised sensor and microelectronics chips.

Association of tracks to the correct bunch crossing often requires excellent timing capabilities. The fixed target NA62 'Gigatracker' pixel array read-out, for example, is able to achieve a 200ps time stamp resolution [18], [49]. The bunch separation time at the proposed CERN Compact Linear Collider (CLIC) [50] of only 500ps represents a severe constraint in terms of required read-out capabilities for the tracking and vertexing detectors. With 200 superimposed primary interactions in every 25ns beam crossing at HL-LHC [51] and possibly as high as 1000 at the proposed Future Circular Collider, FCC [52], timing information becomes an important additional tool in association of tracks to the correct primary vertex within a given beam-crossing. However, new silicon detector technologies are needed to achieve the few tens of ps timing resolution needed to help resolve which tracks belong to which primary vertex as discussed in the main document.

It is worth noting that the broad scientific and commercial applications of silicon for photon detection (where the digital camera market alone is estimated to be worth ~10B€) often lead to developments (such as CCDs in the 80s and CIS technologies today) that feed back into tracking detector technologies. Many important developments such as avalanche photodiodes (APDs) and silicon photomultipliers (SiPM) (see, for example, [19]) have helped revolutionise photon detectors for particle physics and many other applications, but these lie largely outside the scope of this article.

Often groups developing silicon tracking detectors are also involved in other application areas (astronomy, space science, nuclear or medical physics) and may be developing applications (such as x-ray detectors for synchrotron and free electron laser (FEL) light sources) in parallel to work for particle physics (gaining benefit from the synergies between application areas and multiple funding streams). Finally, the developments in other related technologies, Ge, GaAs, GaN, CdTe, CdZnTe, diamond, as well as more exotic semiconductors are not considered in this review although all have found important niche applications. The overview by the Particle Data Group at [53] is a highly recommended resource and also contains many useful pointers to reviews or books which provide further reading on the much broader range of detector technologies in use for accelerator based experiments.

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Supplementary Information: Detector Technologies

1. Passive Sensors

As Figure 1 in the main document illustrates the effect of reverse bias is to increase the barrier height and lead to an increased width of the SCR. In this condition (from the boundary conditions in solving Poisson's equation in one dimension for an abrupt junction) the field at the junction and the depleted region (SCR) thickness, d, both increase with a square root dependence on the applied voltage, V [1], [2]. If it is assumed that, in thermal equilibrium at room temperature, all the donor atoms are ionised and acceptor levels are filled, $d(V) = \sqrt{\frac{2\varepsilon_r\varepsilon_0(N_A+N_D)}{qN_AN_D}(V - V_{bi})}$ where V_{bi} is the small built in potential difference with no applied voltage, V; N_A, N_D are the acceptor and donor doping concentrations by volume in each region and q is the fundamental unit of charge. Note in most detectors discussed below, either $N_A \gg N_D$ or $N_D \gg N_A$, simplifying this equation further for an abrupt one sided junction to having *d* only depend on the doping concentration on the low doped side. For any detector where

the electrode dimensions are much greater than the thickness, the simple formula, $C(V) = \varepsilon_0 \varepsilon_{r_{Si}} A / d(V)$ holds [1], giving the capacitance per unit area, A, varying as $1/C^2 \propto V$.

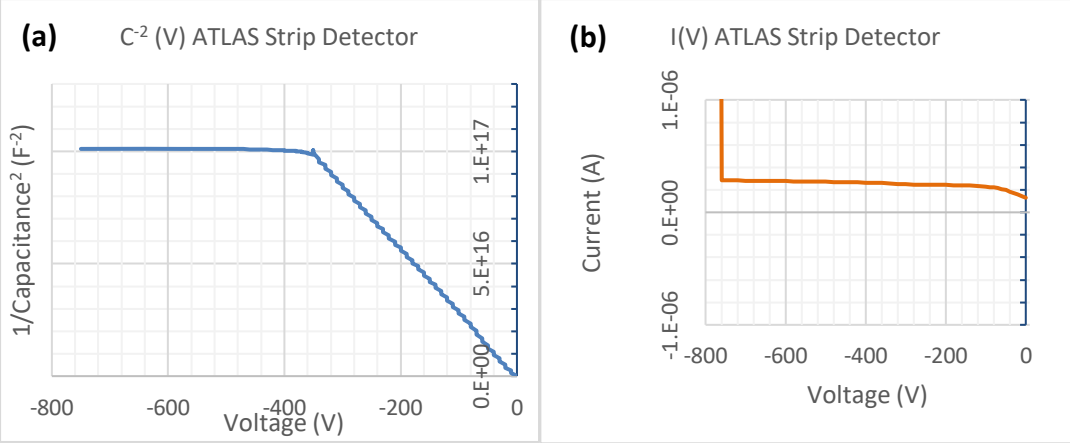

Figure 1 $1/C^2$ and current vs voltage for a 97.54mm×97.54mm area, 320±15µm thick HL-LHC n-in-p Strip Detector

Figure 1 illustrates this relationship in practice, where for this detector the highly doped implanted strips are *n*-type and the substrate very lightly doped *p*-type. The corresponding current vs voltage for this detector is also shown. The slope of the linear part of $C^{-2}(V)$ can then be used to derive N_A and hence substrate resistivity $\left(= 1/q\mu_h N_A\right)$ with hole mobility, μ_h, for this device (given that $V \gg V_{bi}$) using $\left(\frac{\partial\left(1/C^2\right)}{\partial V} = \frac{2}{qN_A\varepsilon_0\varepsilon_{r_{Si}}}\right)$. The voltage at which the device is depleted can be used either to confirm the value of N_A, assuming the device thickness is known, or to determine the sensitive thickness of the device. Identical arguments apply where instead the device has highly doped p^+ implants in a lightly doped n^- substrate. For a device of the thickness shown in Figure 1, once full depletion is achieved, a minimum ionising particle (MIP) traversing the detector will give a most probable signal value of around 3.7fC (or 23ke$^-$).

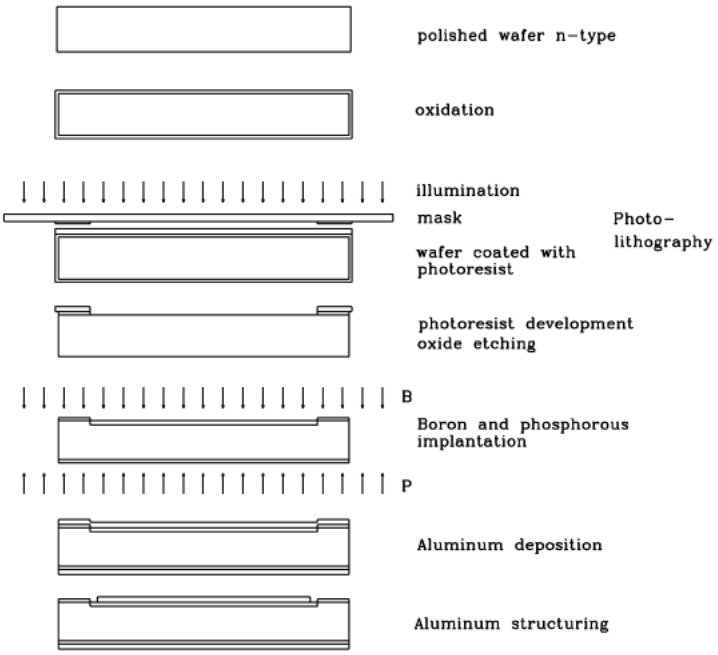

Figure 2 Simplified production sequence for p-in-in detectors. Figure reproduced from Ref. [3]

The first detectors [3], [4], [5] were of the p-in-n type, produced according to the steps shown in Figure 2 which allows patterned highly doped *p* implants with metal (aluminium) contacts on one side and an Ohmic contact (unpatterned highly doped *n* implant with metallisation) on the back side. The aluminium contacts allow the detector implants to be electrically connected. In the case of strip detectors, aluminium wire-bonding allow the strips to be coupled directly to the front-end microelectronics application specific integrated circuits (ASICs). For single-sided detectors, the large area back-surface is typically attached with wire-bonds or conductive glue to pads providing the high-voltage supply. (Note, alternative technologies to implantation were also explored in the early days of strip developments [6] but are not discussed further here.)

The position resolution is primarily set by the segmentation of the patterned implants [7], while the signal size (and hence efficiency) depends on the thickness, assuming sufficient voltage can be applied to deplete the full substrate. However, for a system with analogue read-out (such that the signal size is recorded rather than it simply needing to exceed a pre-set threshold) the resolution can be improved by interpolating the position. This is achieved through using the (non-linear) dependence of the relative signal size seen from neighbouring electrodes on the position of the deposited charge between the electrodes (as explained, for example, in [8], [3] and [9]). Intermediate implants, not connected to the readout, can also be used to enhance the linearity of the charge division with position [10]. Another feature, illustrated in Figure 3, is that spatial resolution, for a pitch much smaller than the silicon thickness, will depend critically on the angle of the incident particle.

In practice, while p-in-n detectors were the first to be fabricated, a number of more recent designs for high radiation environments chose n-in-p designs for reasons linked with radiation effects discussed in Section 1.4. In comparing the two configurations (*p*-strips in *n*-substrate or vice versa) the space between the implant strips becomes important. Most importantly, the Si-SiO_2 interface traps positive charge which for the p-in-n configuration aids the inter-strip isolation while for n-in-p the same charge leads to band-bending and an inversion region (see [1]) between strips with a conduction between neighbouring electrodes destroying their isolation. A further implant (either lithographically defined [11] or as a low doped spray [12]) not only compensates the intrinsic charge densities of a few 10^{10}e/cm^2 to 10^{11}e/cm^2 depending on crystal orientation (<100> or <111>) but can be tuned to protect against oxide charge-up due to ionising dose. Figure 3 illustrates the field configuration for an n-in-p

design for LHC high luminosity upgrades (the HL-LHC [13]) with a p^+ isolation implant between the n^+ read-out strips. Finally, the crystal orientation influences not just the inter-strip isolation but also the inter-strip capacitance, as studies for ATLAS [14] and CMS [15] illustrate, particularly after irradiation (on which much more in Section 1.4).

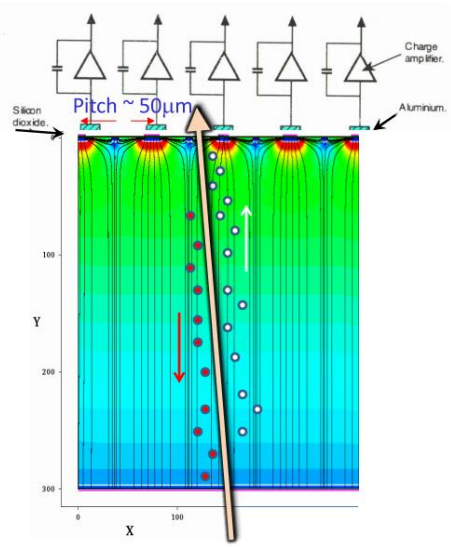

Figure 3 Electrostatic field and equipotential regions for an n-in-p strip detector with isolation structure. A charged particle passing through the depleted bulk produces electron-hole pairs which separate in the electric field giving an induced current on the input of the charge amplifier

A number of different technology details are discussed below, but it should be noted that once the problems of patterning the *n*-implant side was solved, the possibility of designing sensors with orthogonal strips on both faces (double-sided detectors [16]) became available and these were developed early in the history of collider based applications and used at the LEP, HERA, Tevatron, PEP-II, KEKB and CESR facilities. However, the different challenges of hadron colliders have led to other technology choices with cost optimisation for large areas of silicon playing a key role.

1.1. Strip Detectors

1.1.1. Electrical Characteristics

Two important properties for any semiconductor detector relate to the current through the device as a function of applied voltage. The forward bias current density dependence on voltage is governed by the Schockley equation, $J = J_0\,(e^{qV/k_BT} - 1)$ for temperature T and q the fundamental unit of charge. However, the reverse current in a silicon detector, as an indirect bandgap seminconductor, depends on the deep-level trap densities via the Schockley-Reid-Hall (SRH) process. Typical characteristics for a large area particle physics detector are illustrated in Figure 1. The reverse current depends on the levels of imperfections in the initial substrate material, on any issues during device processing and (as will be discussed in section 1.4) lattice damage due to irradiation. With the high resistivity $\rho \approx 10\text{k}\Omega\text{cm}$ materials often available for particle physics, current densities in 300µm thick devices can often be < nA/cm^2 even at room temperature. The other feature of note in Figure 1 is the voltage at which the reverse current rapidly increases (the breakdown voltage). This feature is also material and processing dependent. It results from charge multiplication of minority carriers in regions where the field significantly exceeds 10^7 V/m. Devices making use of such charge multiplication will be discussed later, but for the strip detectors discussed so far, avalanche breakdown represents an ultimate limit to the operating voltage. In a large sensor, often there is a local imperfection where a

'micro-discharge' occurs, where this can often be mitigated by improving the details of the strip implant and metal design [17].

To protect the microelectronics from current flow in the diode, either a decoupling 'AC chip' (as opposed to DC for direct coupling) with a capacitor and resistor for each channel (as used by ALEPH [18]) or a corresponding circuit integrated onto the sensor can be used. This also removes any influence of channel-to-channel variability of the read-out chip inputs from the sensor. The latter approach is the one adopted for nearly all strip detectors, with a thin oxide layer between the metal read-out strips connected to the microplex chips and the actual implanted strip. To ensure complete charge collection the coupling capacitance, C_{Cpl}, per unit length must be much greater than C_{Tot}, the sum of inter-strip capacitance and the strip capacitance to the detector backplane. This is dominated by inter-strip capacitance, which can be influenced by crystal orientation [15], radiation [14] and operating conditions [19], but it can be approximately parametrised as $C_{Tot} = \left(0.8 + 1.6\,{}^{w}/_{p}\right)\mathrm{pF/cm}$ for a given ratio of strip width, *w*, to pitch, *p* [15]. Note also that for a charge sensitive amplifier with feedback C_f, the signal seen by the amplifier is equal to ${}^{1}\Big/\left(1 + \frac{C_{Tot}}{AC_f}\right)$ times the charge produced in the detector, so the gain, A, and feedback capacitance, C_f , must be optimised for a given sensor design.

Given the typical resistance per unit length of the implanted strip, R_S, care must be taken when using an impendence meter to determine C_{Cpl} per unit length as the device acts as a transmission line for most frequencies of interest such that $Z \approx e^{-i\pi/4}\sqrt{\frac{R_s}{\omega C_{Cpl}}}$ for $x \gg \frac{1}{\sqrt{\omega R_s C_{Cpl}}}$ (angular frequency of impedance measurement, ω) [20] . Furthermore, without the direct connections to the amplifier input, the low voltage bias contact to the implanted strip must be achieved through additional features on the sensor. Depending on the amplifier shaper time-constant[1], τ, both C_{Tot} and the bias resistor, R_p , contribute to the equivalent noise charge as $0.96(\frac{v_n C_{Tot} x}{\sqrt{\tau}} \oplus 2\left(\frac{\tau k_B T}{R_p}\right)^{1/2})$ for amplifier noise referred to the input, v_n. These contributions add in quadrature also to terms coming from: shot noise ($1.14\sqrt{q\tau I_B}$) due the leakage current, I_B; thermal noise due to the implant resistance, $R_S x$, ($1.36\left(\frac{k_B T R_S x}{\tau}\right)^{1/2} C_{Tot} x$) and ${}^{1}/_{f}$ noise [21]. Typically, although the strip length, x, is fixed by the experiment requirements, R_s can be chosen low enough ($\lesssim 100k\Omega$/cm) not to impact the noise. Also cooling allows I_B to be reduced by a factor of ~2 for every 7 degrees reduction in temperature. The main processing and design challenge is to minimise C_{Tot} and maximise R_p for a given front-end amplifier shaper characteristics. Values for $R_p$typically need to be in the MΩ range, which requires additional features in the sensor design.

Once strip biasing is no longer linked to connecting to the amplifier inputs (often termed 'DC' coupling) it becomes possible to have "floating" strips between read-out strips at the same potential which can help make the charge division more linear between the read-out electrodes, either reducing channel count (and therefore cost and complexity) or improving spatial resolution [22]. However, for capacitive (or 'AC' coupling) of the inputs, a strategy to achieve the high resistance strip biasing is required. The first solutions employed technologies that did not require additional processing steps to those already needed to make the capacitively coupled sensors.

[1] Assumes a CR-RC shaper with equal time constant, *τ*, from equation 4.20 in Ref. [21]

For ALEPH, a bias rail (actually the guard ring) in close proximity (few µm) to the implanted strips provided a very high impedance connection relying on "reach-through" or "punch-through" biasing [23] for the p^+ strips. The development of this technology and the use of the inter-strip isolation structures to define a resistive path from n^+ strips to n^+ bias [18] allowed the development of the very first double-sided detectors. Features of these biasing techniques include that the p^+ strip potential difference to the guard ring is several volts (and the $\frac{dV}{dI}$ value easily meet the resistance requirements) while the n^+ strip connection only achieves high resistance once the depletion voltage is exceeded.

The implementation of a metal gate over the gap between the bias rail and the end of the strips, as shown in Figure 4, provides external control of both the voltage drop from the bias rail (drain) to the strip (source) in field (thick) oxide FET structure (FoxFET biasing [20]). (Processing of capacitively coupled detectors require, in the region of the p^+ implants, that a further capacitor oxide is developed over the device. The field oxide refers to the regions where this layer is in addition to the oxide left after the first etching step of Figure 2, between the p^+ implants.) This approach also lends itself to double-sided detectors with the added feature that while the p^+ side is an enhancement mode FET, with a negative gate-drain voltage increasing channel conductance from source to drain, the n^+ side FET operates in depletion mode with the negative gate-drain voltage here required to achieve high resistance [24] (in a structure with the added advantage that it introduces very little additional dead space).

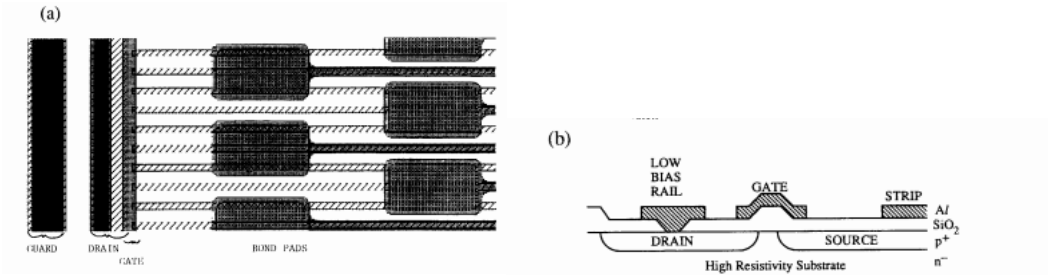

Figure 4 FoxFET Bias Concept Used by the (a) OPAL and (b) CDF Experiments. Reproduced from Ref. [25]

Before the OPAL microvertex detector, DELPHI developed an alternative technological approach which subsequently has become the default for AC-coupled single and double-sided strip detectors. The problem with implementing resistors for the µs shaping times suitable for LEP beam-crossing times is achieving the MΩ resistor value in a very small space, which, even with a serpentine design allowing a length/width ratio of 100□[2], needs a sheet resistance of > $10^4\Omega/\square$. The solution is chemical vapour deposition (CVD) of polycrystalline silicon (polysilicon) with very low doping (needing critical process control, as the sheet resistance varies with the fourth power of the implant density), which has a photolithographically defined shape, highly doped ohmic regions for metallic contacts and vias to contact to both the strips and the bias rail [27]. As one of the most complex silicon systems of the LEP era, the final version of the DELPHI micro-vertex detector [28] will be discussed in a little more detail as developments for both the Tevatron and LHC benefited from several of those initiated by DELPHI.

[2] The symbol □ is used to denote an aspect ratio of a two dimensional structure in semiconductors processing. A sheet resistance is quoted in these units since any structure's actual resistance is proportional to length/width (a unitless quantity) times the resistance in Ω/□.

The key technology features are shown in Figure 5. The photograph shows the ohmic (back) side of the sensor with n^+ strips reading out the z-coordinate along the sensor parallel to the beam axis in the experiment. In this example there is p^+ stop implant around every n^+ strip to interrupt the electron accumulation layer under the oxide which would otherwise short the n^+ strips together [29]. (Note DELPHI also explored field plate isolation which avoids this additional implantation step, but use of this technique alone is less forgiving of processing imperfections due the higher electric fields at the strip implant edges [30]). In Figure 5 the photograph also shows the serpentine profile of the polysilicon resistors to achieve the greatest length/width in the limited space available at the end of the strip. Note the implant runs beneath the polysilicon so this region is still sensitive but the capacitive metal strip can only run over the implant away from the resistors where an aluminium contact links these to the implants (and also allows probing of the strip implants during testing). Note the resistors for every second strip is at the other end of the strip.

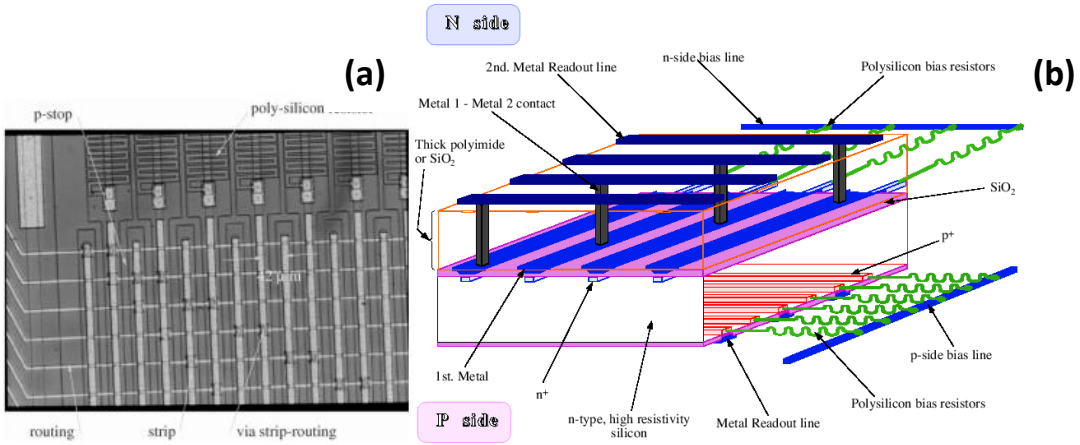

Figure 5 Photograph of the corner of (a) a DELPHI double-sided sensor and (b) corresponding diagram, Panel (a) is reproduced from Ref. [30] and panel (b) is reproduced from Ref. [8]

The routing of the z-strip signals to the same end of the sensors as the rϕ measuring strips, to avoid read-out chips within the sensitive volume of the detector, is achieved by having a thick (at least 3µm CVD SiO_2) insulator layer over which the routing aluminium strips (Metal 2) run. The optimisation of the various insulator layers is vital to these designs. C_{Cpl} needs to be as large as possible to get as much of the signal as possible coupling to Metal 1. However, the dielectric (SiO_2 sometimes also with CVD Si_3N [12]) thickness (typically of ~200nm) has to be a trade-off between achieving high C_{Cpl} and maintaining excellent device yield with over tens of cm^2 of sensor area. If, however, the Metal 1 to Metal 2 insulator layer is too thin, signal will again be lost due to the complicated capacitor network. For double-sided detectors, the implants on at least one side or possibly both usually need to be at an elevated voltage to have at least the full depletion voltage between the N-side and P-side strips of the detector. Unless, as for ALEPH [18] a 'high ground' is used for electronics reading out the N-side, the on-detector dielectrics are required to offset the voltage between the implanted strips and the (near ground) input voltages of the microplex chips. This adds the stringent requirement that on at least one side (usually the N-side since a broadened aluminium Metal 1 can act as a field plate [30]) the dielectric over the full sensor needs to hold off the depletion voltage. For the tens of volts typically needed for LEP detectors this was not such a major problem, but once radiation induced changes to the required operating voltage occur, this can become an issue. Such complicated sensor designs required rigorous quality control, both in terms of the company's own procedures and also the collaboration's reception testing of delivered devices. The high voltage operation specifications did prove demanding since a

dielectric failure anywhere on the sensor would prevent operation unless the wire-bond from the affected strip to the microelectronics could be removed. Such mitigation strategies were adopted by experiments using double-side detectors where an offset voltage was not used for the electronics. The many components and complexity of the final version of the DELPHI silicon tracker, including forward pixel planes (discussed in 1.2) and mini-strip planes [28] are illustrated in Figure 6.

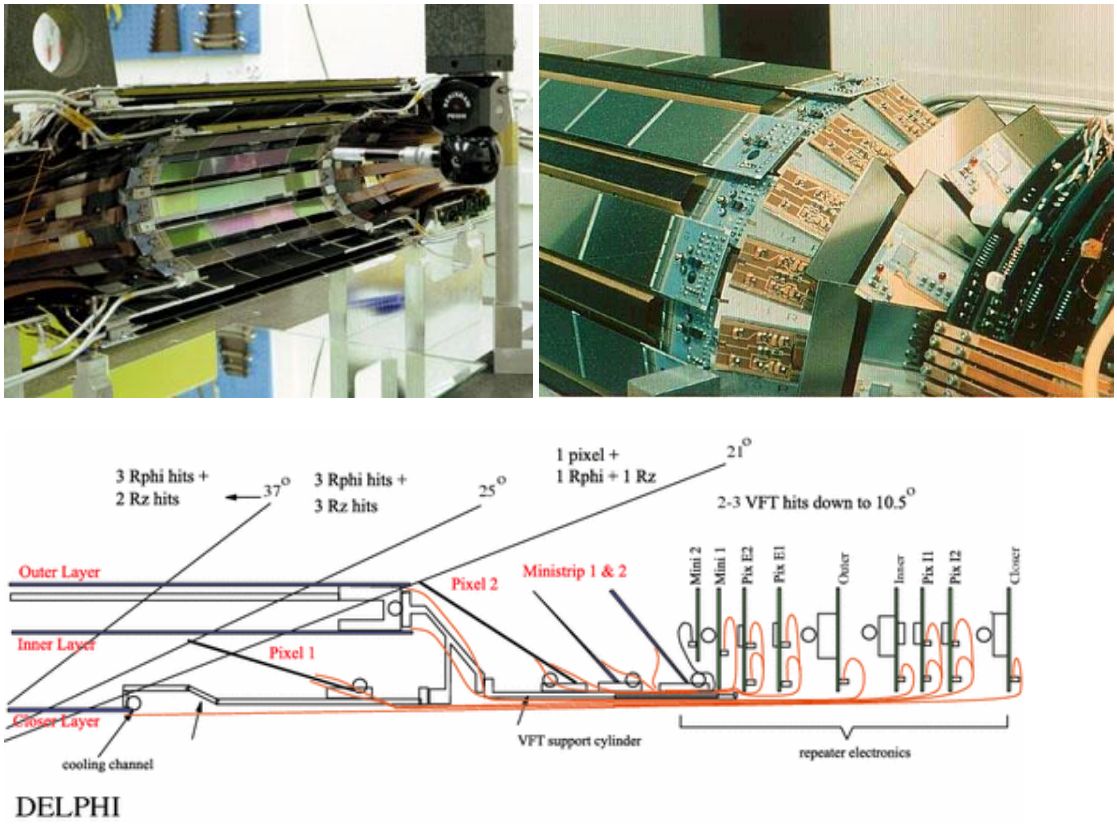

Figure 6 Photographs and Schematic of the DELPHI LEP2 Silicon Tracker (Photographs reproduced with permission from CERN, schematic reproduced from [31])

1.1.2. Readout Microelectronics and Interconnects

Without the exploitation of developments in microelectronics and access to designers able to realise designs for particle physics in application specific integrated circuits (ASICs), [32], [33], it would not have been possible to exploit silicon detector technology in collider environments. As part of this pioneering work, many different chips were designed, initially for the UA2 experiment at CERN's S$\bar{p}p$S Collider [34], the Mark II Experiment at the Stanford Linear Collider (SLC) [35] and the ALEPH [36] and DELPHI [37] experiments at CERN's LEP Collider. A number of strategies were developed for signal amplification, storage and readout. That for the original 128 channel microplex chip in 5µm nMOS technology is shown in Figure 7. The timing of collisions at LEP with 4 bunch operation was 22.5µs (although to increase luminosity the number of bunches in the machine was later increased). Each channel has two inputs, one from calibration lines and the other from the sensor strip connected via 25µm diameter aluminium wires. The calibration circuit both tests every input and measures, for a known C_{cal} and external voltage step, the chip output for a known injected charge, $Q = C_{cal}V_{step}$. Prior to a signal from the calibration or bunch crossing, the Reset switch clears the charge on the

integration capacitor C_{int} and then opens just prior to when signals should appear. The signal, Q_S, and any input due to current in the chip or from the sensor, $I\Delta t$, give rise to an output voltage, $\frac{Q_S+I\Delta t}{C_{int}}$. Assuming that the Reset remains open, the Store switch allows this signal to be transferred to C_{store} a time Δt after the Reset. If the collision is empty (no minimum bias trigger) then this cycle of switches repeats, but if there is a trigger then, instead, the readout sequence is initiated with the stored signal preserved and a pulse clocked down the shift register reading out the voltage on the output from each C_{store} in turn. In practice the Reset switch also injects voltage, so the MX family of chips used double correlated sampling to record on one storage capacitor the signal before the beam crossing and the signal after the beam crossing on another storage capacitor. The differential output is clocked out onto a balanced twisted pair as for the nMOS chip which improves pick-up rejection. The Reset voltage and other noise sources that appear equally on both storage capacitors are thus supressed. Even so, the recorded data for each channel will show channel to channel ("pedestal") variation in the absence of signals which needs to be averaged and subtracted to allow the values of Q_S for triggered events to be recorded for those channels where this is above a preset threshold (usually defined in terms of the channel noise, σ_{rms}). A typical analysis to extract hit coordinates might first select channels where the signal minus pedestal is greater than $4 \times \sigma_{rms}$ where σ_{rms} is the root mean square variation (noise) for that channel. Adjacent channels are then also included in the hit cluster if their Q_S is more than (typically) 1.5 to $2 \times \sigma_{rms}$. The hit coordinate is found from analysing the cluster shape, either as a weighted mean (using the pulse heights) or a more sophisticated modelling of the charge sharing or spreading due to diffusion and track angle.

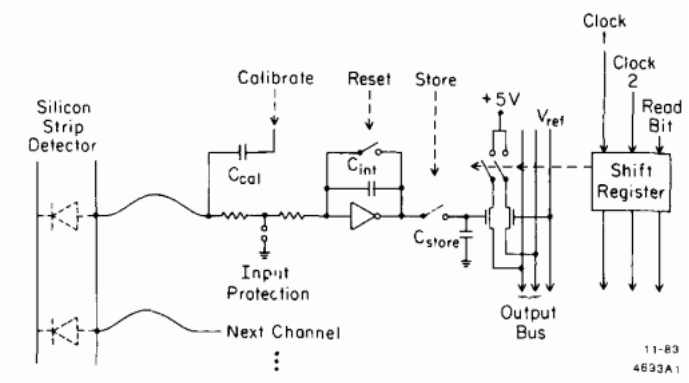

Figure 7 Front-end design of the original nMOS ASIC for silicon microstrip readout. Figure reproduced from Ref. [32]

More recent designs have the front-ends with RC-CR pre-amplifier and shaper response (as already discussed in Section 1.1.1 [21]). The high rates of interactions at ep and pp colliders require in-chip data storage while the online 'trigger' system decides which beam-crossings contain interesting events for further analysis. At the LHC, calorimeter and muon chamber information is used to return a 'first level' (L1) hardware trigger in around 2 to 5μs. With 25ns per beam crossing this means that 100-200 (~500 for HL-LHC) events worth of data needs to be stored for each channel while awaiting the "L1 Accept" signal. Following the designs for the Tevatron and HERA, this is achieved with a pipeline clocked at the beam-crossing frequency and synchronised such that the front-end circuit output is sampled either around or at the time of the front-end circuit peak output (depending on whether the time response of this circuit spans several beam-crossings or not). Note, for a fast shaper, the $\frac{v_n C_{Tot} x}{\sqrt{\tau}}$

term comes to dominate the noise, so there is an advantage in not making τ any smaller than necessary. The time from a beam-crossing to the L1 decision is called the L1 latency and for a fixed latency system, the decision always corresponds to a fixed number of clock cycles after the event of interest, allowing only data from that beam crossing (and possibly also those adjacent in time to that beam crossing) to be read out through a shift register as for the microplex chips. Further buffering allows multiple L1 Accepts during the L1 latency or during read-out to be managed without dead-time. Data transmission from the ASICs to the outside of the experiment has also required the development of specialist radiation-hard optical link technologies for the LHC experiments.

For their front-end ASICs, LHCb and CMS have chosen to use an 'analogue' pipeline that preserves the pulse height information for every channel while ATLAS, following the experience of the ZEUS LPS at HERA [38], elected to have a front-end discriminator such that only channels above an externally settable threshold register a '1' into a "binary" pipeline, while all channels for which signal is below threshold register a '0'. This simplification reduces complexity, connectivity requirements and power consumption but at a significant loss in flexibility. In practice it has been found to make little difference to the achievable spatial resolution but it does complicate calibration and testing. Another benefit for CMS is that, with multiple measurements of the energy deposited in the silicon layers, $^{dE}/_{dx}$, coupled with knowing the track momentum, it becomes possible to aid particle identification up to a few GeV/c. However, the strip trackers for the HL-LHC will have to adopt a binary approach due to the limited available transmission bandwidth for detector read-out coupled with the much larger number of read-out channels needed to cope with the factor of ten higher hit occupancies (when compared with the original LHC specifications).

Table 1 shows a few representative parameters for a number of readout chips for strip detectors fabricated over the last 3 decades, in particular for the noise in electrons (equivalent noise charge, ENC). The depth of pipeline, digital complexity, power consumption or whether analogue, digital or binary read-out are not discussed. What the table does illustrate is that noise performance for strip detectors has been maintained despite a two orders of magnitude increase in speed requirements and three orders of magnitude in radiation levels, along with the associated data rates. This combined with the vast increase in the numbers of channels and area of detector to be read out, illustrated in Figure 3 of the main document, give a sense of the progress since the md 1980s. This has been achieved at least in large part due to the steady reduction in the available minimum feature size from the 5µm of the first Microplex to the 0.25µm of the APV25 chip. The trend continues with the development of 180nm, 130nm and 65nm ASICs for current and future projects.

ASIC Series	Experiment	Peaking/Response Time (ns)	Noise ($a + bC_{Tot}$) a (enc), b (enc/pF)	Radiation Hardness (kGy)
Microplex [32]	**Mark-II**	~10^3	280, 97	~0.5
CAMEX64A [33]	**ALEPH**	~10^3	335, 35	~0.1
MX1, MX3, MX6 [37]	**DELPHI**	~10^3	340, 20	~0.1
MX5, MX7 [25]	**OPAL**	~10^3	325, 23	~0.4
SVX [39]	**L3**	~10^3	350, 58	~0.2
SVXD, SVXH, SVX3 [40]	**CDF, D0**	132/396	600, 60	100
APC128 [41]	**H1**	100	700, 50	~1
HELIX [42]	**ZEUS, HERA-B**	50	340, 40	5
AToM [43]	**BABar**	100-400 (tunable)	300, 30	50
VA1 [44]	**Belle**	~10^3	200, 8	20

Beetle [45]	**LHCb**	24	450, 50	300
ABCD3TA [46]	**ATLAS**	20	400, 70	100
APV25 [47]	**CMS**	50 (peak)	270, 38	200

Table 1 Some Representative ASIC Parameters (CMOS minimum feature sizes range from 5µm to 0.25µm) for constructed detectors

1.2.Pixel detectors

As the density of hits in a silicon plane increases, the ability to unambiguously reconstruct position coordinates in 2D from patterns of hits on orthogonal strips diminishes. In practice, strip systems for hadron colliders are obliged to orientate the strips at small angles (40 mrad in ATLAS) to remove ambiguities but this comes at the cost of the spatial resolution that can be extracted in the direction along the strips. At higher radii and where the measurement of track bending in the rϕ plane to measure momentum is much more critical, this matters less but at low radii alternative technologies are needed. As discussed in the Historical Development Supplementary Information, the first applications of hybrid pixel sensors were in the Omega Spectrometer [48] and DELPHI [49], but for vertexing at the LHC this technology is essential [50], as hit rates can be as high as several hundred MHz/cm^2 (LHC) or GHz/cm^2 (HL-LHC). The key ingredients for these vertex detectors are illustrated in Figure 8. These consist of a silicon detector processed with 'under bump metallization' (UBM) and high density read-out ASICs with UBM bond pads matched to those of the sensor, connected via either SnPb, AsAg, AuSn solder bumps electroplated to one device or In bumps evaporated on both devices [9]. High precision alignment, heat and pressure are necessary to make reliable contacts from sensor to readout.

The key technological challenges for hybrid pixels are achieving the required data processing rates, radiation hardness (both sensor and microelectronics) and very high throughput and yields for large area silicon chips mated together with up to 40,000 connections per cm^2.

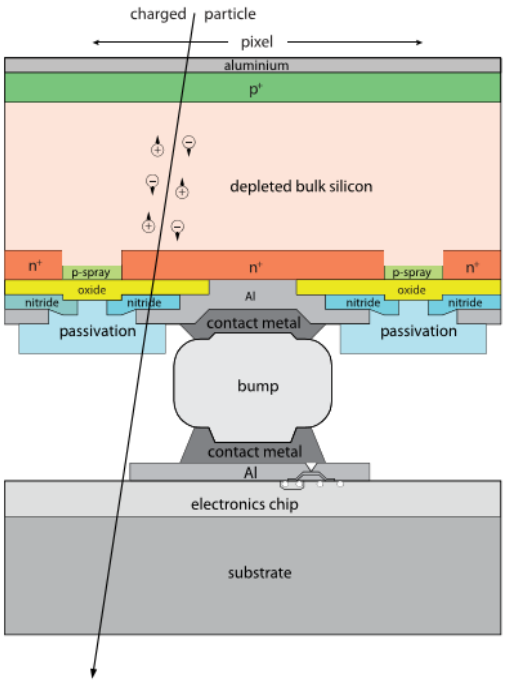

Figure 8 Hybrid Pixel Detector Concept. Figure reproduced from Ref. [9]

1.2.1. Electrical Characteristics of Planar Sensors

As the areas of each pixel is small, the noise contributions due to leakage current and detector capacitance are much smaller than for strips, but as will be discussed below, the effects of radiation impact both signal and leakage current to compromise the achievable signal/noise. Furthermore, the hugely increased number of read-out channels compared to a strip detector mean that the readout chips must achieve a massive data reduction to be able to communicate through a practical number of electrical connections. To suppress data, only channels with signal above a pre-set threshold can be read out and that threshold must be significantly greater than the intrinsic electronics noise, with a threshold value of 2500e typical for current LHC detectors. As for strip detectors, collected charge is spread out both due to diffusion during drift and by the Lorentz force due to the experiment magnetic field. Designs therefore have to maintain efficiency when the total cluster signal is potentially shared across many pixels. Radiation both increases the required operating voltage and greatly reduces the carrier lifetime (see [1]). Therefore, signal will also be lost for longer drift distances and, due to their lower mobility, holes will trap more readily than electrons. This and other advantages have motived the development of electron collecting (n^+ electrode) pixel detectors [51], [52], [53]. Figure 9 shows the measured signal for such detectors as a function of voltage at doses up to those expected for the innermost pixel layer at the HL-LHC [53]. Retaining high efficiency, particularly for inclined tracks, is

also a key consideration for hybrid pixel detector design.

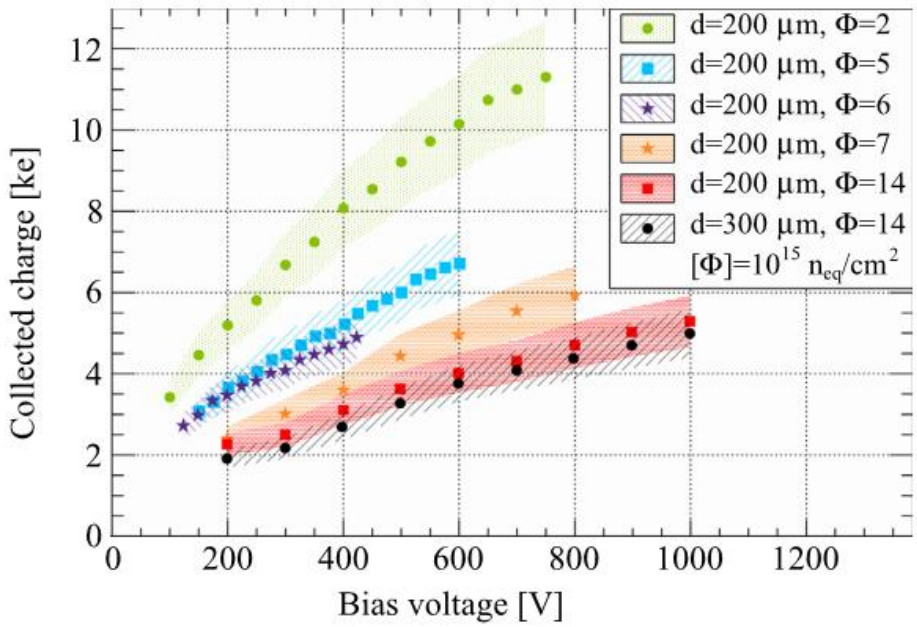

Figure 9 Planar Hybrid Sensors with n^+ Electrodes of 200um and 300um Thickness Irradiated up to $1.4\times10^{16} n_{eq}/cm^2$ Figure reproduced from Ref. [53]

The low leakage current per electrode due to the tiny area of silicon in each diode removes the requirement from the electronics for AC coupling on the sensor, although very effective cooling is anyway required for a number of reasons discussed below. This means that bias structures are not strictly needed. However, they are often implemented as without them sensor quality control is difficult to achieve as there is no practical way to quickly measure the full detector I(V). Reach-through biasing best achieves this with minimal loss of sensitive area and no required additional processing steps [53].

Strip and pixel sensors can have up to 1mm from the last active implant to the sensor physical edge to avoid excessive edge currents and low breakdown voltage due to imperfections where the silicon can been cut. Overlapping sensors in both directions can be problematic due to space constraints, especially at low radius, so to keep the tracking coverage as hermetic as possible, extra processing to reduce this dead area is desirable but can increase costs [54].

1.2.2. Electrical Characteristics of 3D Sensors

The need for higher operating voltages and the effects of trapping are both significantly mitigated by using detectors where alternating p^+ and n^+ doped columns penetrate through the sensor (a 3 dimensional, "3D", electrode distribution [55] [56], [57]) rather than (as for planar processing) having electrodes simply implanted at the device surfaces. The process requires hole production via deep reactive ion etching, followed by thermal diffusion to dope the walls of electrode columns and the possibility to further fill the holes with polysilicon. Although for planar detectors, lower depletion voltages and drift distances can equally be achieved by making thinner devices, in this case the signal also reduces with the thickness. With 3D designs, the inter-electrode distance can be made small while keeping the same device thickness, as illustrated in Figure 10 for a range of different technologies. A number of designs [58], [59], [60] can be achieved with the aim of maximising yields, reducing low field regions, avoiding non-uniformities and minimising regions where the electric field could

approach the condition for avalanche breakdown. One way this can be achieved, as in Figure 10 b) and c), is by avoiding the *n* column penetrating all the way to the sensor back. Figure 11 shows that good track finding efficiency (97%) is obtained even after HL-LHC doses with only 160V operating bias for such a design [61].

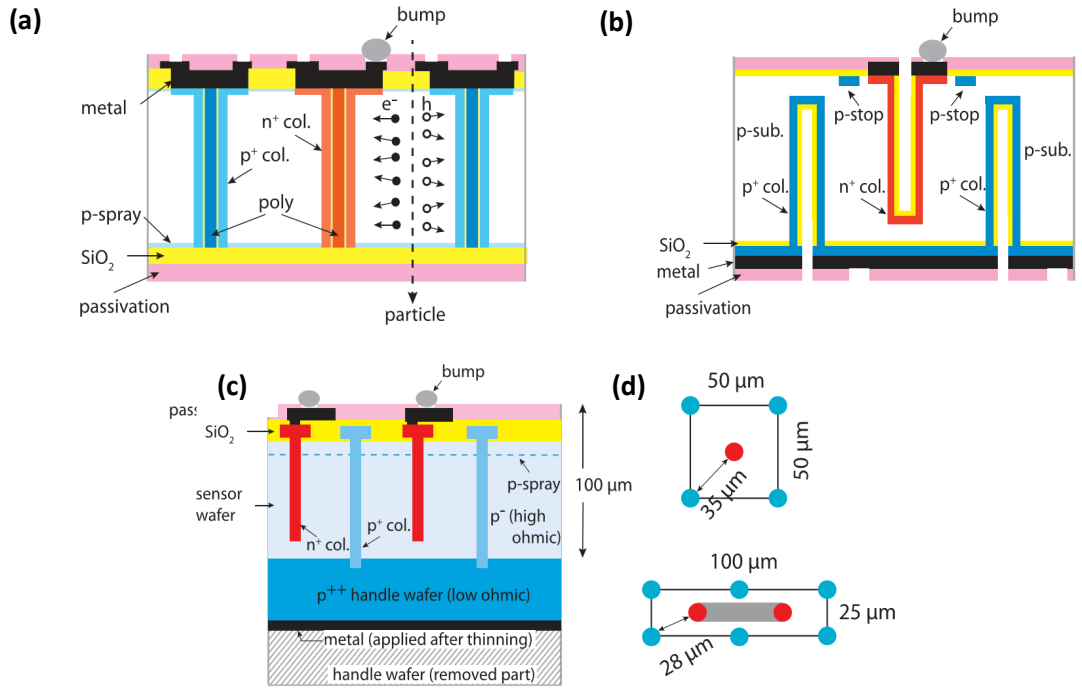

Figure 10 3D Sensor Designs a) Columns etched from top b) Two-sided etching c) Single-sided etching with handle wafer, d) column spacings. Panel (d) is reproduced from Ref. [10]

The added complexity of producing these 3D detectors does allow, without additional processing steps, the production of 'active edge' detectors where the outer walls of the detector can be defined by etching and doping to be as close to the outer electrodes as the typical inter-electrode spacing. Such devices can be butted together with an unprecedented ratio of active area to dead area [62]. This helps in building arrays of sensors without complicated overlaps to keep the tracking hermetic and has benefits where the space for detectors is very limited [63].

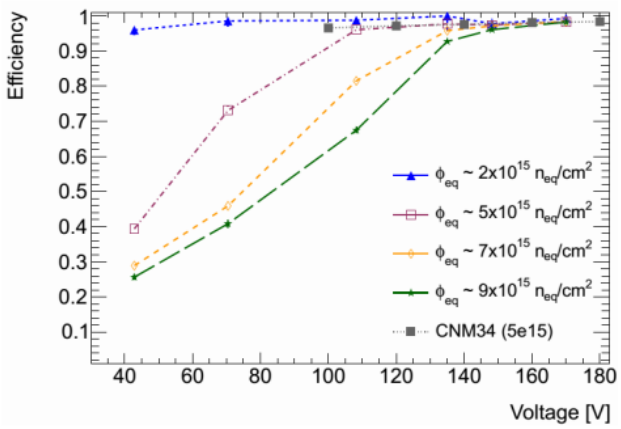

Figure 11 ATLAS IBL 3D Sensor Read-out Efficiency vs Dose with 1500e threshold. Figure reproduced from Ref. [59]

1.2.3. Pixel Readout Microelectronics and Interconnects

The evolution of hybrid pixel microelectronics has followed the same technology trends as that for strips but with the requirements of much greater channel numbers, very limited space per channel for front-end circuitry and more complicated interconnect technology. Even with much more sophisticated on-chip data reduction, there are major challenges coming from the required data bandwidth both within the chip and to the outside. For hadron colliders in particular, to this is added the problem of operating in the highest radiation region of the experiment. Connectivity to the sensor is most commonly achieved through electrochemical application of solder micro bumps to either the chip or sensor [50]. Pitches down to 25µm are currently achievable as are yields above 99% [9]. Vapour deposition of indium on both surfaces has also been widely used [64].

Table 2 lists some of the different recent hybrid pixel chip developments in particle physics for fixed target, LHC, HL-LHC, CLIC and for x-ray applications in medical, space and synchrotron science. The last two rows reflect the progressive requirements at the LHC and HL-LHC [9]. A common feature is the use of Time over Threshold (ToT) to digitally encode the pulse height for pixels where the signal has exceeded the pre-set threshold in the comparator, by counting the number of clock cycles for which the comparator output is high. The earlier devices have mainly analogue pixel matrices and column drain architecture to bring hit information to the periphery for data processing, digital storage and data transmission. As required hit densities and rates increase, the transmission to the periphery needs greater bandwidth, so the next step has been to move much of the digital processing and storage functionality into the pixels themselves. The 65nm RD53 chip for ATLAS and CMS has the analogue features embedded in small islands surrounded by a sea of digital circuitry with logical complexity similar to that of commercial microprocessors [9].

Minimum feature size	250nm	130nm	65nm
Example Read-out Hybrid Pixel Chips	ATLAS FE-I3 [65] CMS [66] Medipix [67]	NA62 TDCPix [68] ATLAS IBL FE-I4 [69] LHCb VeloPix [70] Medipix3RX [71] TimePix3 [72]	CLICpix [73] RD53A [74] TimePix4 [75]
Typical hit data storage density capabilities	<1Gb/s/cm^2	~5Gbp/s/cm^2	40Gb/s/cm^2

Output Bandwidth	40-160 Mb/s	0.3-1.2 Gb/s	2-20 Gb/s

Table 2 Recent evolution of pixel readout chips (table reproduced from [9])

1.3. Drift Detectors

Inspired in part by the evolution of the more mature gaseous tracking detector technologies, an alternative route to achieving truly 2 dimensional readout without a vast increase in the number of channels was to use field shaping electrodes on the sensor to drift the produced charge cloud to one end of the sensor such that the arrival time (with respect to a known interaction time) could be used to determine the coordinate along the drift direction [76]. Through use of lateral depletion (see Figure 12 and Figure 13) a potential minimum valley for majority carriers can be created which channels charge towards the substrate contact electrode. Because this signal collecting nodes can be small, such detectors have very low capacitance allowing excellent signal/noise leading to their providing both good position and excellent energy resolution [77]. As an example, cylindrical drift detectors have been developed for high resolution x-ray spectroscopy applications [3].

Reading 2D information just from one edge also minimises the material due to readout and associated services. However, spatial variations in the bulk material mobility (and hence charge drift velocity) and the relatively low rate capabilities have limited their use as particle tracking detectors, although examples of use can be found in heavy ion colliders (see for example [78], [79]) where the event rates are low but of high complexity. The long drift times also give greater sensitivity to the reduction in carrier lifetimes due to irradiation as discussed in Section 1.4.

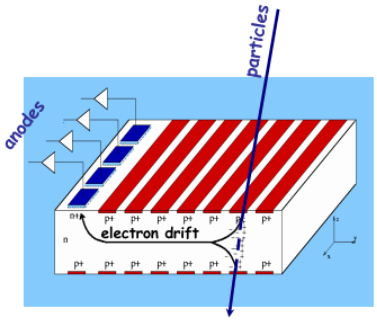

Figure 12 Principle of operation of a silicon drift detector. Figure reproduced from Ref. [3]

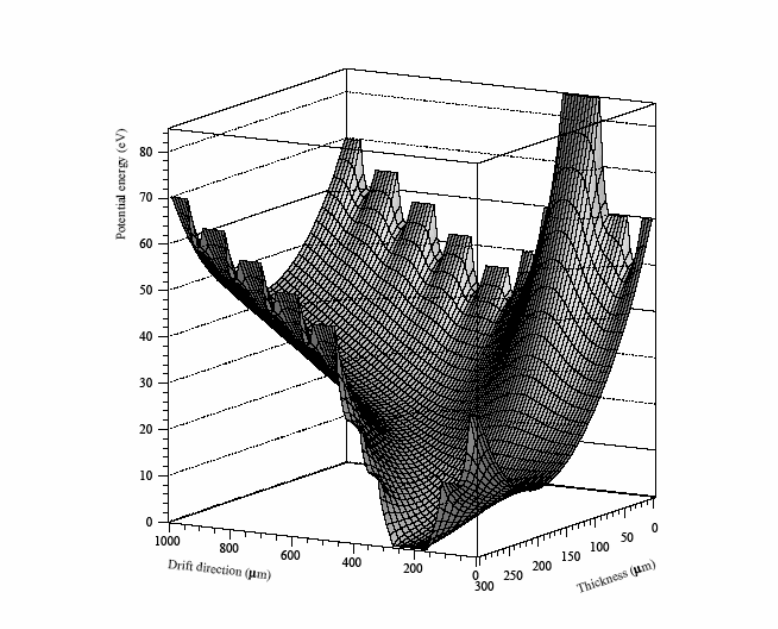

Figure 13 Potential map inside a drift detector illustrating how charge is drifted to the collecting electrode. Figure reproduced from Ref. [3]

1.4. Radiation Effects

1.4.1. Sensors

A key advantage over other possible tracking technologies for silicon is its good rate and radiation tolerance so that both the instantaneous and integrated particle fluences at facilities like the LHC and the HL-LHC can be tolerated. However, the surface and bulk properties of the material do change, with different implications for different technologies realised in silicon. Many of the initial studies on silicon irradiation effects at the LHC were carried out by the RD2 and RD20 collaborations [80].

Radiation effects can be characterised by two processes: ionisation and displacement damage. The former, measured by the integrated total ionising dose (TID) is more familiar and can be conveniently measured in the usual units for radiation dose (Gy or Rads where 100 Rads = 1 Gy). The TID is the main source of damage to electronics, but for the sensors it mainly causes charge build-up at interfaces such as the SiO_2-Si interface where it can change the characteristics of reach-through or FoxFET biased detectors [81], increase local electric fields (along with the potential for breakdown at implant edges) and compensate the p^+ isolation structures for n-in-p detectors, potentially leading to the strips shorting together if the p^+ isolation dose is not high enough. The oxide charge density largely saturates with ionising dose at around 2.5-3.5×$10^{12}e^-/cm^2$ [82] so this sets the minimum p^+ doping density needed to maintain good strip isolation as a function of dose [83]. However, the observed inter-strip isolation and onset protection voltage (using the punch-through effect described in Section 1.1.1 to limit voltage excursions on strips due to excess current) continue to degrade above 1 MGy [84].

Whereas polysilicon biasing and high enough implantation doping can counter the effects of total ionising dose on the sensors, the effects of displacement damage do significantly deteriorate the device performance [85] [86]. This is parameterised by the non-ionising energy loss (NIEL) which measures the extent to which the silicon lattice is damaged by irradiation (see [87] and Figure 14).

When an atom is displaced from its location in the lattice a Frenkel pair is formed of the vacancy and the interstitial atom. This can both directly alter the substrate properties or, because at finite temperature the vacancy and interstitial atom are free to propagate through the lattice, lead to more complex defect clusters. Depending on the presence of either lattice site substitute or interstitial impurities, electrically active defect states can form which contribute additional levels in the band-gap. The NIEL assumption [86], [87] is that all the effects of substrate damage for different particle types simply scale according to their relative NIEL as a function energy as illustrated in Figure 14. Using this assumption, different particle fluences are all expressed in units of 1MeV neutron equivalent flux, usually written as n_{eq}/cm^2. This assumption works reasonably well for leakage current increases and (to a lesser extent) charge trapping, but does not hold for changes to effective bulk doping concentration where substrates have an enhanced presence of interstitial oxygen [87].

As already discussed in 1.1.1, enhanced defect concentrations will lead to increases in dark current through the SRH mechanism leading eventually to the need to operate at reduced temperature to suppress this. This leakage current not only contributes noise in the electronics it also leads to heating, with the risk of 'thermal runaway' [88] since increases in temperature lead to further current increases and so on. This effect drives a considerable part of the thermal management and cooling design requirements for detectors in high radiation environments.

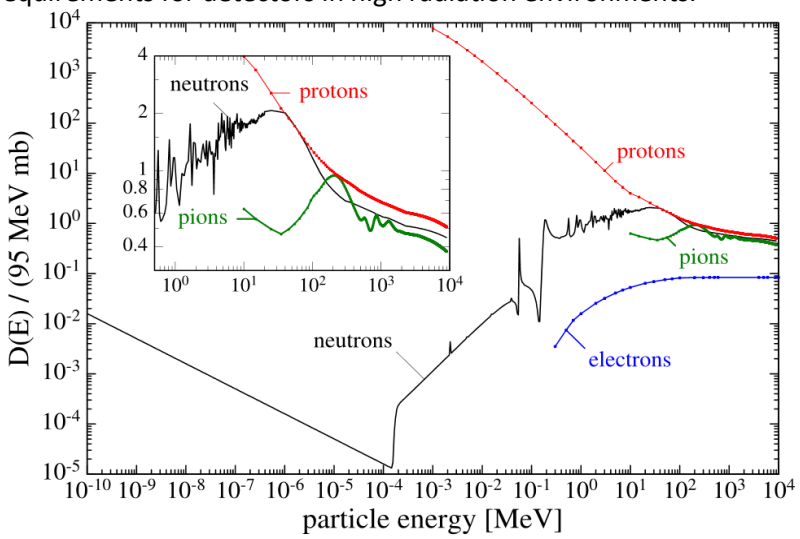

Figure 14 Non-ionising Energy Losses for Different Particle Species in Silicon (reproduced from Ref. [87])

As the substrate doping is only ~$10^{12}/cm^3$ in particle physics silicon detectors, the defect cluster concentrations can build up to exceed this, leading to the effective substrate doping being determined by the defect density. The impact depends on the details of the substrate, but for planar silicon sensors, this leads, for n^- substrate detectors with depletion voltages in the few tens range, to type inversion, with an effectively p^- substrate, after fluences around $2\times10^{13}n_{eq}/cm^2$ since the defect clusters act mainly as acceptor states [8], [86] , [87] (an effect already witnessed at the LHC [89]). Detectors irradiated well beyond this (for example to $3\times10^{14}n_{eq}/cm^2$) can still be read-out via p^+ contacts, even if partially depleted, but with lower efficiency than detectors implanted with n^+ contacts [90]. For detectors with n^+ contacts for the read-out and n^- substrate (often denoted n-in-n designs), irradiation eventually leads to an effectively p-type substrate with depletion growing from the read-out side as required for high efficiency. However, before irradiation the depletion grows from the p^+n^- junction on the back of the device. Since the p^+ back-bias implant cannot extend to the cut region without large currents and electrical breakdown, for an n-in-n design the p^+ implant on the back

must also be lithographically defined [91], [92], thus requiring double-sided processing and additional cost. This can be avoided if the starting substrate material is p^- (n-in-p detectors [93], [94]).

In practice, for ATLAS and CMS the best cost-performance optimisation was to use p-in-n for strips at large radius (lower dose, highest area) with n-in-n pixels for the highest dose regions. LHCb chose n-in-n strips (using an elegant routing design employing the technology described in Figure 5 to minimise material in the active region [95]). However, at the HL-LHC, even the large area strip sensors will receive over $10^{15} n_{eq}/cm^2$ and n-in-p offers a more cost effective solution for large area detectors to withstand such high fluences [96]. This can be further enhanced by "defect engineering", deliberate inclusion of interstitial impurity atoms, using the understanding developed by the RD48 [97] and RD50 [98] collaborations. Oxygen enriched detectors show improved hardness to pions and protons but not neutrons for example (showing the limitations of the NIEL hypothesis) [87]. Because the defect complex formation continues after irradiation in a temperature dependent way, leading to further deteriorating of the device performance [99], operation at low temperature (typically ~-20°C) during the lifetime of the experiments is required as a mitigation strategy.

A further complication to operation after irradiation is that, at the highest fluences, the defect clusters result in loss of carrier lifetime such that the detected signal is reduced. The combined effects of trapping and changes to effective doping are complicated, with both temperature and time dependencies that lead to changes (annealing) long after the irradiation causing the damage has ceased. Modelling of this requires taking full account of how signal formation takes place alongside the microscopic understanding of the defect dynamics [98] and the behaviour can be parametrised as a function of fluence, temperature and time [87]. Depending on the initial material, the effective doping with time first recovers slightly before further deteriorating. (The dark current, however, always benefits from annealing [86].) To reduce effects of fast annealing processes (which may depend on the details of the device temperature history during and just after irradiation) and to better mimic the likely behaviour after periods of unavoidable room temperature operation, comparisons are made after an accelerated annealing at +60°C for 80 minutes. A compilation of HL-LHC data on the signal seen at 500V vs fluence is shown in Figure 15 [100]. That the green points (neutrons) are lower is understood in terms of differences in detailed defect formation [86] for reactor neutrons compared with higher energy charged particle beams (meaning that the NIEL hypothesis is not fully valid, as already mentioned for oxygenated silicon [87]). Signal collection for devices with high defect concentrations are further complicated by a double peak electric field distribution coming from space-charge build-up due to partial trapping of charge carriers [101]. Also the signal at the highest fluences is understood to have contributions from effects similar to the charge multiplication processes exploited in the LGAD designs of section 1.5 (although note that the dark current is also amplified by the same factor [102]). Operation at higher voltages further improve the signal seen at the largest doses. For an up to date summary of recent results and parametrisations see [87].

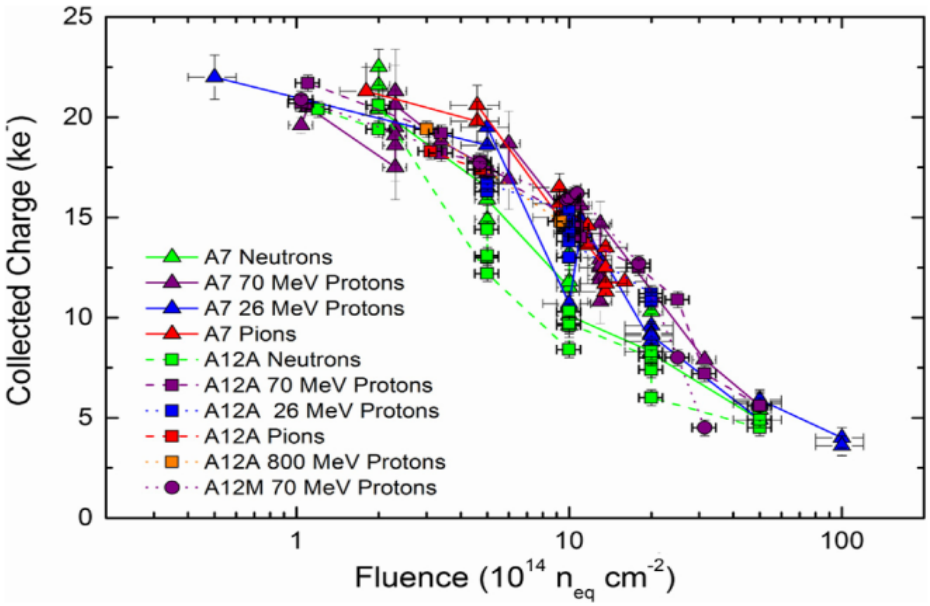

Figure 15 Charge collection at 500V vs fluence (corrected to 1 MeV neutron equivalent using the NIEL hypothesis). Figure reproduced from Ref. [100]

1.4.2. Microelectronics

Radiation effects in the microelectronics is another major topic with a vast literature. Build-up of positive charge in SiO_2 structures and at interfaces (as for sensors) due to the total ionising dose (TID) is the dominant issue [9]. Here, the impact can vary significantly with commercial manufacturing details over which it can be hard to have much influence. For 0.25µm chip designs, such as the APV25 [47], CMS used custom CMOS Enclosed Layout Transistor (ELT) designs for which channel edge effects can be significantly reduced [9] but other effects can still limit performance [103] . However, such an approach is not usually practical in commercial designs of smaller feature size (0.13µm 0.065µm) and also less necessary, but devices need careful characterisation, also at intermediate doses (several kGy) where adverse effects can be seen which actually compensate each other at high doses [104].

Although the intermediate dose effects just discussed can lead to significant operational problems if not known in advance [105], once anticipated and characterised for a given delivered ASIC as a function of dose rate, operating temperature and annealing time they can be protected against. This does, however, come at the cost of greater cooling capacity which tends to increase material and therefore scattering in the detector. The limitations at the highest doses are much more severe and result both from the reduced feature sizes and the processing complexity needed to achieve this [9], [106]. The effects are technology, manufacturer, temperature, annealing and transistor type dependent [9]. Figure 16 shows PMOS transistor characteristics in a 65nm technology as a function of dose [107] for different transistor designs with the same channel length irradiated at -15°C. Not only do all devices suffer significant deterioration after 10 MGy (1Grad) the deterioration can continue after irradiation. Current technologies are not considered robust enough to guarantee device performance much beyond 5MGy [9].

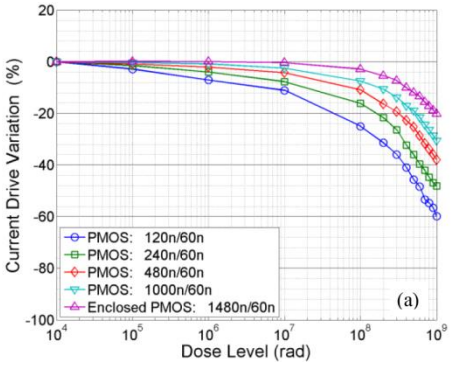

Figure 16 Current drive variation in 65nm technology PMOS transistors with varying transistor width. Figure reproduced from Ref. [107]

In addition to accumulated dose, ionisation can induce Single Event Upsets (SEUs) which can switch logic or memory in digital circuitry, potentially leading to latch-up conditions that can require resetting or power cycling the microelectronics and can result in device failure. Mitigation can be achieved by both device design and circuit design (for example triple redundancy) or by continuous refresh of configuration data during operation [9]. In practice SEU effects are usually less of a limitation for particle physics experiments but care needs to be taken.

1.5. Fast Timing Detectors

For non-tracking applications, a number of technologies have been developed which achieve very fast and high signal/noise through exploiting signal amplification through avalanche multiplication. In very high field regions (>10^7V/m), charges will be accelerated sufficiently to create further electron-hole pair production, effectively leading to amplification. A number of detectors, such as Avalanche Photodiode Detectors (APDs, [3]) and Silicon Photo-Multipliers (SiPMs [108]) provide single photon counting capabilities operating at room temperatures exploiting the signal/noise achievable with high signal multiplication. They also offer excellent timing resolution.

Low Gain Avalanche Detectors (LGADs) are a variety of Ultra-Fast Silicon Detectors (UFSDs) for simultaneous charged particle tracking and timing. The LGAD principle is illustrated in Figure 17 where a high field region is deliberately created in a very shallow region just below the diode junction. Figure 17 a) illustrates how the field profile looks where there is a much higher doping *p*-type (multiplication layer) introduced just at the boundary with the n^+ electrode implant on top of the p^- substrate [109]. Figure 17 b) shows the induced signal on the electrode as a function of time due to the charges moving in this intense field and how this is actually dominated by the motion of the holes in the avalanche being driven away from the electrode (although the signal starts as primary electrons reach the multiplication region). The time resolution depends not only on the signal rise time but also on the ratio of signal to threshold (which influences time-walk), signal/noise (which influences jitter) and the TDC binning [110].

Fast timing already benefits detectors around 200m from the collision points very close to the LHC beam (such as TOTEM [111]) which tag protons emerging intact from the interactions and use the time of arrival to associate these to the correct primary vertex, whose z coordinate has been determined by the central detector (CMS for TOTEM or ATLAS for AFP [63]). However, the main use case for LGADs is envisaged to be for the HL-LHC is to help with the extreme pile-up of 200 superimposed collisions in every 25ns bunch crossing, distributed both in z (σ ~9cm) and time (σ

~200ps). Timing detectors with resolution $\lesssim 30$ps [112] and adequate spatial resolution to associate the correct time to as many tracks as possible will significantly help reduce ambiguities in track-vertex association. Such detectors have been prototyped with the required timing resolution at high gain (~20) and low thickness (50 µm) but radiation hardness issues still require further development for the highest dose regions [113]. The proposed detectors for HL-LHC have pads of mm dimensions, not least to avoid having too significant an area where tracks can pass between electrodes giving degraded timing resolution, but the long term goal would be truly 4D detectors with pixel spatial resolution as well as <20ps time resolution [114]. The challenge is minimising the regions between pixels (where there is no multiplication layer) and keeping the thickness much less than the pitch.

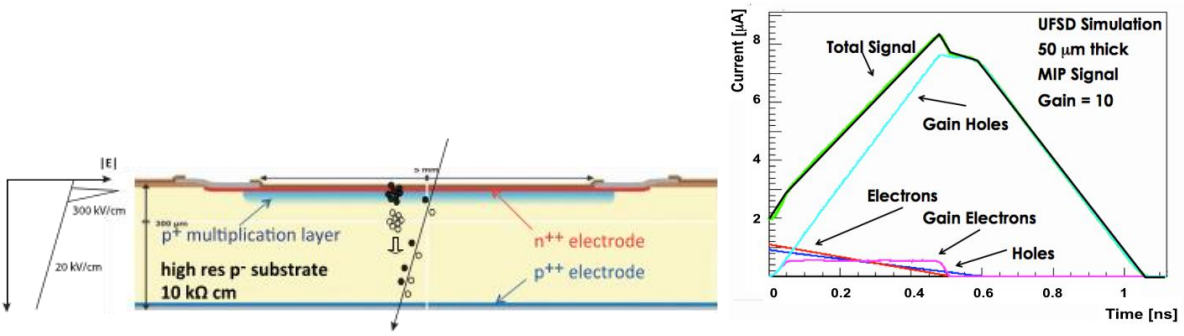

Figure 17 a) Design of a Low Gain Amplification Detector (LGAD) and b) Signal Formation with Time. Figure reproduced from Ref. [9]

Figure 18 shows how achieving the required gain for fast timing requires increased voltage after irradiation but this is also sensitive to small changes in processing parameters. The loss of gain is understood to be due to acceptor removal in the multiplication layer. RD50 is also looking at defect engineering solutions to radiation hardening either with interstitial carbon or using gallium instead of boron as the dopant [113]. The main challenges for this technology are therefore now addressing the worst case HL-LHC irradiation regions (down to radius of 12cm at ±3.5m each side of the interaction point in ATLAS, for example) where the fluence will exceed the $10^{15} n_{eq}/cm^2$ range. Having part of the system replaceable after several years of operation will help with this issue.

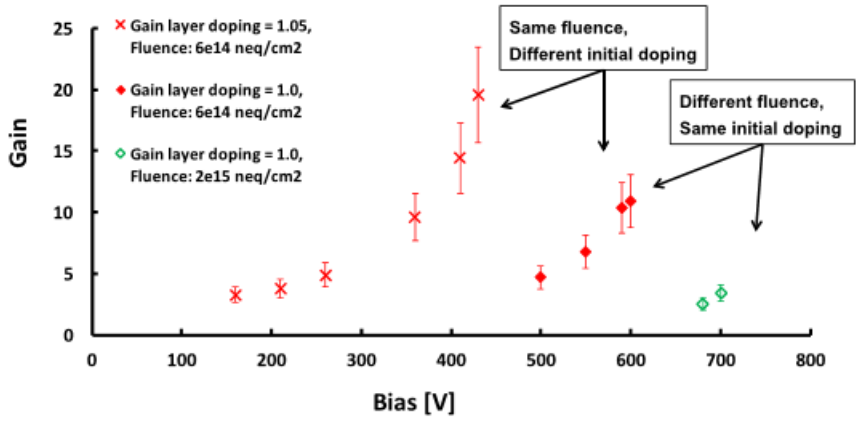

Figure 18 Gain after irradiation as function of operating voltage for 50µm thick LGAD showing how a 5% increase in gain layer doping can greatly improve performance after irradiation. Figure reproduced from Ref. [113]

2. Active Hybrid Sensors

For many reasons high resistivity silicon has emerged as the substrate of choice for solid-state tracking detectors and, with commercial microelectronics nearly all realised on silicon, it has long been a dream to integrate the sensor and electronics into a single monolithic device. However, there can be significant advantages in incorporating aspects of the electronics (for example aspects of the analogue circuit) in the sensor while retaining a hybrid approach to not give up the advantage of high density commercial microelectronics technology for the digital processing.

2.1. DepFETs

These detectors combined both the amplification capabilities of a Field Effect Transistor with possibility for charge storage beneath the FET structure. As lateral depletion due to a separate substrate contact drives a depleted region beneath the FET, a potential minimum is created for majority carriers within the bulk. Rather than drive charge along this potential valley to be collected at the substrate contact, the electrode potentials can be set to store the charge beneath the FET structure such that the FET conductance becomes a function of the stored charge, allowing a drain current, proportional to the charge, to be read out non-destructively, in that the charge is not disturbed by the read out [3]. A pixel array can be created with a grid of external lines to contact the source, gate, drain and clear of Figure 19. The source, gate and drain voltage control which pixel transistor is turned on, so each pixel can be addressed individually in sequence (or any chosen order) to read out the array. Further flexibility is provided by the possibility to turn on groups of transistors in turn to do a crude sweep to find a region of interest and then, because the signal is stored, to read out just that region in detail before issuing a clear [115]. Of course, there is also the need to issue a clear from time to time to remove the stored signal.

DEPFET detectors offer an excellent signal/noise, low power and flexible read-out with microelectronics control chips at the periphery, such that the sensitive volume of the array can contain minimal material. The technology is not well suited to high radiation environments and suffers from bandwidth limitations for very high data rate applications. However, the potential to minimise the thickness and therefore further reduce scattering material, while retaining good signal/noise, has led to application at the SuperKEKB upgraded Belle-II experiment [116].

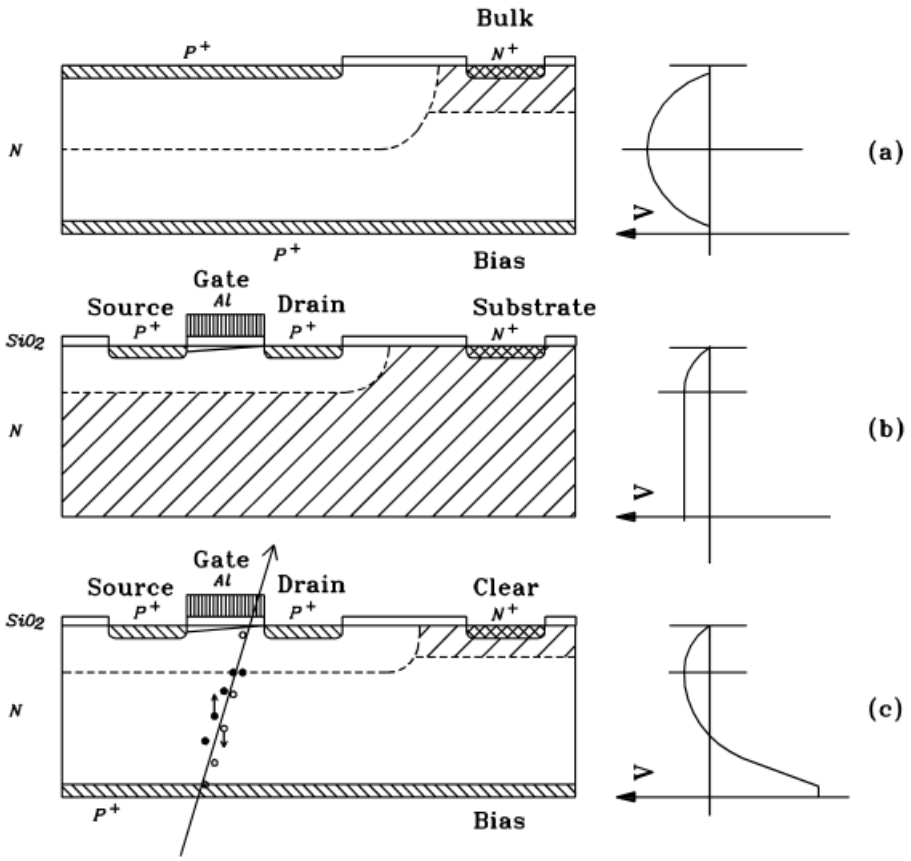

Figure 19 DEPFET Working Principle: a) sideways depletion (as used for drift detectors) with depletion valley; b) FET structure and c) both combined. Figure reproduced from Ref. [3]

2.2. CMOS Pixels

The monolithic CMOS Imaging Sensor (CIS) discussed in Section 3.3, do not currently allow readout with the full sophistication of the 65nm CMOS ASICs discussed in Section 1.2.3, needed for the highest hit data storage capabilities and output bandwidths presented in Table 2. However, if the initial amplification and shaping analogue functionality is implemented in a separate CMOS sensor chip, its output, as a voltage signal, can be coupled into a separate readout chip through a capacitive connection. Since the sensing chip can use widely available and inexpensive CIS technologies and the coupling can be achieved by a glue layer or similar, also at lower cost than the high density bump bonding technology, this can provide a cost effective hybrid pixel option [117] but the precision alignment of sensor and ASIC still requires use of sophisticated flip-chip technology.

3. Monolithic Silicon Detectors

3.1.CCD and CCD-inspired Detectors

One of the most important designs of imaging detector is the Charge-Coupled Device (CCD) invented in 1969 at Bell labs [118]. The “conventional” three-phase design has a MOS structure in each pixel where the gates from consecutive pixels are each connected to external lines. A biased substrate contacts a thin epitaxial layer with a front diode contact giving a depletion region with potential depth influenced by the MOS gate voltage. Minority carriers produced by light or a charged particle are

stored at the potential minimum below the gate. Every third gate down a column is connected to the same clocked pulse and the pattern of pulses is designed to sweep the charge to the end of the column. For any pixel storing charge, first it sees the potential below the next pixel down the column brought to the same level while the potential for the pixel before it down the column is kept high, then the potential for the pixel where the charge is stored is raised, emptying the charge into the next cell down the column. The pattern for the three potentials repeats and after each cycle the charge has been moved a further cell down the column [3]. This mechanism is used to move the charge to the bottom of the column where it is transferred into a readout register. The same mechanism can also be used to transfer the charges in the readout-registers out through a single amplifier. A vital figure of merit is the charge transfer efficiency, which with judicious design can be greater than 99.999% [119]. Given the capacitance is determined by that at the node of the single amplifier the noise can be very low, while the fact that all pixels can be read out through the same amplifier gives unprecedented uniformity of response, a key consideration in the continued popularity of CCDs in scientific instrumentation, particularly for space and astronomy.

For particle physics, the slow frame rate is an issue and the response uniformity less essential, leading to designs with multiple read-out of directions for both the CCD and the read-out register [120] [119]. For Linear Collider applications, the LCFI collaboration proposed a column parallel readout with a separate chip to process data directly from each column [121]. Other concepts take advantage of Linear Collider time structures (with trains of particle bunches and then significant periods (tens of ms or more) without collisions. The CCD structure can be exploited for in-pixel charge storage for different time bins during the bunch train collisions and then read-out between bunch trains [119].

An alternative to in pixel storage for the ILC is to exploit the very high granularity available for CCD technology. The Fine Pixel CCD (FPCCD) proposal (see [122]) has 5µm × 5µm pixels with 10Mpixel/s read-out between bunch trains through 16 outputs addressing different regions [122].

3.2. Silicon on Insulator Detectors and 3D Integration

Another way to make it easier to optimise the substrate and microelectronics separately is to use wafer bonding technology that is standardly used in industry, potentially allowing access to smaller feature size CMOS and allowing better isolation of the microelectronics circuitry from the substrate than is possible with the MAPS devices discussed in Section 3.3 [123]. Figure 20 a) shows a detector cross section with electronics fully insulated from the detector substrate and the transistors isolated from each other by trenches. Conducting vias penetrate both the electronics layer and the isolation layer to contact implants in a depleted substrate which then acts as the sensing medium. Such stacking technology is also leading to novel ways to greatly increase the electronics density in a microchip through 3D integration (see Figure 20 b)). 3D integration technologies are employed in commercial microelectronics to greatly increase memory chip component densities and (more recently) for imaging applications (see for example [124]). This approach, which reduces distances between active components and therefore improves speed and power losses in conductors, is becoming more affordable but typically targets large volume markets. Nevertheless, ASICs for particle physics and

other applications are being explored with analogue and digital functionality separated into different layers [125].

The SOIPIX programme [123] is using these technologies in monolithic sensor designs of the type illustrated in Figure 20 a) to target ILC and space applications. For more severe radiation environments, the effects of charge trapping in insulators and at interfaces can lead to radiation hardness issues that require further developments. The benefit of through silicon vias (TSVs) for any monolithic or hybrid pixel sensor, in terms of connectivity on the back of the read-out, give this technology many attractions for particle physics and many other application areas. However, the requirement of high yield (and hence cost effectiveness) still needs to be fully addressed in designs for particle physics.

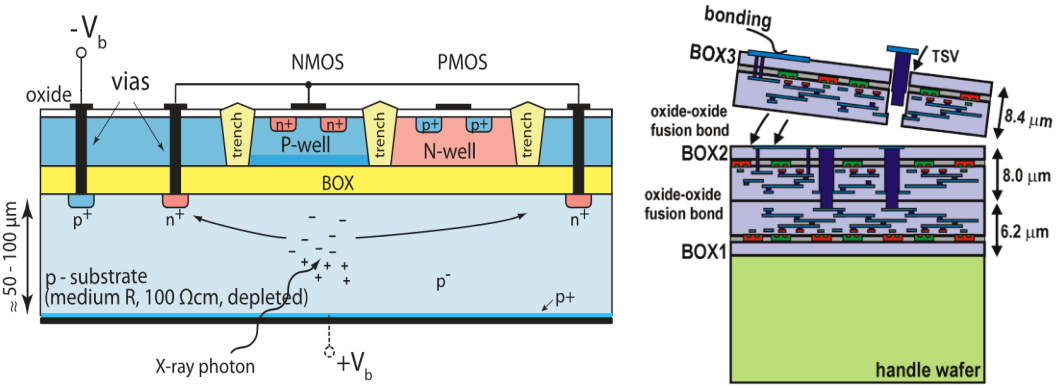

Figure 20 a) Silicon on Insulator (SoI) Detector Concept and b) 3D integration of microelectronics. Reproduced from Ref. [9]

3.3. Monolithic Active Pixel Sensors (MAPS)

Just as the development of commercial CCDs as imaging sensors led to exciting developments for particle physics (see Section 3.1), so the huge growth of CMOS Imaging Sensors (CIS) has from its very beginnings seen parallel developments in tracking detector concepts exploiting this technology [126]. Given the ubiquitous nature of cheap cameras using CIS technology (particularly in mobile phones), a key driver has been to see if commercial processing technologies can result in suitable sensors for particle physics [127]. The economies of scale in manufacturing lead to costs which are a fraction of those for hybrid detectors and are highly competitive per unit area with those for strip detectors [128]. However, the most widely available CIS do not require an electric field within the sensing volume and collect charge mostly by diffusion, making signal speed too slow and sensitivity to carrier lifetime reduction with radiation too high for many applications.

3.3.1. Diffusion Dominated Charge Collection

Although initially developed for the ILC, the first particle physics applications of MAPS technology was at the RHIC heavy ion collider [129]. However, the most ambitious project to date, with 10^{10} pixels of 30µm × 30µm pixels covering 10m^2, is for the ALICE (heavy ion) Inner tracking System at the LHC [130] due for installation by the end of this decade. Figure 21 a) illustrates the design and operation of this detector. Electron hole pairs produced in a 25µm thick > 1kΩ cm p-type epitaxial layer diffuse through the substrate until the electrons reach the depletion around the *n*-well diode contacts. Full CMOS is achieved by having a highly doped deep *p*-well under the PMOS transistor whose *n*-well substrate would otherwise act as a charge collecting node [131]. A few volts back bias ensure the depletion

extends partially into the epitaxial layer giving a design that gives good efficiency and very low nose hit rate for charged particle detection over a range of threshold settings even after irradiation to 3.5kGy and $1.7\times10^{13} n_{eq}/cm^2$, as shown in Figure 21 b).

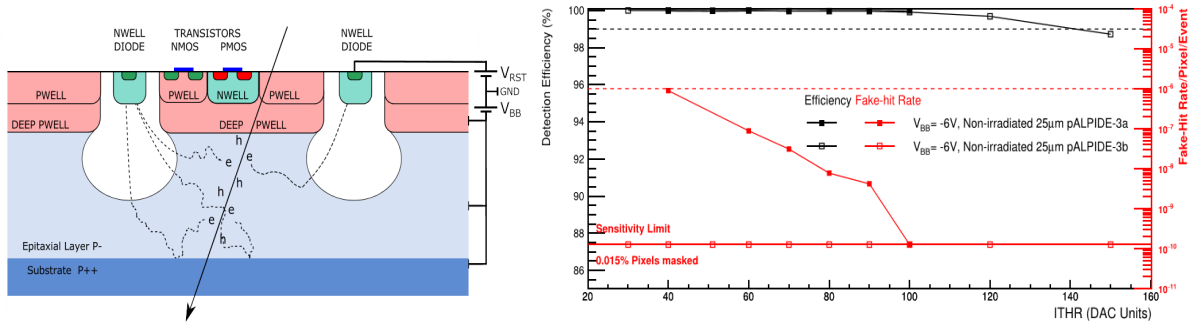

Figure 21 a) Schematic of the ALPIDE MAPS for the ALICE ITS upgrade and b) measured radiation tolerance in terms of detector efficiency (black) and fake hit rate (red) as a function of the pixel threshold. Both panels are reproduced from Ref. [130]

3.3.1.1. Characteristic Readout and Performance

A typical charge collection time by diffusion alone of ~120ns (see for example [132] for 15µm cells on an 8µm epitaxial layer) represents both a potential issue for high speed operation and a limitation in terms of radiation tolerance due to trapping resulting from bulk damage (see Section 1.2). The expected mean signal for a minimum ionising charged particle can be as low as $63e^-h^+$ pairs/µm for thin sensors [133] (given the average 3.68eV deposited energy to create each pair). This means that with a sensitive (epitaxial) layer thickness in the range 10-25µm, for good signal /noise, the noise should ideally be in the tens of electrons (ENC) range, even allowing for the fact that usually some signal from the substrate also contributes.

Detectors which rely on charge mostly produced in the epitaxial layer can be used to build very low mass arrays (for example the ALPIDE inner silicon sensors are back thinned to 50µm and each complete module layer is only 0.3% of a radiation length, X_0 [130]). Depending on the minimum feature size of the technology and the required in-pixel circuit complexity, pitches matching the epitaxial thickness can be achieved, approaching the goal of a symmetric 3-dimensional sensing voxel with greatly reduced sensitivity of signal to incident track angle. Better than 5µm resolution, <300mW/cm^2 power density (albeit with 30µs integration time) and respectable radiation hardness have now been demonstrated with this technology [130].

3.3.1.2. Radiation Limitations

The LHC proton-proton experiments at the HL-LHC have requirements for their innermost pixel layers which go a factor 1500 [9] beyond those of the ALICE heavy ion programme. Every collision, at 25ns bunch crossing time, needs to have signals above threshold measured and stored until an external trigger signal identifies which events should be read out. The first step towards meeting such requirements is to greatly reduce the charge collection time in the pixel and to increase the front-end electronics response time. The former is achieved with designs that create a field within the detector so charge collection takes place primarily by drift rather than diffusion (see Section 3.3.2. Designs with short collection distances should then be less prone to trapping, but the other effects of irradiation, both to the circuitry (Total Ionising Dose) and to the substrate (increased dark current, effective doping changes due to bulk damage) need to be designed against. Cold operation helps as for hybrid sensors (see 1) but changes in effective doping are seen, which at relatively low doses is initially

attributed to an effective acceptor removal. Figure 22 shows that over a wide range of initial p-type doping concentrations, the final effective dopant concentration after about $10^{15} n_{eq}/cm^2$ is $N_{eff} \approx 10^{14} cm^{-3}$ ($\rho \approx 100 \Omega cm$) [9].

Finally, the effects of TID are heavily circuit and technology dependent but manifest themselves first in changes to noise and gain which do deteriorate in devices studied so far. Probably for higher doses, in the several MGy range, some of the same issues that beset CMOS hybrid sensor electronics could also limit the applicability of currently available technologies.

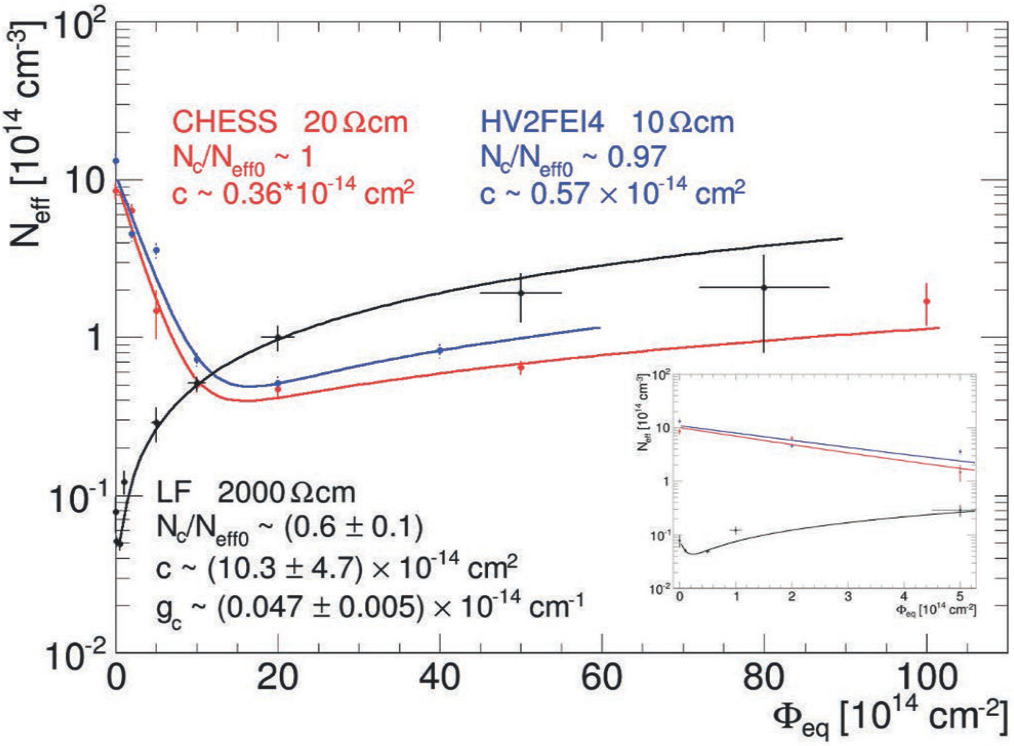

Figure 22 Effective doping concentration variation with neutron fluence for materials with starting resistivities from 10Ωcm to 20kΩcm. Figure reproduced from Ref. [9].

3.3.2. Drift Dominated Charge Collection (Depleted MAPS)

Figure 23 illustrates how the deep *n*-well detector design works with the well containing the electronics providing the diode contact to a high resistivity substrate that can deplete to depths >100µm as for a hybrid sensor, giving a corresponding high signal [134]. Furthermore, for low doses the effective acceptor removal with dose even increases the resistivity (see Figure 22) and hence the signal for a given operating voltage even increases with dose at first.

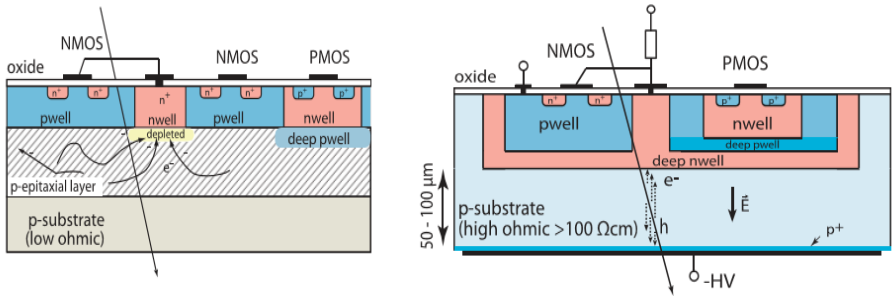

Figure 23 a) CMOS Imaging Sensor and b) HV-CMOS design. Figure reproduced from Ref. [9]

3.3.2.1. Large Well Designs

The first DMAPS designs followed the design of Figure 23 b) with depletion depths at low irradiation fluences penetrating over 100µm into the substrate giving signals of order 7000e$^-$ as well as an excellent fill-factor in terms of charge collection anywhere in the pixel area (see Figure). Signal/noise and timing accuracy depend on the capacitance seen by the front-end circuit in each pixel which is larger (~100fF) for these designs. 99.7% track efficiencies after irradiations to $10^{15}n_{eq}/cm^2$ are achieved with this technology but with slightly less efficiency if the requirement to be recorded in the correct 25ns time bin is imposed [9]. The depletion depth and hence sensitive volume is proportional to $\sqrt{V/N_{eff}}$ so a given signal/noise typically requires a larger depletion depth in the presence of larger noise. Most prototypes for high radiation environments use this technology which is available with several vendors and a proposal has been considered in ATLAS [135] to use DMAPS designs for the highest radius pixel layer in the tracker upgrade, which is both the lowest in dose and largest in area giving potentially greatest benefit from exploiting the cost savings with CMOS sensors.

3.3.2.2. Small Diode designs

The alternative, low fill-factor, designs have much smaller collecting diodes outside the well structure containing the electronics and therefore typical capacitance values of ~10fF seen by the front-end circuitry giving lower noise [9]. This allows a good signal/noise, and hence high efficiency for a given threshold, even though the signal is smaller as mostly produced just in the epitaxial layer. (The threshold is set as in Figure 21 b) to suppress the noise hit rate.) This gives a sensitive volume which does not vary with dose and a better approximation to the voxel concept discussed above. Because of the thin collection region, signal produced below the diode is collected very quickly. However, the problem is when charge is produced in the region beneath the CMOS electronics (see Figure b)) where charge collection due to the weak field can be both slow and inefficient. A recent significant technology development (illustrated in Figure c)) allows a shallow n^- layer contacting the n^+ node to be realised above the lightly doped p^- epitaxial layer. The depletion region once a voltage is applied between the n^+ node and the back grows from the n^- p^- junction, giving the possibility of full depletion and an electric field over the full region of the pixel. With -6V substrate voltage, the signal before and after irradiation to $10^{15}n_{eq}/cm^2$ is effectively unchanged at around 1740e$^-$ (as expected for full depletion) with fast charge collection only rising from 16.7ns to 19ns after irradiation [136]. The signal/noise ratio after $10^{15}n_{eq}/cm^2$ for 30µm×30 µm pixels is also excellent at 39:1. As with the large well designs, performance and limitations at $10^{16}n_{eq}/cm^2$ still need to be explored further.

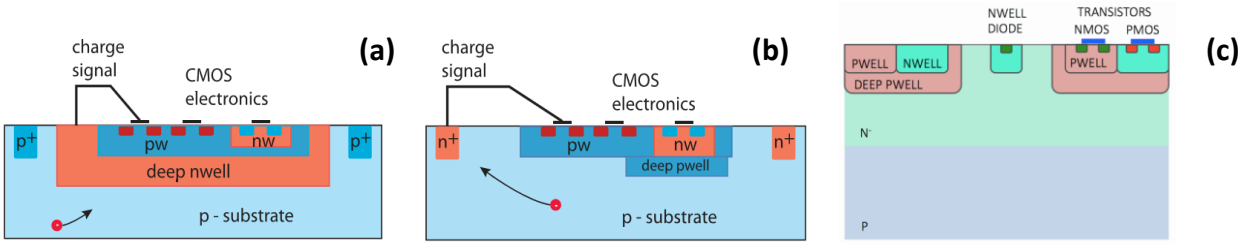

Figure 24 a) Large fill factor, b) small fill factor pixel designs and c) small fill factor in modified process. Panels (a) and (b) reproduced from Ref. [9], panel (c) reproduced from Ref. [136]

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