Supplementary Information

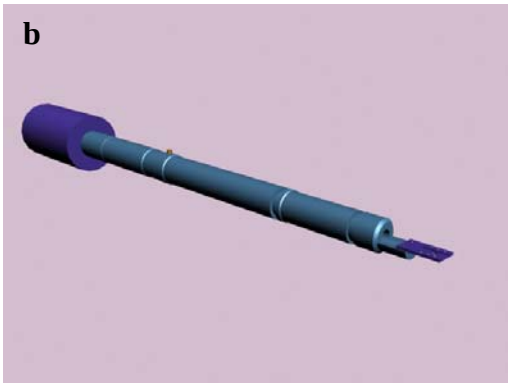
In Situ Imaging of the Conduction Filament in a Silicon Oxide Resistive Switch

Jun Yao[1], Lin Zhong[2,3*], Douglas Natelson[2,4*] and James M. Tour[3,5*]

[1]Applied Physics Program through the Department of Bioengineering; [2]Department of Electrical and Computer Engineering; [3]Department of Computer Science; [4]Department of Physics and Astronomy; [5]Departments of Chemistry and Mechanical Engineering and Materials Science, Rice University, 6100 Main St., Houston, Texas 77005

**To whom correspondence should be addressed. Emails:* lzhong@rice.edu; natelson@rice.edu; tour@rice.edu

1. Home-Built TEM Imaging Stage



c

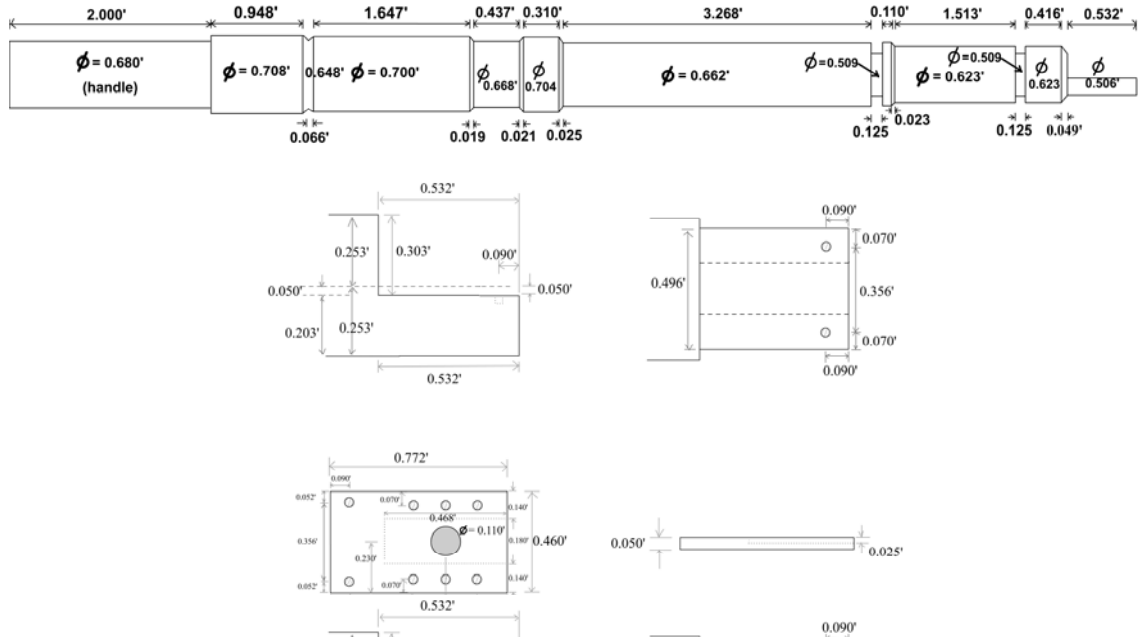


Figure S1. Design of the TEM imaging tool. **a**, The home-built TEM holder (for a JEM-2100F TEM system) that is capable of electrical inputs. **b** and **c**, Schematics of the components of the TEM holder with detailed parameters for each part.

2. Device Fabrication

The multi-stage SiO_x thin-wall structure as shown in Fig. 2 in the main article is fabricated from a silicon wafer (thickness ~ 500 μm) capped with 2 μm thermal SiO_x (x ~ 2) on top. It includes the following steps (Fig. S2):

1. Cr sacrificial mask (~ 400 nm thick) is defined by photolithography. Reactive ion etching (RIE) is then used to define the Si stage as shown in Fig. 2b. The etching depth for the Si stage is ~ 12 μm. CHF_3/O_2 and $SF_6/Ar/O_2$ recipes are used for SiO_x and Si etching, respectively. The Cr mask is then removed by Cr etchant (CEP-200).

2. At 900 ºC, a layer of α-C is grown on top of the defined Si stage by chemical vapor deposition (CVD) method using C_2H_2/H_2 (50/150 sccm).[1] The α-C layer is ~ 20 nm thick with its resistivity ~1-2 KΩ/□. Note that low resistivity is desirable so that the resistance of the α-C electrode is comparatively lower than that of the ON state in SiO_x.

3. RIE (O_2) is performed for selected-area removal of the α-C layer, with photoresist (S1813) as sacrificial mask defined by photolithography.

4. Electrodes (Ti/Au = 5/50 nm, for wire bonding) is then defined by photolithography. Note the selected-area removal of α-C layer in step 3 is to ensure a direct SiO_x/Ti/Au contact for good adhesion during wire bonding.

5. Pt wires that connect the α-C layer and the Au electrodes are defined by electron-beam lithography (EBL). The two Pt wires are separated by ~ 3 μm atop the α-C region.

6. Narrow Cr stripe (~ 140 nm wide, 50 nm thick) between the Pt wires atop the α-C layer is defined by EBL. It serves as the sacrificial mask for SiO_x etching during the definition of the thin-wall SiO_x structure as shown in Fig. 2c.
7. A second Cr mask (~ 40 nm) is defined by photolithography to protect the Au electrodes during SiO_x etching. Note the Pt wires need no protection as they are resilient to the SiO_x-etching recipe.
8. RIE is used to define the SiO_x thin-wall structure with a height of ~ 500 nm (Fig. 2c). Because of undercut, the 140 nm-wide Cr mask eventually results in the width of the SiO_x thin-wall structure ~ 100 nm (Fig. 2d). And the Cr mask is then removed.

The fabricated structure above is then sliced into slim piece (300 μm × 3 mm, Fig. 2a) by a dicing saw. With the height of the SiO_x thin-wall structure ~ 500 nm (Fig. 2c), the width and height of the Si stage ~ 20 μm and 10 μm, respectively (Fig. 2b), the width of the device ~ 300 μm, the fabricated device is expected to have an angle-mismatch tolerance of ~ 0.5 degree for the electron beam. The sliced device is then vertically mounted on a home-built TEM stage (Fig. S1) that is capable of electrical input, and electrically connected through wire bonding. An Agilent B1500 semiconductor parameter analyzer is used for the electrical characterizations. The imaging is carried out on a JEM-2100F TEM system with the beam energy at 200 KeV.

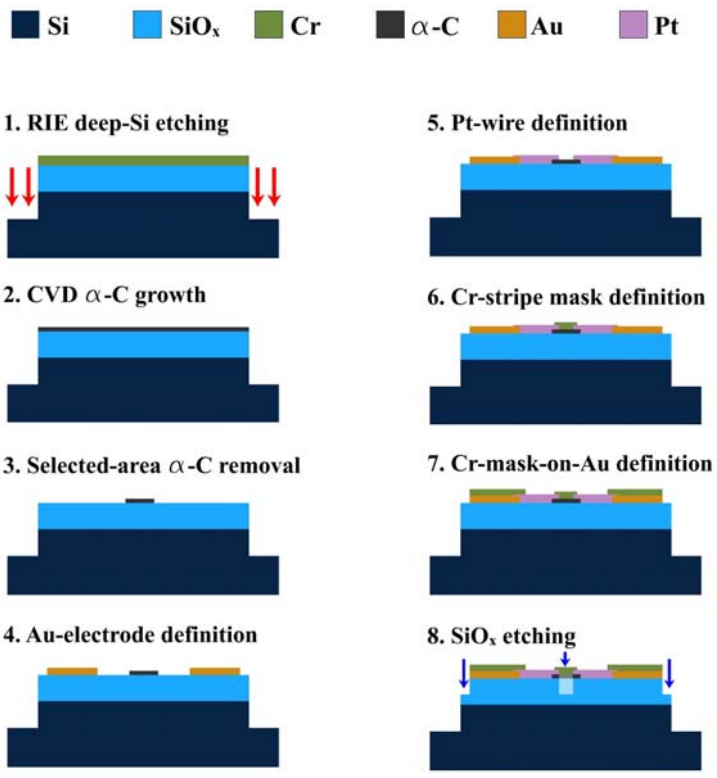


Figure S2. Fabrication flow of the device for the *in situ* TEM imaging device.

3. Switching Behaviors

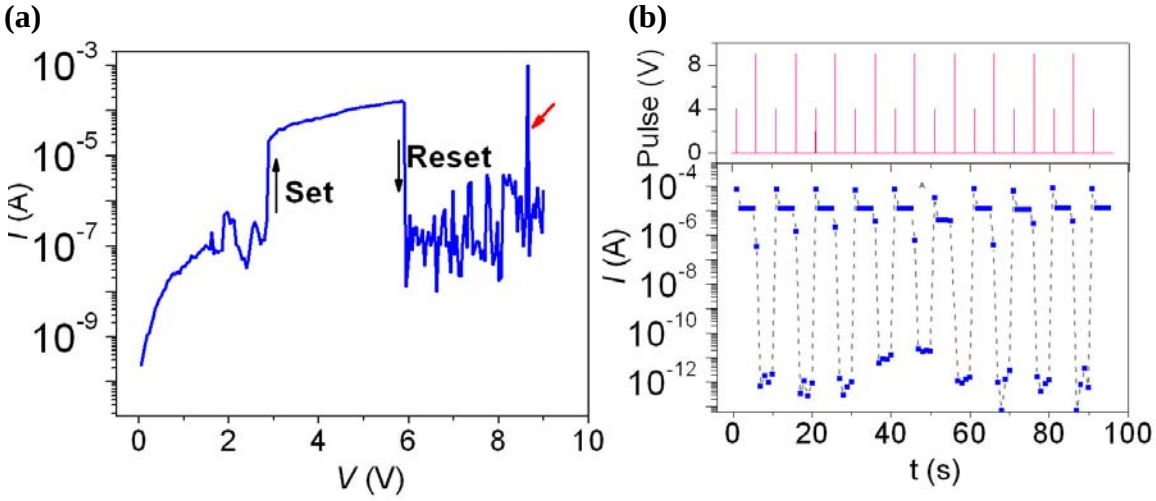
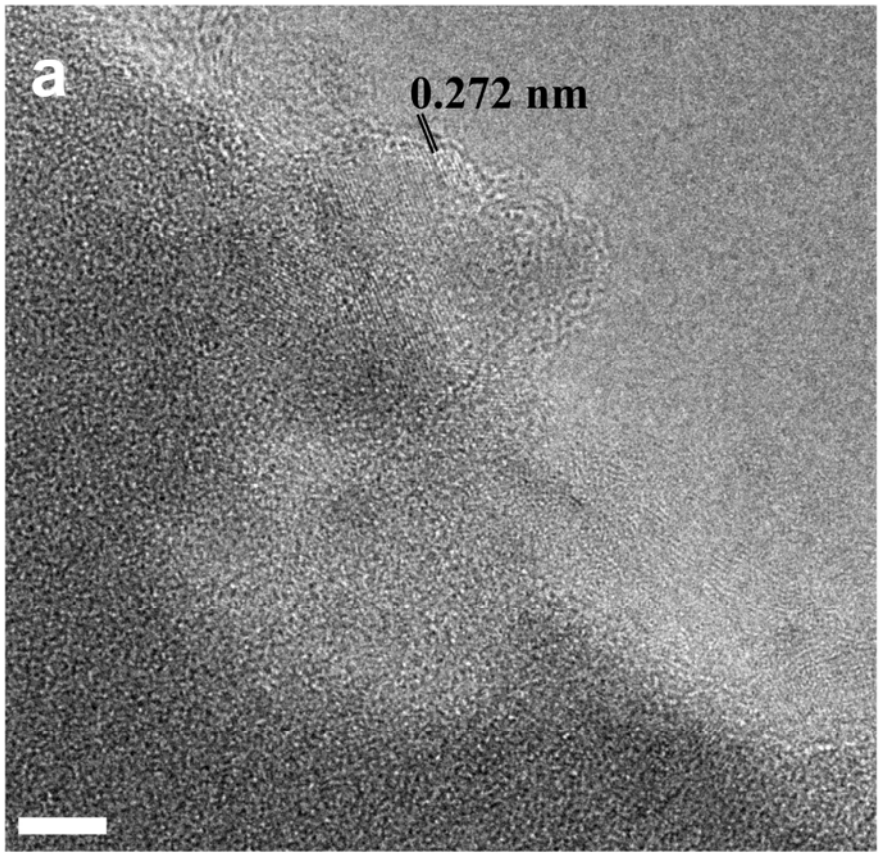


Figure S3. **a**, *I-V* curves from a SiO_x thin-wall device. The red arrow indicates transient ON-state peak in the region $V > V_{reset}$. **b**, (Top panel) A series of voltage pulses of +4 V,

and +9 V serve as set and reset operations, respectively. (Bottom panel) Memory states (read at +1 V) corresponding to the programming operations in the top panel.


a
0.272 nm

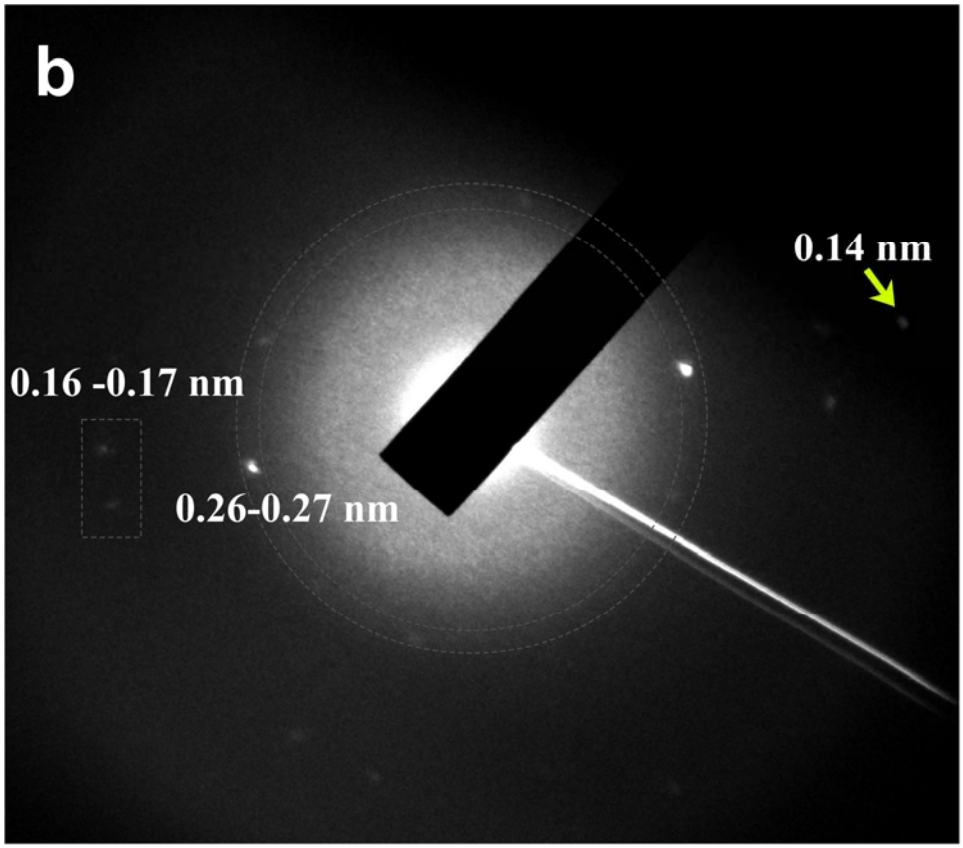
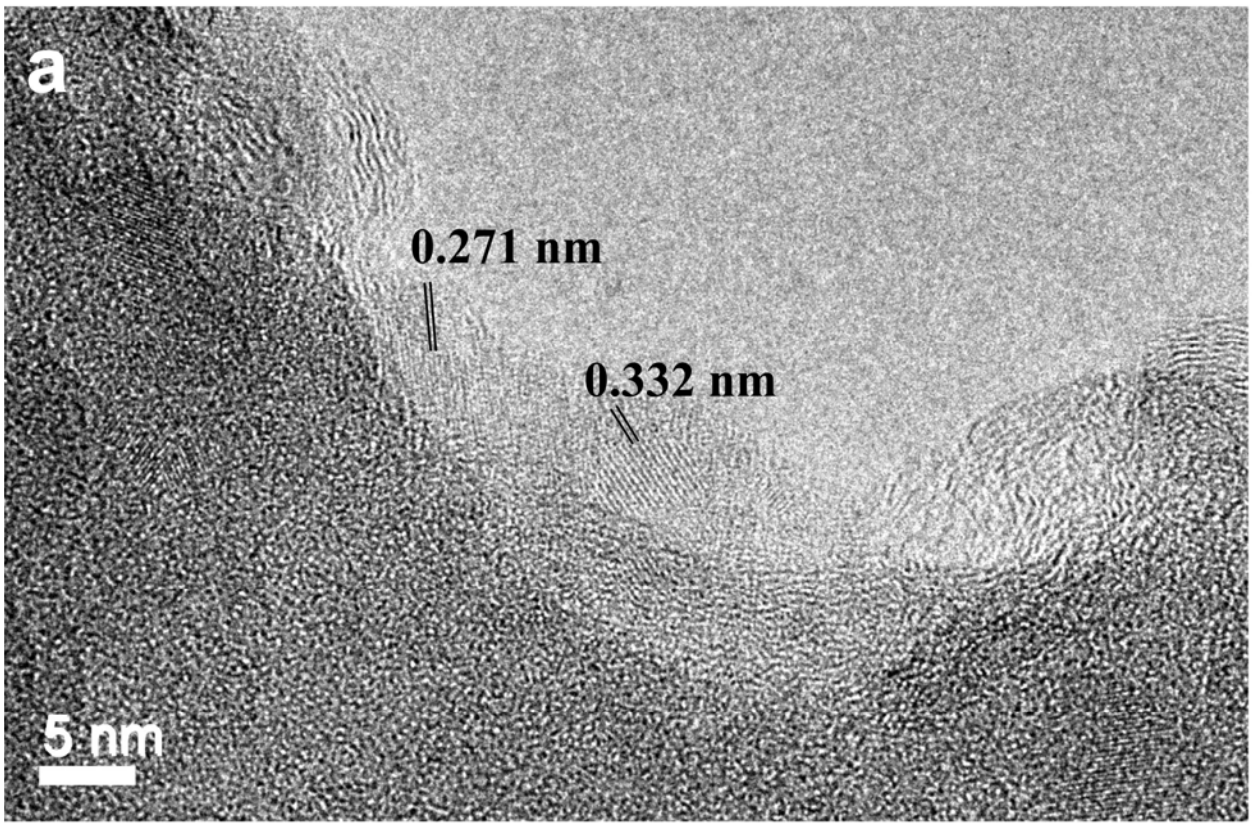

b
0.14 nm
0.16 -0.17 nm
0.26-0.27 nm

Figure S4. **a**, High-resolution TEM image of a third switching nanogap (the first and second are in Figs. 3 and 4, respectively) showing the corresponding selected-area diffraction pattern for the device. **b**, The lattice spacing of 0.27 nm and 0.16 nm and 0.14 nm can be assigned to Si-I (200), (311) and (400) planes, respectively. However, (200) plane is the forbidden plane for diffraction in diamond cubic structure.[2] Instead, it is more reasonable to assign the strong signal at 0.27 nm^{-1} to Si-III/Si-XII phases.[3] The lattice spacing of 0.27 nm and 0.16 nm and 0.14 nm correspond to Si-III (211), (400) and (422) planes.[4,5] More evidence is shown in Fig. S5 below. In additional, the diffraction pattern here is different from those in the SiC forms[5-7] and crystalline silica,[5] ruling out the possibility of all those forms.


a
0.271 nm
0.332 nm
5 nm

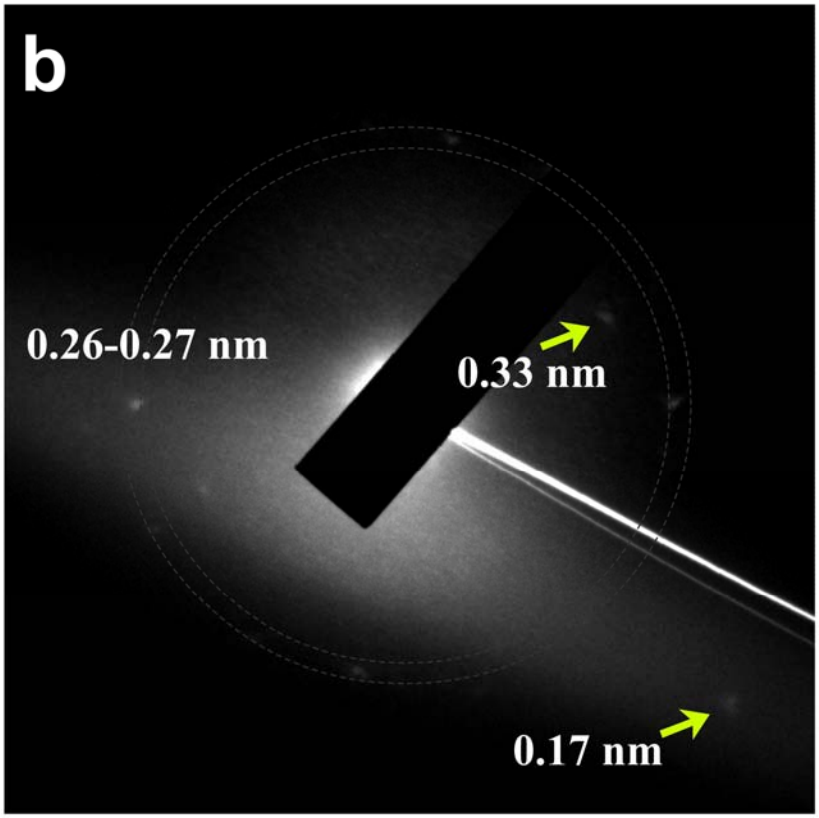

b
0.26-0.27 nm
0.33 nm
0.17 nm

Figure S5. a, High-resolution TEM image of a fourth switching nanogap and (**b**) the corresponding selected-area diffraction pattern. The diffraction pattern here shows similar feature as that in Fig. S4(b). The signal at 0.33 nm^{-1} can only be assigned to Si-III (211) or its closely-related phase Si-XII (11-1).[4] This lattice spacing along with the absence of 0.31 nm^{-1} signal (corresponding to Si-I(111)) further indicates the Si-III/Si-XII phases.

References

1. Li, Y. ; Sinitskii, A.; Tour, J. M. *Nat. Mater*. **2008**, *7*, 966.
2. Colella, R. ; Merlini, A. *Phys. Stat. Sol.* **1966**, *18*, 157.
3. Ge, D.; Dominich, V.; Gogotsi, Y. *J. Appl. Phys.* **2003**, *93*, 2418.
4. Ge, D.; Dominich, V.; Gogotsi, Y. *J. Appl. Phys.* **2004**, *95*, 2725.
5. International Centre for Diffraction Data (ICDD), 2011 database.
6. Sharma, R.; Rao, D. V. S.; Vankar, V. D. *Mater. Lett*. **2008**, *62*, 3174.
7. Jeong, J. K.; Hwang, C. S.; Kim, H. J. *J. Electrochem. Soc*. **2002**, *148*, G526.