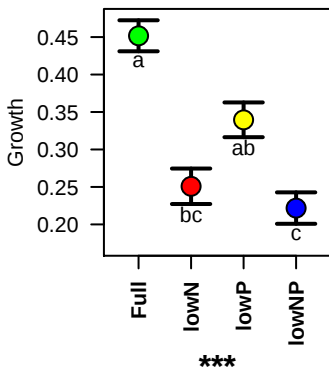
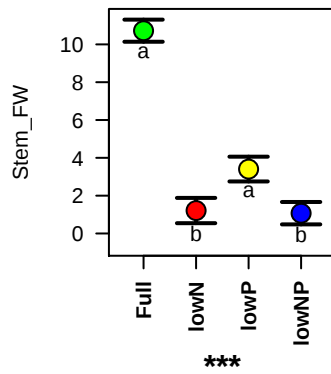


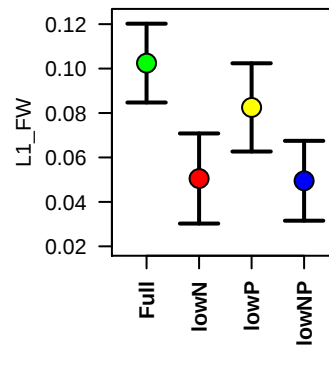
Growth



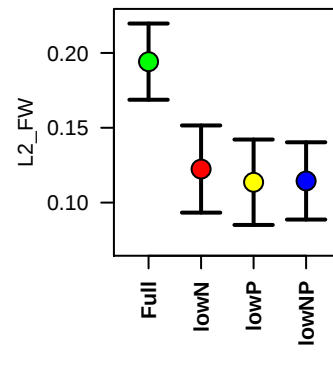
Stem_FW



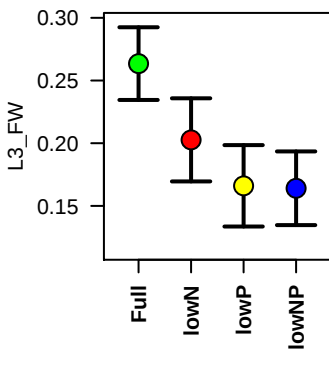
L1_FW



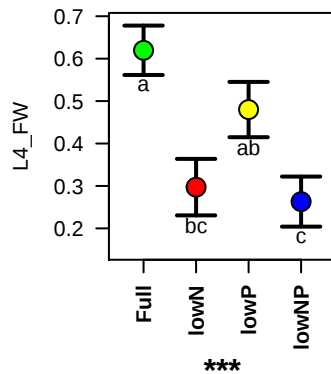
L2_FW



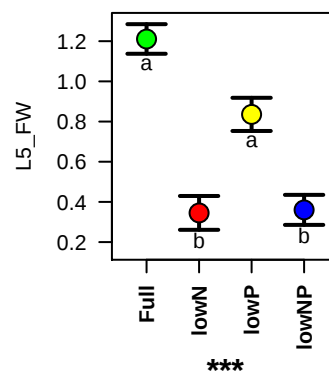
L3_FW



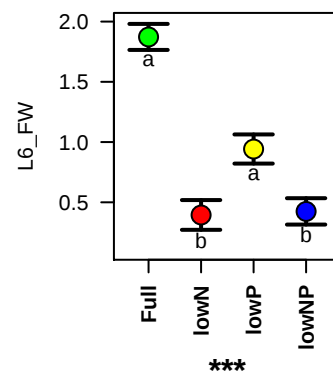
L4_FW



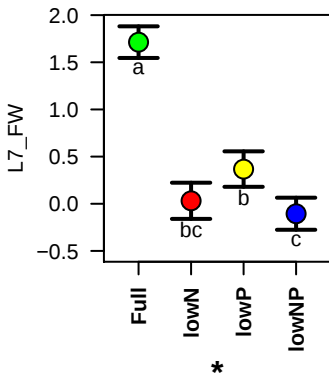
L5_FW



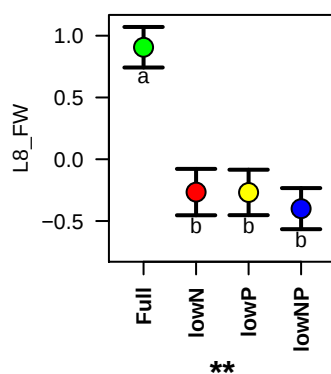
L6_FW



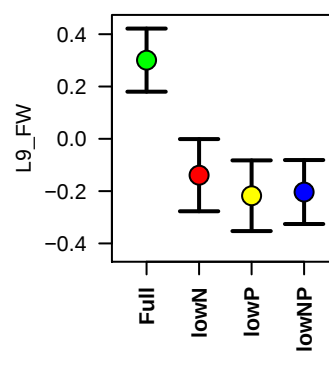
L7_FW



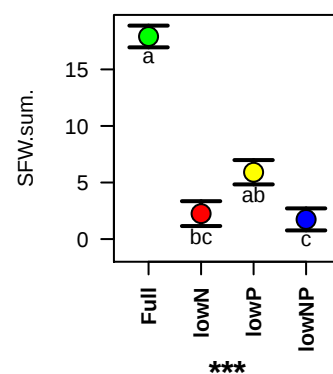
L8_FW



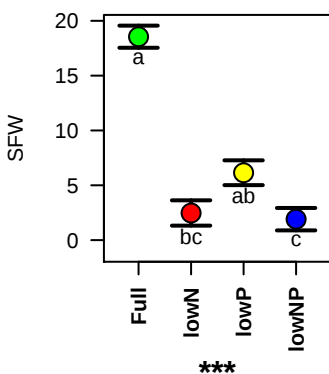
L9_FW



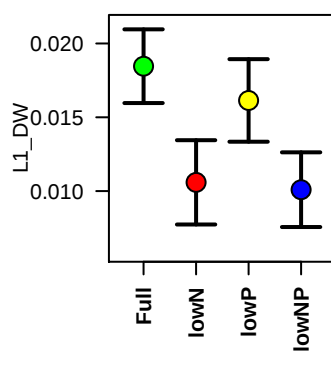
SFW.sum.



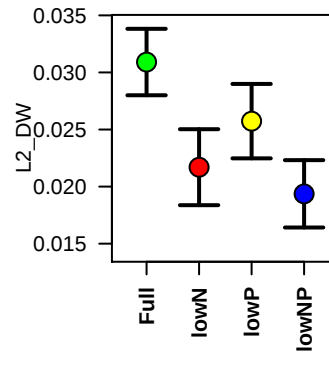
SFW



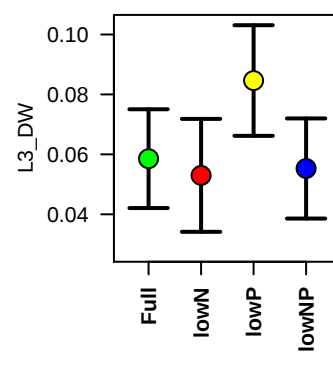
L1_DW



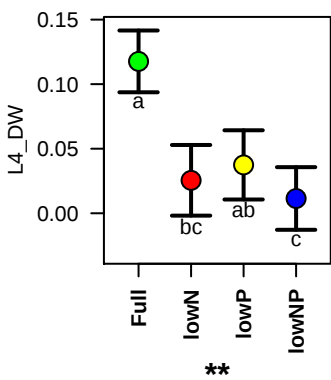
L2_DW



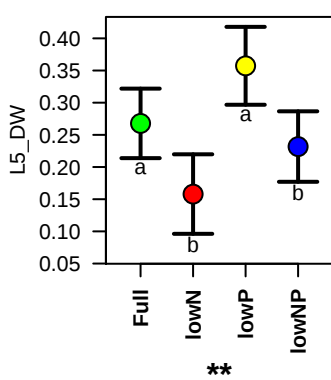
L3_DW



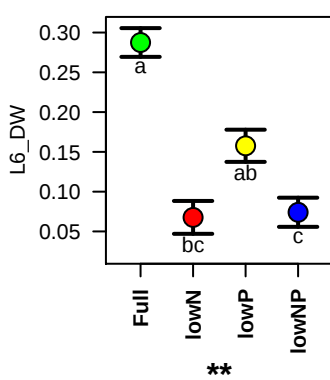
L4_DW



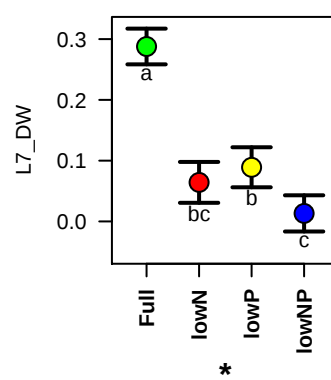
L5_DW



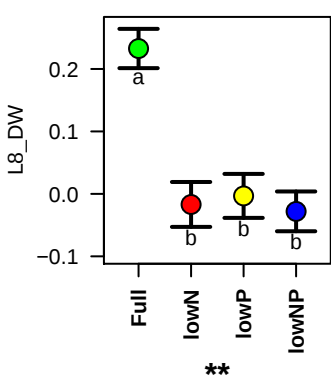
L6_DW



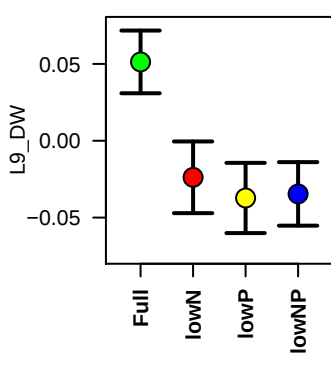
L7_DW



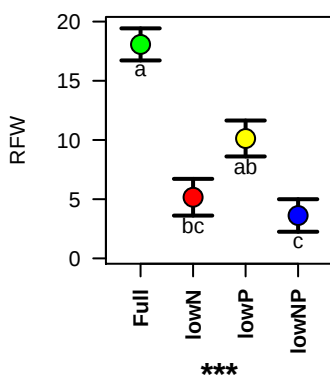
L8_DW



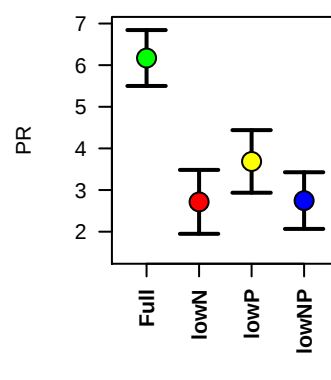
L9_DW



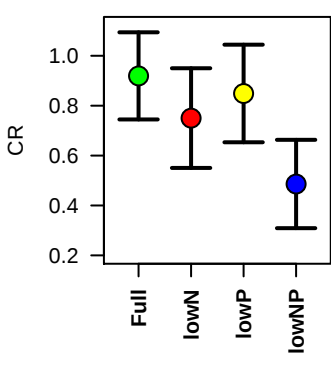
RFW



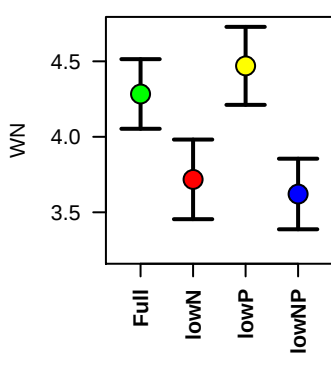
PR



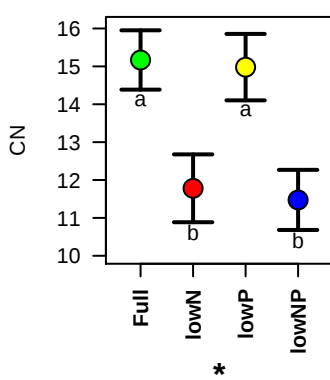
CR



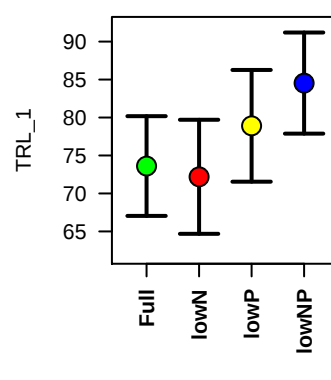
WN



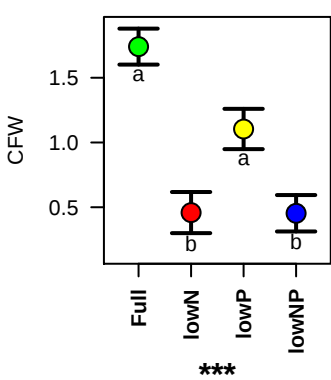
CN



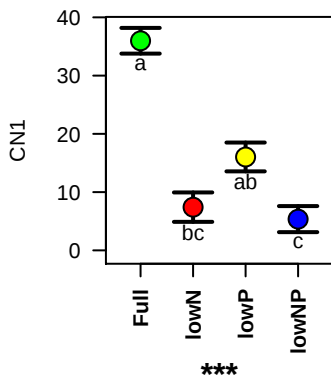
TRL_1



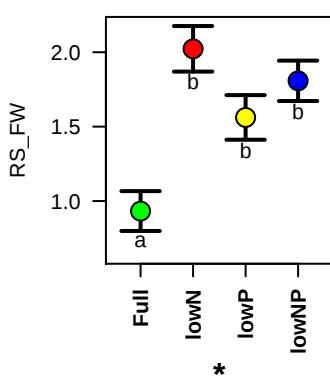
CFW



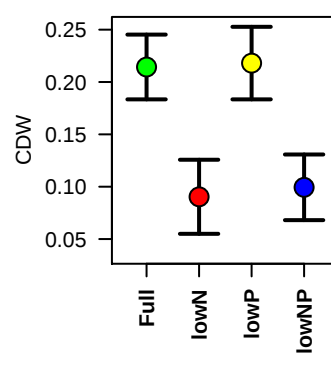
CN1



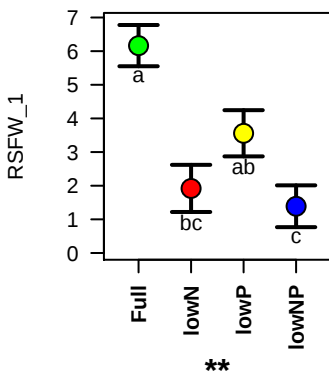
RS_FW



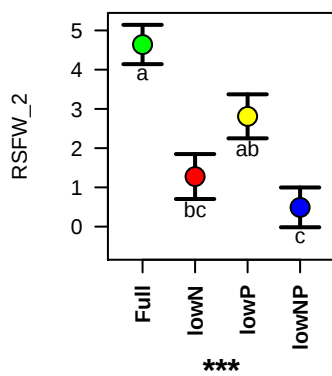
CDW



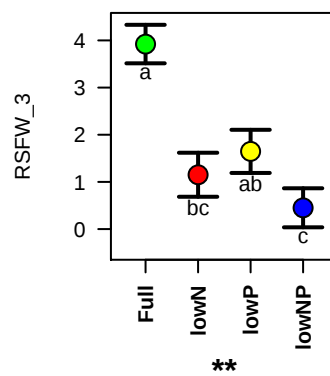
RSFW_1



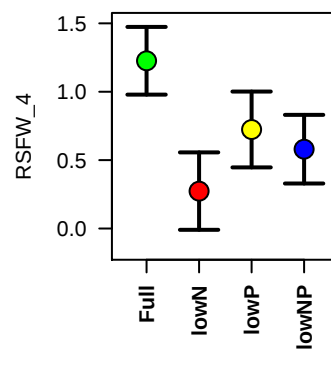
RSFW_2



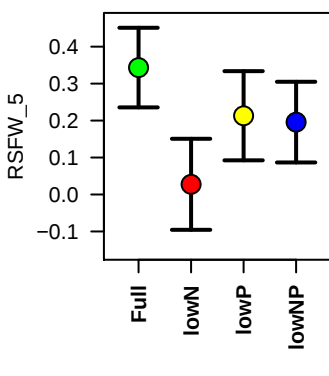
RSFW_3



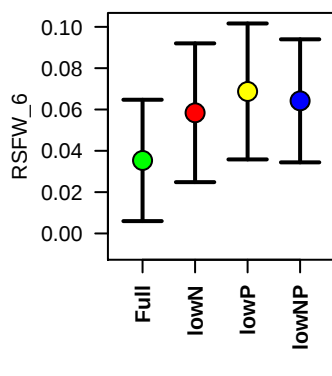
RSFW_4



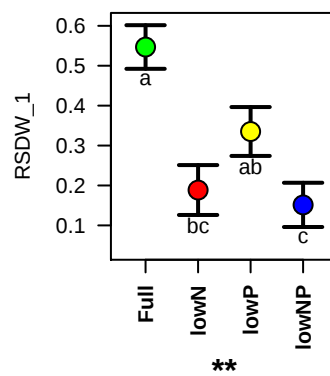
RSFW_5



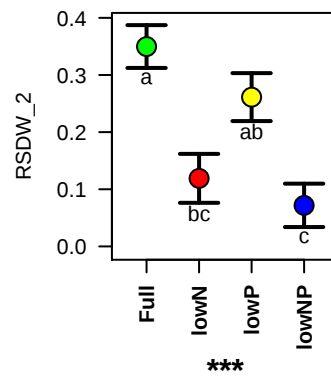
RSFW_6



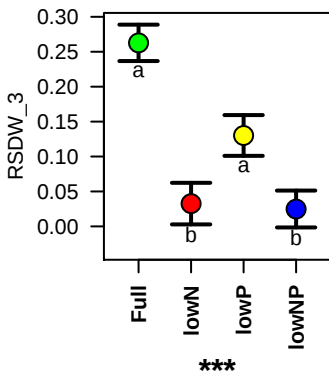
RSDW_1



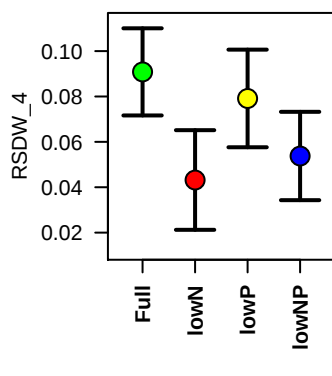
RSDW_2



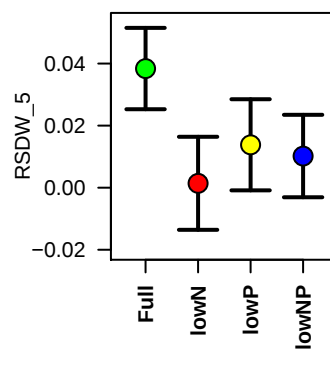
RSDW_3



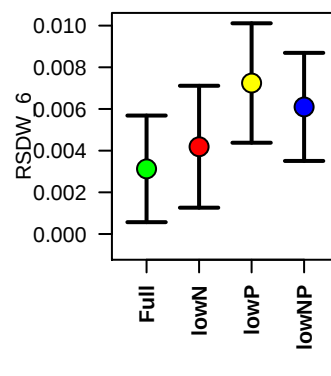
RSDW_4



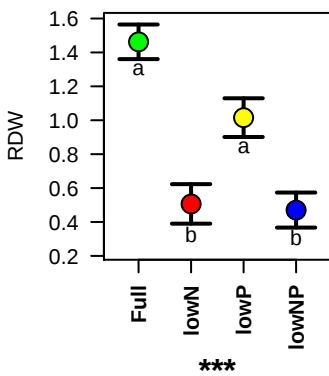
RSDW_5



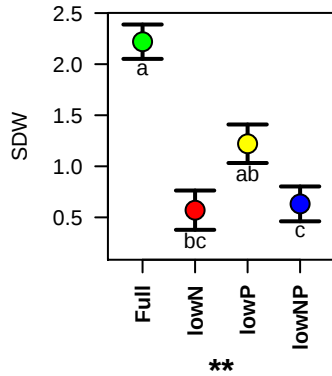
RSDW_6



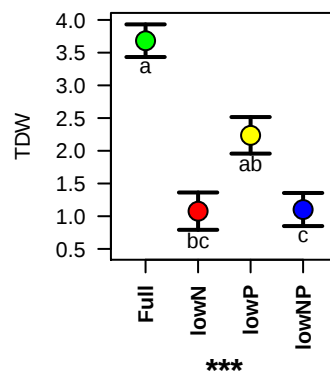
RDW



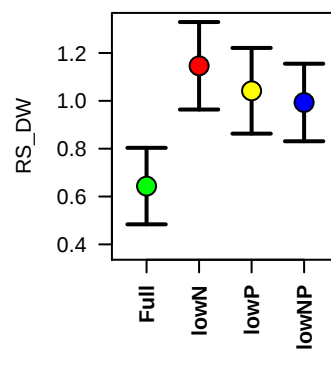
SDW



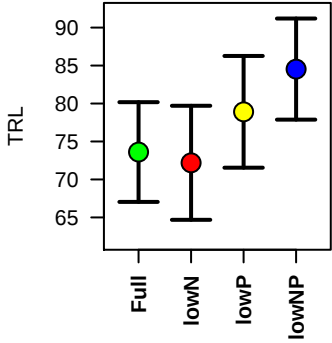
TDW



RS_DW



TRL



SRD

