

Ultra-fast Co-packaged Optical Wireless Link for Wireless-assisted Data Center Interconnection

-Supplementary Information-

Peng Yan^{1,2,3†}, Shenghui Wu^{2†}, Yunhao Zhang^{1,2,3†}, Yu Sun⁴,
Bitao Shen³, Zhen Zhen², Xiaobin Liu², Linshan Yang³,
Qijie Xie², Jun Qin⁴, Lei Wang^{2*}, Haowen Shu^{3,5*},
Xingjun Wang^{1,2,3,5*}

^{1*}Peking University Shenzhen Graduate School, Peking University,
Shenzhen, 518055, China.

²Peng Cheng Laboratory, Shenzhen, 518055, China.

³State Key Laboratory of Photonics and Communications, School of
Electronics, Peking University, Beijing, 100871, China.

⁴Key Laboratory of the Ministry of Education for Optoelectronic
Measurement Technology and Instrument, Beijing Information Science
and Technology University, Beijing, 100192, China.

⁵Frontiers Science Center for Nano-optoelectronics, Peking University,
Beijing, 100871, China.

*Corresponding author(s). E-mail(s): wangl07@pcl.ac.cn;
haowenshu@pku.edu.cn; xjwang@pku.edu.cn;

[†]These authors contributed equally to this work.

1 Supplementary Note I. Modeling of the PCB–bond-wire–chip interface

Figure 2(b) presents the lumped-element model of the electrical interface from the PCB trace to the on-chip I/O node, driven by V_i and observed at V_o . Here, R_s represents the source and PCB trace resistance, while L_{eq} captures the equivalent inductance of the single- or dual-bond-wire interconnect. The PCB pad at the bond-wire landing site

is modeled as a shunt capacitance to ground, $C_{\text{pad,PCB}}$. The EIC input is represented by an effective parallel load ($R_L \parallel C_{\text{total,EIC}}$), where R_L is the on-chip load resistance and $C_{\text{total,EIC}}$ denotes the total capacitance at the I/O node, given by

$$C_{\text{total,EIC}} = C_{\text{pad,EIC}} + C_{\text{esd,EIC}} + C_{\text{in,EIC}}. \quad (\text{S1})$$

The small-signal transfer function is defined as $H(s) = V_o(s)/V_i(s)$.

With the on-chip load impedance $Z_L(s) = R_L/(1 + sR_L C_{\text{total,EIC}})$, circuit analysis yields the exact transfer function in a cubic form:

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{R_L}{\alpha_3 s^3 + \alpha_2 s^2 + \alpha_1 s + \alpha_0}, \quad (\text{S2})$$

where the coefficients are

$$\begin{aligned} \alpha_3 &= C_{\text{pad,PCB}} C_{\text{total,EIC}} L_{\text{eq}} R_L R_s, \\ \alpha_2 &= C_{\text{pad,PCB}} L_{\text{eq}} R_s + C_{\text{total,EIC}} L_{\text{eq}} R_L, \\ \alpha_1 &= C_{\text{pad,PCB}} R_L R_s + C_{\text{total,EIC}} R_L R_s + L_{\text{eq}}, \\ \alpha_0 &= R_L + R_s. \end{aligned} \quad (\text{S3})$$

This system constitutes a third-order low-pass network due to the three independent energy-storage elements: $C_{\text{pad,PCB}}$, L_{eq} , and $C_{\text{total,EIC}}$.

Derivation of the simplified second-order model

To estimate the bandwidth and compare bond-wire configurations, we derive a simplified second-order model. The PCB pad capacitance $C_{\text{pad,PCB}}$ forms a shunt path between R_s and L_{eq} . However, if its reactance magnitude significantly exceeds the driving-point resistance (dominated by R_s) over the frequency range of interest, the signal current bypassed through $C_{\text{pad,PCB}}$ is negligible. This condition is expressed as

$$|Z_{\text{pad}}(j\omega)| \gg R_s \implies \omega R_s C_{\text{pad,PCB}} \ll 1. \quad (\text{S4})$$

For a maximum frequency f_{max} (with $\omega_{\text{max}} = 2\pi f_{\text{max}}$), a sufficient design criterion becomes

$$\omega_{\text{max}} R_s C_{\text{pad,PCB}} \ll 1. \quad (\text{S5})$$

Given the parameters in this work ($R_s \approx 50 \, \Omega$ and $f_{\text{max}} = 40 \, \text{GHz}$), the constraint implies

$$C_{\text{pad,PCB}} \ll \frac{1}{2\pi f_{\text{max}} R_s} \approx 80 \, \text{fF}. \quad (\text{S6})$$

Since electromagnetic extraction of the PCB layout yields $C_{\text{pad,PCB}} \approx 10\text{--}20 \, \text{fF}$, the PCB pad capacitance is treated as a secondary shunt parasitic element in the following reduced-order analysis. To isolate the dominant dependence on L_{eq} , a second-order approximation is obtained by setting $C_{\text{pad,PCB}} \rightarrow 0$ in the coefficients of (S3).

This approximation reduces the interface to a series R_s - L_{eq} network driving the on-chip parallel load ($R_L \parallel C_{\text{total,EIC}}$). The transfer function (S2) then collapses to a second-order form:

$$H(s) \approx \frac{R_L}{C_{\text{total,EIC}} L_{\text{eq}} R_L s^2 + (C_{\text{total,EIC}} R_L R_s + L_{\text{eq}}) s + (R_L + R_s)}. \quad (\text{S7})$$

Normalizing by $(R_L + R_s)$ yields

$$H(s) \approx H_0 \frac{1}{as^2 + bs + 1}, \quad \text{with } H_0 = \frac{R_L}{R_L + R_s}, \quad (\text{S8})$$

where

$$a = \frac{C_{\text{total,EIC}} L_{\text{eq}} R_L}{R_L + R_s}, \quad b = \frac{C_{\text{total,EIC}} R_L R_s + L_{\text{eq}}}{R_L + R_s}. \quad (\text{S9})$$

By matching this to the standard normalized second-order low-pass form

$$H(s) \approx H_0 \frac{1}{\left(\frac{s}{\omega_0}\right)^2 + \frac{1}{Q} \frac{s}{\omega_0} + 1}, \quad (\text{S10})$$

we identify the natural frequency ω_0 and quality factor Q as

$$\omega_0 = \frac{1}{\sqrt{a}} = \sqrt{\frac{R_L + R_s}{C_{\text{total,EIC}} L_{\text{eq}} R_L}}, \quad (\text{S11})$$

$$Q = \frac{\sqrt{a}}{b} = \frac{\sqrt{C_{\text{total,EIC}} L_{\text{eq}} R_L} \sqrt{R_L + R_s}}{C_{\text{total,EIC}} R_L R_s + L_{\text{eq}}}. \quad (\text{S12})$$

This derivation yields the simplified second-order model employed to guide the interface design.

Bandwidth extension enabled by dual bond-wires

The dependence on L_{eq} in (S11) explicitly captures the benefit of using dual bond-wires. In contrast to a single bond-wire with self-inductance L , a dual-bond-wire configuration places two wires in parallel with self-inductances L_1 and L_2 and a mutual inductance $M = k\sqrt{L_1 L_2}$. Positive mutual inductance is assumed for co-routed wires carrying co-directed currents, with the coupling coefficient k typically ranging from 0.1 to 0.3 for practical layouts.

Modeling the dual bond-wires as identical inductors $L_1 = L_2 = L$ simplifies the mutual inductance to $M = kL$. Furthermore, assuming approximately equal current sharing between the two wires, valid for symmetric bond geometries with comparable series resistance and similar return paths, the equivalent inductance seen by the signal current in the parallel combination is

$$L_{\text{eq}} = \frac{L + M}{2} = \frac{1 + k}{2} L. \quad (\text{S13})$$

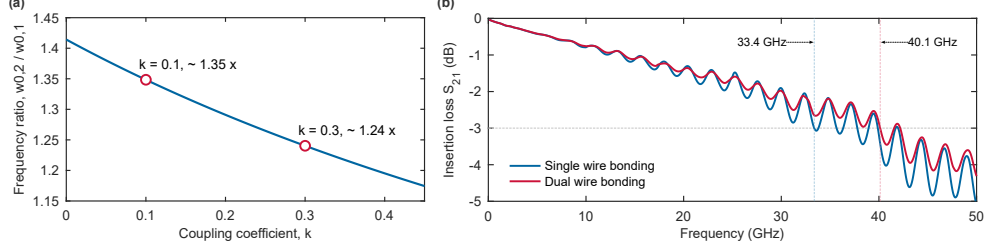


Fig. S1 Equivalent-circuit analysis and electromagnetic verification of the bandwidth extension enabled by dual bond-wires. (a) Calculated natural-frequency ratio $\omega_{0,2}/\omega_{0,1}$ as a function of the coupling coefficient k . The highlighted points correspond to $\omega_{0,2}/\omega_{0,1} \approx 1.35$ and ≈ 1.24 for $k = 0.1$ and $k = 0.3$, respectively. (b) Simulated insertion loss S_{21} of the Ch1 PCB-bond-wire-chip interface for single- and dual-bond-wire configurations under identical interface conditions.

Denoting the natural frequency for a single bond-wire by $\omega_{0,1}$ with $L_{\text{eq}} = L$, and that for a dual-bond-wire configuration by $\omega_{0,2}$ with L_{eq} given by (S13), we obtain from (S11):

$$\omega_{0,1} = \sqrt{\frac{R_L + R_s}{C_{\text{total,EIC}} L R_L}}, \quad \omega_{0,2} = \sqrt{\frac{R_L + R_s}{C_{\text{total,EIC}} L_{\text{eq}} R_L}}. \quad (\text{S14})$$

Consequently, the ratio of natural frequencies is given by:

$$\frac{\omega_{0,2}}{\omega_{0,1}} = \sqrt{\frac{L}{L_{\text{eq}}}} = \sqrt{\frac{2}{1+k}}. \quad (\text{S15})$$

For representative coupling coefficients, $k = 0.1$ and $k = 0.3$, this results in

$$\frac{\omega_{0,2}}{\omega_{0,1}} \approx \sqrt{\frac{2}{1.1}} \approx 1.35, \quad \frac{\omega_{0,2}}{\omega_{0,1}} \approx \sqrt{\frac{2}{1.3}} \approx 1.24. \quad (\text{S16})$$

As shown in Fig. S1(a), replacing a single bond-wire with a dual-bond-wire configuration increases the interface natural frequency by approximately 24%–35% for fixed R_s , R_L , and $C_{\text{total,EIC}}$, providing a first-order indication of the associated bandwidth extension.

The damping behavior is governed by the quality factor Q in (S12). Up to constant prefactors, substituting (S13) into (S12) shows that

$$Q \propto \frac{\sqrt{L_{\text{eq}}}}{C_{\text{total,EIC}} R_L R_s + L_{\text{eq}}}. \quad (\text{S17})$$

While reducing L_{eq} increases ω_0 , its effect on Q depends on the relative magnitudes of L_{eq} and $C_{\text{total,EIC}} R_L R_s$ in (S12). The damping behavior and high-frequency response of the complete interface are therefore assessed using full-wave S_{21} simulation.

The full-wave S_{21} simulation in Fig. S1(b) quantitatively evaluates the Ch1 interface response. Under otherwise identical PCB, pad, and chip-loading conditions, the simulated 3-dB bandwidth increases from approximately 33.4 GHz for the single-bond-wire configuration to approximately 40.1 GHz for the dual-bond-wire configuration, corresponding to a practical improvement of about 1.20 $\times$. This simulated bandwidth improvement is slightly smaller than the natural-frequency ratio predicted by the simplified lumped model, as the full-wave simulation captures distributed interconnect effects, conductor and dielectric losses, pad discontinuities, and non-ideal current sharing between the two bond wires. In addition to the bandwidth extension, the dual-bond-wire configuration exhibits reduced high-frequency ripple and less pronounced insertion-loss notches, resulting in a smoother high-frequency interface response.

Overall, the analytical model and full-wave electromagnetic simulation consistently indicate that dual bond-wires can reduce the effective interface inductance, extend the interface bandwidth, and maintain a smooth high-frequency response without pronounced resonant peaking.

Supplementary Note II. VNE tap-length trade-off

The tap lengths of the Volterra nonlinear equalizer (VNE) are selected based on a performance–DSP-power trade-off. As shown in Fig. S2, increasing the Volterra tap length initially improves the BER for both NRZ and PAM-4 signaling. For NRZ, the BER improvement becomes limited beyond approximately 20 taps. For PAM-4, the BER continues to improve with tap length, but the improvement becomes less pronounced beyond approximately 40 taps. These results indicate that further increasing the memory length provides diminishing BER improvement once the selected tap lengths are reached.

In contrast, the estimated DSP power increases continuously with tap length, as shown in Fig. S3. The estimated DSP power was obtained from hardware-power monitoring during offline VNE processing using HWiNFO (<https://www.hwinfo.com/>) on a computing platform equipped with an Intel Core i9-13900HX processor, 32 GB 5600 MHz memory, and an NVIDIA RTX 4060 GPU. This increase reflects the higher computational load of the third-order Volterra equalizer as the memory length increases. In particular, the processing burden grows rapidly for longer tap lengths because of the higher-dimensional Volterra kernels. Therefore, increasing the tap length beyond the selected operating points leads to limited BER improvement but a continued increase in estimated DSP power.

Based on this trade-off, 20 taps for NRZ and 40 taps for PAM-4 are selected as practical operating points to balance equalization performance and DSP power. The DSP power values in Fig. S3 are used to indicate the estimated power-scaling trend of offline VNE processing on the adopted computing platform, rather than measured absolute DSP power consumption from a real-time silicon implementation.

Supplementary Note III. Radial alignment tolerance

To further evaluate the alignment robustness of the optical wireless link, the radial alignment tolerance was characterized by recording the BER as a function of radial

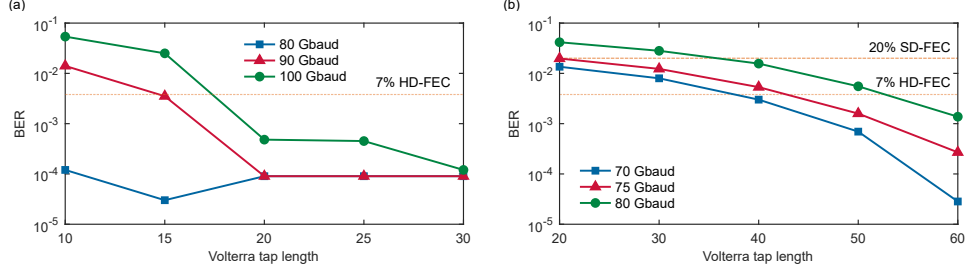


Fig. S2 BER performance as a function of Volterra tap length. (a) NRZ signaling at 80, 90, and 100 Gbaud. (b) PAM-4 signaling at 70, 75, and 80 Gbaud.

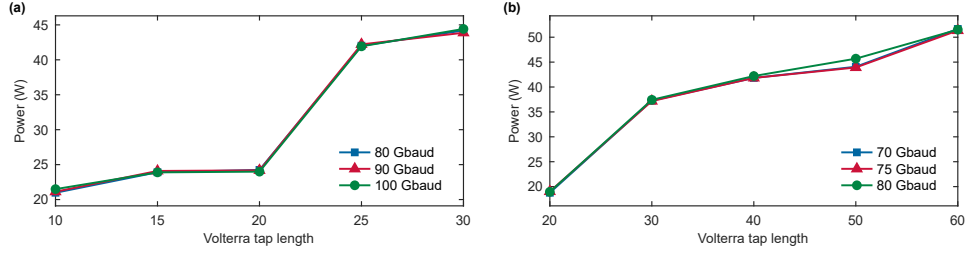


Fig. S3 Estimated DSP power as a function of Volterra tap length for NRZ and PAM-4 signaling. (a) NRZ signaling at 80, 90, and 100 Gbaud. (b) PAM-4 signaling at 70, 75, and 80 Gbaud.

displacement for two representative channels. As shown in Fig. S4, both Ch1 and Ch2 exhibit an alignment-dependent BER response, with the lowest BER obtained near the optical axis and a gradual degradation at larger radial offsets. For Ch1, the BER remains below the 20% SD-FEC threshold over the measured offset range of approximately -65 to $+65$ μm . Ch2 shows a similar trend over an offset range of approximately -60 to $+60$ μm .

The relatively modest radial tolerance is mainly attributed to the receiver-side focused coupling geometry in the present proof-of-concept setup. Although the link maintains FEC-compliant operation over the tested 0.5–2 m free-space distance range, the focused optical spot at the receiver must be accurately overlapped with the photodetector active area. Radial displacement therefore reduces the optical power coupled into the photodetector, lowering the received signal-to-noise ratio and increasing the BER. This sensitivity is determined by both the finite active area of the high-speed photodetector and the focusing condition set by the receiving optics. Further tolerance improvement is expected through optimized collimation and focusing optics, improved spot-size matching, a larger effective receiving aperture, and active or passive alignment strategies in future packaged implementations.

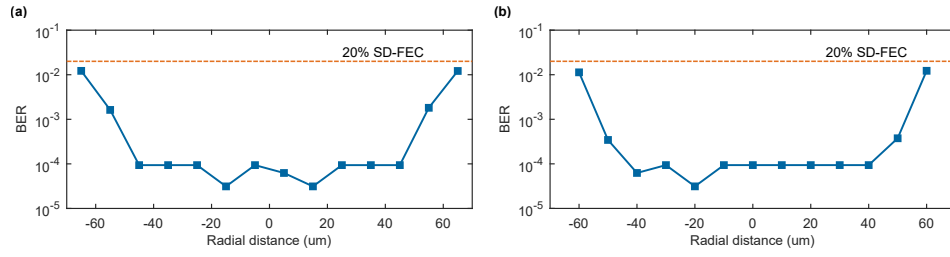


Fig. S4 Radial alignment tolerance of the 80 Gb/s NRZ optical wireless link. BER as a function of radial displacement for (a) Ch1 and (b) Ch2.